Sol SYSTEMS MANUAL,

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PREFACE

This new edition of the Sol Systems Manual contains many revisions and additions. Its release coincides with the release of a new "2708" Personality Module, and the Revision E version of the main circuit board: Sol-PC. The new "Sol-PC Rev E" has several improvements: resistors have been added which increase the reliability of the cassette motor relays, jumper options have been added, and traces moved to improve performance. Many improvements which had been accumulating as update information have been integrated into the text. Section VII, Operating Procedures, and Appendix 5, IC Pin Configurations, are now included. A subsection, Modification for 625 Line Video, has been added. If your copy is missing Section VIII, Theory of Operation, it will be available soon. New divider pages with plastic-coated tabs are included to make it easier to flip to frequently referenced sections.

Much effort has gone towards making this manual complete and accurate. The process of updating and revision always continues, however, and we invite your input. If you should find an error, or have suggestions for improving any of our documentation, please submit your suggestions in writing to our Technical Documentation Department, and they will be given thorough consideration.

The three-ring binder you are holding, is an "easel" binder. The cover is hinged from side to side, as well as down the binding, so that it may form its own "easel" stand. To use this feature, lay the manual open on a table. Bend the full width of the manual along the creased hinge, until a resistance to further bending is felt. Then set the manual up on the table, with the bottom of the pages down against the table, and the top inclining away from you. It is supported from falling by the portion of the binder you have bent back. In this position your hands are free for building, making measurements, or troubleshooting.

The first part of this manual you should read is at the very end: the Updates section. Integrate this information into your manual before you begin.

CONTENTS OUTILNE

Detailed contents precede each section.

I INTRODUCTION and GENERAL INFORMATION

II Sol POWER SUPPLY ASSEMBLY and TEST

III Sol-PC ASSEMBLY and TEST

IV PERSONALITY MODULE ASSEMBLY

V KEYBOARD ASSEMBLY and TEST

VI Sol CABINET-CHASSIS ASSEMBLY

VII OPERATING PROCEDURES

VIII THEORY OF OPERATION

IX SOFTWARE

X DRAWINGS

APPENDICES

UPDATES

This manual for the Sol Terminal Computer is made up of those sections and appendices preceded with a check (X) mark.

SECTION		TITLE	PAGE
(X)	I	INTRODUCTION and GENERAL INFORMATION	
		1.1 Introduction	I-1
		1.2 General Information	I-1
		1.2.1 Sol-PC Description	I-1
		1.2.2 Receiving Inspection	I-2
		1.2.3 Warranty Information	I-2
		1.2.4 Replacement Parts	I-2
		1.2.5 Factory Service	I-3
(X)	II	Sol POWER SUPPLY ASSEMBLY and TEST	
		2.1 Introduction	II-1
		2.2 Parts and Components	II-1
		2.2.1 Sol Regulator (Sol-REG)	II-1
		2.2.2 Power Supply Subchassis and Components	II-1
		2.3 Assembly Tips	II-5
		2.3.1 Electrical	II-5
		2.3.2 Mechanical	II-5
		2.4 Assembly Precautions	II-5
		2.5 Required Tools, Equipment and Materials . .	II-6
		2.6 Orientation	II-6
		2.6.1 Sol-REG PC Board	II-6
		2.6.2 Fan Closure Plate	II-6
		2.7 Assembly-Test	II-6
		2.7.1 Fan Closure Plate Assembly	II-7
		2.7.2 Sol-REG Assembly and Test	II-10
		2.7.3 Power Supply Subchassis Assembly and Test	II-14
(X)	III	Sol-PC ASSEMBLY and TEST	
		3.1 Parts and Components	III-1
		3.2 Assembly Tips	III-1
		3.3 Assembly Precautions	III-6
		3.3.1 Handling MOS Integrated Circuits . .	III-6
		3.3.2 Soldering	III-6

SECTION	TITLE	PAGE
(X) III	Sol-PC ASSEMBLY and TEST (Continued)	
	3.3.3 Power Connection (J10)	III-6
	3.3.4 Installing and Removing Integrated Circuits	III-6
	3.3.5 Installing and Removing Personality Module	III-6
	3.3.6 Use of Clip Leads	III-7
	3.4 Required Tools, Equipment and Materials	III-7
	3.5 Orientation (Sol-PCB)	III-7
	3.6 Sol-PC Assembly-Test Procedure	III-7
	3.6.1 Circuit Board Check	III-8
	3.6.2 Personality Module Assembly	III-9
	3.6.3 Sol-PCB Assembly and Test	III-9
(X) IV	PERSONALITY MODULE ASSEMBLY	
	4.1 Parts and Components	IV-1
	4.2 Assembly Tips	IV-1
	4.3 Assembly Precautions	IV-1
	4.4 Required Tools, Equipment and Materials	IV-1
	4.5 Orientation	IV-1
	4.6 Assembly-Test	IV-2
	4.6.1 Circuit Board Check	IV-2
	4.6.2 Assembly-Test Procedure	IV-2
(X) V	KEYBOARD ASSEMBLY and TEST	
	5.1 Parts and Components	V-1
	5.2 Assembly Tips	V-1
	5.3 Assembly Precautions	V-1
	5.4 Required Tools, Equipment and Materials	V-1
	5.5 Orientation	V-1
	5.6 Assembly-Test	V-3
	5.6.1 Circuit Board Check	V-3
	5.6.2 Assembly-Test Procedure	V-3
(X) VI	Sol CABINET-CHASSIS ASSEMBLY	
	6.1 Introduction	VI-1
	6.2 Parts and Components	VI-1

SECTION	TITLE	PAGE
(X) VI	Sol CABINET-CHASSIS ASSEMBLY (Continued)	
	6.3 Assembly Tips	VI-1
	6.3.1 General	VI-1
	6.3.2 Electrical	VI-1
	6.3.3 Mechanical	VI-5
	6.4 Required Tools, Equipment and Materials . .	VI-6
	6.5 Orientation	VI-6
	6.5.1 Sol Backplane Board, Sol-BPB	VI-6
	6.5.2 Sol Cabinet-Chassis	VI-6
	6.6 Assembly-Test	VI-7
	6.6.1 Backplane Board (Sol-BPB) Assembly .	VI-7
	6.6.2 Wooden-Masonite Parts	VI-8
	6.6.3 Sol Assembly	VI-10
( ) VII	OPERATING PROCEDURES	
( )VIII	THEORY OF OPERATION	
(X) IX	SOFTWARE	
	9.1 CONSOL	IX-1
	9.1.1 DUmp (addr) (addr)	IX-2
	9.1.2 ENter addr	IX-2
	9.1.3 TLoad (speed)	IX-2
	9.1.4 EXecute addr	IX-3
	9.1.5 BAsic	IX-3
	9.2 Standard I/O Routines	IX-3
(X)	X DRAWINGS	
	X-1 Assembly, Fan Closure Plate, Drawing #105014	
	X-2 Assembly, Sol-10 & 20 Power Supply, Drawing #105001	
	X-3 Sol-PC Assembly Drawing	
	X-4 Personality Module Assembly Drawing, PM5204	
	X-5 Personality Module Assembly Drawing, PM6834	
	X-6 Personality Module Assembly Drawing, PM2708	
	X-7 Sol Keyboard Assembly Drawing	

SECTION		TITLE	PAGE
(X)	X	DRAWINGS (Continued)	
	X-8	Side Assembly, Left-hand, Drawing #101007	
	X-9	Side Assembly, Right-hand, Drawing #101008	
	X-10	Assembly, Sol, Drawing #101000 (Sheet 1)	
	X-11	Assembly, Sol, Drawing #101000 (Sheet 2)	
	X-12	Sol-REG Schematic Drawing	
	X-13	Sol-10 Schematic Drawing	
	X-14	Sol-20 Schematic Drawing	
	X-15	Sol CPU and Bus Schematic, Drawing 1	
	X-16	Sol Memory and Decoder Schematic, Drawing 2	
	X-17	Sol Input/Output Schematic, Drawing 3	
	X-18	Sol Display Control Schematic, Drawing 4	
	X-19	Sol Audio Tape I/O Schematic, Drawing 5	
	X-20	Personality Module (PM5204) Schematic	
	X-21	Personality Module (PM6834) Schematic	
	X-22	Personality Module (PM2708) Schematic	
	X-23	Sol Keyboard Schematic	
APPENDICES			
(X)	I	Statement of Warranty	
(X)	II	8080 Operating Codes	
(X)	III	Standard Color Code	
(X)	IV	Loading DIP Devices, Soldering Tips and Installing Augat Pins	
( )	V	IC Pin Configurations	
(X)	VI	TV Interface	
(X)	VII	Memory and I/O Allocation Chart	

FIGURE	TITLE	PAGE
2-1	sol-20 fan closure plate assembly	II-7
2-2	Coaxial cable preparation	II-9
2-3	Aluminum heat sink installation	II-12
2-4	Sol-10 power supply subchassis assembly	II-15
2-5	Sol-20 power supply subchassis assembly	II-16
2-6	Sol-PC power connector and voltage measurements .	II-19
2-7	Sol-20 power connector and voltage measurements .	II-19
3-1	Identification of components	III-5
3-2	Clock circuit waveforms	III-15
3-3	Test probe for Steps 16B and 25B	III-16
3-4	Coaxial cable preparation	III-19
3-5	Display section timing waveforms	III-21
3-6	Bending selected pins on U42, 59 and 75	III-23
3-7	U14 through U21 socket jumpers	III-24
3-8	Display circuits test pattern	III-25
3-9	CPU Functional Test No. 1 display	III-29
3-10	CPU Functional Test No. 2 display	III-31
3-11	Personality module bracket/guide installation . .	III-31
4-l	R1 through R4 installation	IV-4
4-2	Handle bracket (Sol-1045) installation	IV-5
6-l	Types of screws used in Sol cabinet-chassis assembly	VI-4
6-2	Brackets used in Sol cabinet-chassis assembly . .	VI-4
6-3	Sol-20 with covers removed	VI-11
6-4	Sol-20 with covers removed	VI-11
6-5	Sol-PC coaxial cable connector assembly	VI-14
6-6	Backplane board (Sol-BPB) installation	VI-16
6-7	Backplane board (Sol-BPB) installation	VI-17
6-8	Protective foot pad installation	VI-20
7-l	Connecting the basic Sol system	VII-6
7-2	Sol control switch settings for terminal mode . .	VII-7
7-3	Location Of positioning adjustments, VR1 and VR2	VII-8

FIGURE	TITLE	PAGE
7-5	Connecting Sol to two cassette recorders	VII-29
7-6	Connecting Sol SDI to current loop device such as TTY	VII-31
7-7	Connecting Sol SDI to communications modem	VII-31
7-8	Connecting Sol PDI to parallel device	VII-32

TABLE	TITLE	PAGE
2-1	Sol Regulator Parts List	II-2,3
2-2	Sol-10 Power Supply Parts List	II-4
2-3	Sol-20 Power Supply Parts List	II-4
3-1	Sol-PC Parts List	III-2,3,4
4-1	PM2708 Personality Module Parts List	IV-1
5-1	Sol Keyboard Parts List	V-2,3
6-l	Sol-10 Cabinet-Chassis Parts List	VI-2
6-2	Sol-20 Cabinet-Chassis Parts List	VI-3
7-l	Sol Operating Controls and Their Functions	VII-2
7-2	Baud Rate Selection with Switch S3	VII-15
7-3	Word Length Selection with S4-2 & 3	VII-15
7-4	Sol Keyboard Assignments	VII-18
7-5	Control Character Symbols and Definitions	VII-23

SECTION I

INTRODUCTION and GENERAL INFORMATION

Sol-PC SINGLE BOARD TERMINAL COMPUTER™

Processor Technology

I INTRODUCTION and GENERAL INFORMATION

1.1 Introduction I-1

1.2 General Information I-2

1.2.1 Sol-PC Description I-1
1.2.2 Receiving Inspection I-2
1.2.3 Warranty Information I-2
1.2.4 Replacement Parts I-2
1.2.5 Factory Service I-2

1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the Sol-PC Single Board Terminal Computer. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all the parts and components listed in the "Parts List" (Table 3-l) in Section III. When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from poor soldering, backward installed components, and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 Sol-PC Description

The Sol-PC is a single board microcomputer/terminal built around an 8080 microprocessor. Support circuitry permits full implementation of every 8080 function.

It features both parallel and serial communications interfaces, a keyboard interface, an audio cassette interface, a video display generator, 1024 8-bit words of system RAM (random access memory), 1024 8-bit words of display RAM, and a plug-in personality module with up to 2048 bytes of ROM (read only memory) stored program, and bus compatibility with all Processor Technology hardware and firmware products. Power requirements for the Sol-PC are +5 V dc +-5% at 2.5 A, +12 V dc +-5% at 150 mA and -12 V dc +-5% at 200 mA.

Parallel interfacing is eight bits each for input and output plus control handshaking signals, and the output bus is tristated TTL for bidirectional interfaces. The serial interface circuit includes both asynchronous RS-232 and 20 mA current loop provisions, 75 to 9600 baud (switch selectable).

Seven-level ASCII encoded, TTL keyboard interfacing requires a 2 to 10 usec strobe pulse after data is stable. The dual rate, 300 or 1200 bps (bits per second), audio cassette interface is program controlled and self clocking with phase-lock loop. It includes automatic level control in both the record and playback modes. Recording is CUTS/Byte standard compatible, asynchronously Manchester coded at 1200/2400 Hz or 600/1200 Hz.

The video display circuitry generates sixteen 64 character lines from data stored in an on-card 1024 8-bit word display RAM. Alphanumeric and control characters (the full 128 upper and lower case plus control ASCII character set) are displayed black on white

or reverse (switch selectable). Solid video inversion cursors, with switch selectable blink, are programmable. The display output is standard EIA, 1.0 to 2.5 V p-p with composite negative sync, with a nominal bandwidth of 7 MHz. It can consequently be used to drive any standard video monitor. (A monochrome TV, converted for video input, can also be used. See Appendix VI.)

Included on the card are 1024 words of static, low power system RAM capable of full speed operation and a plug-in personality module which contains the software control program. Three personality modules are available for Sol:

CONSOL™--allows simple terminal operations plus direct control of the basic computer functions for entering or examining data in any memory location, or executing a program stored at a known location in memory.

SOLED™--allows advanced terminal operations with CONSOL plus screen, file and cassette tape editing/ transmission operations.

SOLOS™--allows full stand-alone terminal-computer operation.

1.2.2 Receiving Inspection

When your kit arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the kit to Processor Technology should it become necessary to do so.) If your Sol-PC kit is damaged, please write us at once describing the condition so that we can take appropriate action.

1.2.3 Warranty Information

In brief, parts which fail because of defects in materials or workmanship are replaced at no charge for 3 months for kits, and one year for assembled products, following the date of purchase. Also, products assembled by the buyer are warranted for a period of 3 months after the date of purchase; factory assembled units carry a one year warranty. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (DM8131 IC or lN2222 diode, for example) and/or a complete description (680 ohm, 1/4 watt, 5% carbon resistor, for example).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty Processor Technology products. Before returning the unit to us, first obtain our authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the unit, proceed as follows:

1. Write a description of the problem.

2. Pack the unit with the description in a container suitable to the method of shipment.

3. Ship prepaid to Processor Technology Corporation, 6200 Hollis Street, Emeryville, CA 94608.

Your unit will be repaired as soon as possible after receipt and return shipped to you prepaid. (Factory service charges will not exceed $20.00 without prior notification and your approval.)

SECTION II

Sol POWER SUPPLY

Sol TERMINAL COMPUTER™

II Sol POWER SUPPLY ASSEMBLY and TEST

2.1 Introduction II-1

2.2 Parts and Components II-1

2.2.1 Sol Regulator (Sol-REG) II-1
2.2.2 Power Supply Subchassis and Components II-2

2.3 Assembly Tips. II-5

2.3.1 Electrical II-5
2.3.2 Mechanical II-5

2.4 Assembly Precautions 11-5

2.5 Required Tools, Equipment and Materials . . II-6

2.6 Orientation II-6

2.6.1 Sol-REG PC Board II-6
2.6.2 Fan Closure Plate II-6

2.7 Assembly-Test II-6

2.7.1 Fan Closure Plate Assembly II-7
2.7.2 Sol-REG Assembly and Test II-10
2.7.3 Power Supply Subchassis Assembly and Test II-14

2.1 INTRODUCTION

The Sol power supply consists of a regulator board plus additional chassis-mounted components. This section covers assembly and test of the complete power supply.

2.2 PARTS AND COMPONENTS

2.2.1 Sol Regulator (Sol-REG)

Check all parts and components against the appropriate "Parts List", Tables 2-1, 2-2 and 2-3. If you have difficulty in identifying any parts by sight, refer to Figure 3-1 on Page III-5 in Section III of this manual.

2.2.2 Power Supply Subchassis and Components

In addition to the Sol-REG, you will need the following parts and components supplied with the Sol Cabinet-Chassis Kit. Check these parts against the appropriate "Parts List(s)", Tables 6-l and 6-2, in Section VI and separate them from the other cabinet-chassis parts.

Fan Closure Plate

Power Supply Subchassis (L-shaped)

4 each 4-40 x 3/16 Machine Screw

4 each 4-40 x 5/16 Machine Screw

4 each 4-40 Hex Nut

10 each #4 Lockwasher

14 each 6-32 x 1/2 Machine Screw

14 each 6-32 Hex Nut

16 each #6 Lockwasher

3 each 8-32 x 1/2 Machine Screw

3 each 8-32 Hex Nut

3 each #8 Lockwasher

11 each #6 x 1/4 Sheet Metal Screw

1 each #6 x 5/16 Sheet Metal Screw

2 each #4 Solder Lug

2 each 1/4" Spacer, 4-40 Tapped

Table 2-1. Sol Regulator Parts List.

INTEGRATED CIRCUITS**

1 1458 (U2)
1 7812 (U1)
1 7912 (U3)

TRANSISTORS

2 2N2222 (Q2 & 3)
1 T1P41 (Q1)

DIODES and RECTIFIERS

1 MDA101A (FWB2)
1 MDA970-1 (FWB1)
1 IR106B2 or MCR106-2 (SCR1)
2 1N4001 (D3 & 4)
1 1N4148 (D2)
1 1N5231B (D1)

RESISTORS

1	0.1 ohm,	3 watt,	5%
	or	5 watt,	5%
1	68 ohm,	1/4 watt,	5%
1	330 ohm,	1/4 watt,	5%
2	1 K ohm,	1/4 watt,	5%
4	10 K ohm,	1/4 watt,	5%
1	56 K ohm,	1/4 watt,	5%
1	1690 ohm,	1/4 watt,	5%
1	4020 ohm,	1/4 watt,	5%

CAPACITORS

2	.1	ufd, disc
3	15	ufd, tantalum dipped
2	2500	ufd, tubular electrolytic
1	"18,000	ufd, electrolytic

CABLE ASSEMBLIES

1 *Single wire, 3" (Fuse Holder to Power Switch)
1 *Single wire, 3 1/4 (Power Switch to Commoning Block)
1 Two wire, 10" (C8 to Regulator Board)

*Chassis-mounted component

**When identifying IC's, you can iqnore prefix and suffix characters in the IC nomenclature since these vary with the manufacturer. For example a 1458CP, 1458CPI and MC1458N are all 1458 This applies to all Parts Lists in this manual.

Table 2-1. Sol Regulator Parts List (Continued).

	MISCELLANEOUS
1	Sol REG Circuit Board
1	Heat Sink, 690-220-P
1	Heat Sink, 203-AP
1	Heat Sink, aluminum
1	Package Heat Sink Compound
2	Coax Connector, female* (Video Output)
1	Coax Connector, male (Video Output Cable)
1	Coax Connector Adapter Sleeve (Video Output Cable)
1	*AC Receptacle, female
1	*Fuse Holder
1	*SPST Power Switch, pushbutton (S5)
1	AC Power Cord
2	*Commoning Blocks
1	*Clamp for C8, 1 1/2"
4	Tie Wraps
3	Mica Insulators
1	4-40 x 7/16 screw
1	4-40 x 5/8 screw
2	4-40 Hex Nut
1	6-32 x 1/2 screw, metal
2	6-32 x 1/2 screw, Nylon
3	6-32 Hex Nut
5	Lockwasher, internal tooth
1	Length Solder

*Chassis-mounted component

Table 2-2. Sol-10 Power Supply Parts List.

The Sol-10 Power Supply Kit includes all Sol-REG parts listed in Table 2-l plus the following components:

1	*Power Transformer, T1
1	*Fuse, 3 amp Slo-Blo (F1)

*Chassis-mounted component

Table 2-3. Sol-20 Power Supply Parts List.

The Sol-20 Power Supply Kit includes all Sol-REG parts listed in Table 2-l plus the following components:

RESISTORS	**CAPACITORS**
1 *39 ohm, 2 watt, 5%	1 *54,000 ufd, electrolytic
RECTIFIERS	**TRANSFORMERS**
1 *MDA980-1 (FWB3)	1 *Power Transformer, T2

MISCELLANEOUS

1 *Fan	1 5-wire Cable Assembly
1 *Fan Guard	1 *Clamp for C9, 2 1/2"
1 *Fuse, 3 amp Slo-Blo	2 solder lug, internal tooth

*Chassis-mounted component

2.3 ASSEMBLY TIPS

2.3.1 Electrical

For the most part the assembly tips given in Paragraph 3.2 of Section III (Page III-l) apply to assembling the Sol regulator board and power supply.

In addition, scan Section II completely before you start to assemble the power supply.

2.3.2 Mechanical

1. If you do not have the proper screwdrivers (see Paragraph 2.5), we recommend that you buy them rather than using a knife point, a blade screwdriver on a Phillips screw, and other makeshift means. Proper screwdrivers minimize the chances of stripping threads, disfiguring screw heads and marring decorative surfaces.

2. To assure a correct fit and tight assembly, be sure you use the screws specified in the instructions.

3. Lockwashers are widely used in the power supply assembly so that screws will not loosen when subjected to stress or vibration. When a lockwasher is specified, do not omit it and make sure you install it correctly.

4. Some instructions call for prethreading holes. This is done to make assembly easier by giving you maximum working space for installing relatively hard-to-drive sheet metal screws. If you bypass prethreading instructions you will only make subsequent cabinet-chassis assembly more difficult.

To prethread a hole, insert specified screw in the hole and position it as straight as possible. While holding the screw in this position, drive it into the metal with the proper screwdriver. If started straight the screw will continue to go straight into the metal so that the head and sheet metal surfaces are in full contact.

5. The diameter of the shank (threaded portion) of a screw increases in relation to its number. For example, a 6-32 screw is larger in diameter than a 4-40 screw. Also, a #8 lockwasher is larger than a #4 lockwasher.

6. Heat sink compound is supplied with this kit in a small clear plastic package. It is a thick white substance which improves transfer between components and their heat sinks. To use the compound, pierce a small hole near the edge of the top surface of the plastic package, using a pin or sharp knife point. Squeezing the package will cause a small amount of the compound to ooze out

out of the hole, which may then be applied with a toothpick or small screwdriver blade. Spread a thin film of the compound on the mating surfaces of both the heat-generating component and the heat sink surface which it will contact. Then assemble as directed.

2.4 ASSEMBLY PRECAUTIONS

The precautions concerning soldering and the installation and removal of integrated circuits given in Paragraph 3.3 of Section III (Page 111-6) also apply to assembling the Sol regulator board.

2.5 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the Sol regulator board:

1. Needle nose pliers
2. Diagonal cutters
3. Sharp knife
4. Screwdriver, thin 1/4" blade
5. Screwdriver, #2 Phillips
6. Controlled heat soldering iron, 25 watt
7. 60-40 rosin-core solder (supplied)
8. Volt-ohm meter
9. Ruler

2.6 ORIENTATION

2.6.1 Sol-REG PC Board

Location C5 (2500 ufd capacitor) will be located in the lower right-hand corner of the circuit board when locations SCR1, Q1 and FWB1 are positioned along the top of the board. In this position the component (front) side of the board is facing up and the horizontal legends will read from left to right; the other legends will read from bottom to top. Subsequent position references related to the Sol-REG board assume this orientation.

2.6.2 Fan Closure Plate

The large circular cutout will be located in the upper right quadrant of the plate when the heavy guage doubler plate is facing UP. In this position the rectangular cutouts are on the left, the front side of the plate is facing down, the back side is facing up, and the small circular cutout is at the bottom. We suggest you label the two sides.

2.7 ASSEMBLY-TEST

NOTE: Instructions that apply only to the Sol-20 are preceded by an asterisk. Skip these instructions if you are assembling a Sol-lo.

2.7.1 Fan Closure Plate Assembly

Refer to Assembly Drawings dn Pages X-1 and 2 in Section X. (Figure 2—1 shows a completed fan closure plate assembly.)

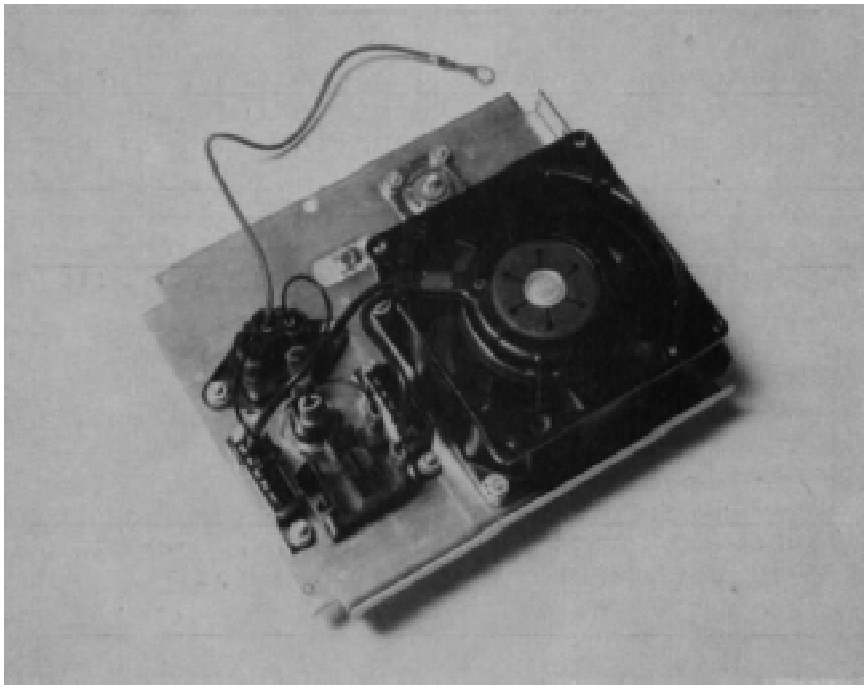


Figure 2—1. Sol-20 fan closure plate assembly.
(Top of plate in foreground.)

*( ) Step 1. Mount cooling fan and guard to fan closure plate.

Insert four 6—32 x ½″ binder or pan head screws from back side of fan closure plate. (Use the holes positioned in each quandrant of the large circular cutout.) Slip fan guard over screws on front side of plate. Position fan so that air flow will be from front to back side of plate and with its leads next to the rectangular cutouts in the place. Place #6 lockwasher on each screw and secure with 6—32 hex nut.

WARNING

FAILURE TO INSTALL FAN GUARD MAY RESULT IN DAMAGE TO THE Sol AND/OR PERSONAL INJURY.

( ) Step 2. Install power on-off switch in upper rectangular cutout in fan closure plate.

(Step 2 continued on Page il-S.)

Bend four retainer tabs on switch in and position switch with terminals facing front side of fan closure plate. Push switch unit from back side of plate through mounting hole and bend retainer tabs outward if needed to hold switch in place.

( ) Step 3. Install commoning blocks (Item 6 on drawing on Page X-l) on front side of fan closure plate, one on each side of on-off switch.

Position each block with terminal #1 at top and terminal #5 at bottom and attach each block to front side of fan closure plate with two 6-32 X 1/2 binder or pan head screws. Insert screws from back side of plate, place block over screws, on front side of plate, put #6 lockwasher on each screw and secure with 6-32 hex nut.

( ) Step 4. Install fuse holder in mounting hole located between the two rectangular cutouts in the fan closure plate.

Insert fuse holder from back side of plate, poition large tab at top, next to on-off switch,and secure holder to plate with the large lockwasher and nut supplied with holder.

( ) Step 5. Install AC Power cord receptacle on fan closure plate.

Position receptacle on front side of fan closure plate over the rectangular cutout below fuse holder. Orient receptacle with green lead at the botton and align the receptacle and closure plate mounting holes. Insert two 6-32 x 1/2 binder or pan head screws from back side of plate through each mounting hole, put #6 lockwasher on each screw and secure with 6-32 hex nut. Be sure receptacle is properly seated in cutout before tightening to avoid damage.

( ) Step 6.Install female coaxial connector on fan closure plate.

Insert connector from front side of plate so that the threaded end projects through to the back side. Then insert four 4-40 X 5/16 binder or pan head screws from back side of plate through the four connector and plate mounting holes. Place #4 lockwasher on each screw except the upper one which is closest to the AC receptacle. Secure with 4-40 hex nuts. (Leave upper nut closest to receptacle loose.)

( ) Step 7. Prepare RG59/U coaxial cable.

Cut a 13" piece of coaxial cable from that supplied with the Sol-PC kit. Strip away one inch of the outer insulation at both ends to expose shield. Unbraid shield at one end and twist it into a single lead. Do the same thing at the other end. Tin shield lead at each end and solder a #4 lug to each lead. Then remove 1/2" of the inner conductor insulation at both ends. (See Figure 2-2.)

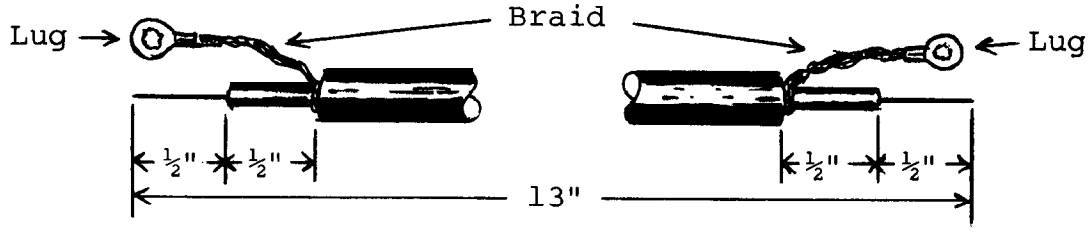


Figure 2-2. Coaxial cable preparation.

( ) Step 8. Connect coaxial cable to coaxial connector installed in Step 6.

Solder inner conductor on one end to the pin of the connector. Remove hex nut on upper connector mounting Screw closest to AC receptacle, place lug (coaxial shield) on screw and reinstall hex nut.

( ) Step 9. Connect fan closure plate wiring.

( ) Install the 3" power switch-to-commoning block cable supplied with your Sol-REG kit. Connect the female spade lug end to the upper terminal of the on-off switch and the commoning block lug end to the #1 terminal of the commoning block closest to the fan. NOTE: To install commoning block lugs, position lug with its open side facing away from the terminal numbers on the block. Then gently push lug into appropriate terminal receptacle until it is fully seated.

( ) Install the 3 1/4" fuse holder-to-power switch cable supplied with your Sol-REG kit. (This cable has female spade lugs at both ends.) Connect one end to the bottom terminal of the on-off switch and the other to the longer male spade lug on the fuse holder.

( ) Connect the AC receptacle wire closest to the fan to the other fuse holder lug. NOTE: The green AC receptacle wire will be connected later.

( ) Connect other AC receptacle wire to terminal #4 on the commoning block furthest away from the fan.

*( ) Connect upper wire of fan cord to terminal #3 of the commoning block closest to fan.

*( ) Connect lower wire of fan cord to terminal #5 of commoning block furthest from fan.

( ) Put fan closure assembly aside.

2.7.2 Sol-REG Assembly and Test

Circuit references, values and outlines are printed on the component side of the board to assist in assembly.

( ) Step 10. Visually check Sol-REG board for solder bridges (shorts) between traces, broken traces and similar defects.

If visual inspection reveals any defects, return the board to Processor Technology for replacement. If the board is not defective, proceed to next paragraph.

( ) Step 11. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R1	.1, 3 watt	none
( )	R2	330 5 watt	orange-orange-brown
( )	R3	10 K	brown-black-orange
( )	R4	10 K	" " "
( )	R5	1 K	brown-black-red
( )	R6	68	blue-gray-black
( )	R7	10 K	brown-black-orange
( )	R8	1 K	brown-black-red
( )	R9	56 K	green-blue-orange
( )	R10	10 K	brown-black-orange
( )	R11	1690	bronw-blue-white-brown
( )	R12	4020	yellow-black-red-brown

( ) step 12. Install U2 (1458) in its location between C2 and C3. U2 is positioned with pin 1 in the lower left-hand corner and soldered into place. See "Loading DIP Devices" in Appendix IV.

( ) Step 13. Install diodes D1 (1N5231B), D2 (1N4148), D3 and D4 (1N4001). Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim. BE SURE to position D1 with its cathode (dark band) to the left, D2 and D3 with their cathode at the bottom, and D4 with its cathode at the top.

( ) Step 14. Install the following capacitors in the indicated locations. Take care to observe the proper value, type and orientation, if applicable, for each installation. Bend leads outward on solder (back) side of board, solder and trim.

(See NOTE on Page 11-11.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacitor and clear the holes of' any wax. Reinsert and install.

	LOCATION	VALUE (ufd)	TYPE	ORIENTATION
( )	C1	15	Tantalum	"+" lead bottom right
( )	C2	.1	Disc	None
( )	C3	.1	Disc	None
( )	C6	15	Tantalum	"+" lead right
( )	C7	15	Tantalum	"+" lead left

( ) Step 15. Install 2500 ufd capacitors in locations C4 and C5. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim. Be sure to install C4 with its "+" lead to the right and C5 with its "+" lead to the left.

( ) step 16. Install Q2 and Q3 (2N2222) in their locations. The emitter lead (closest to tab on can) of Q2 is oriented toward the left and the base lead toward the bottom. The emitter lead of Q3 is oriented toward the bottom and the base lead toward the right.

( ) Step 17. Read assembly tip 6, on page 11-5. Apply heat sink compound to the inside of the small black "star-shaped" cooling fin, and install it, with the cylinderical grip down, on Q2 by slipping it down onto the can. Be sure heat sink does not touch any other component on the board.

( ) Step 18. Install bridge rectifier FWB 2 (MDA101A) in its location at the bottom of the board. Apply heat sink compound, per Assembly tip 6 on page 11-5. Position FWB2 with its "+" lead at the top and its "-" lead at the bottom, insert leads, solder and trim.

( ) Step 19. Install large heat sink, U1 and U3 in their locations on the bottom left corner of the circuit board.

( ) Position large black heat sink, (flat side to board) over the square foil area in the lower left corner of the PC board. Orient sink so that the two triangular cutouts in the sink are over the two triangles of mounting holes in the board.

( ) Position U1 (7812) on heat sink and observe how leads must be bent to fit mounting holes. Note that the center lead must be bent down approximately 0.2 inches.

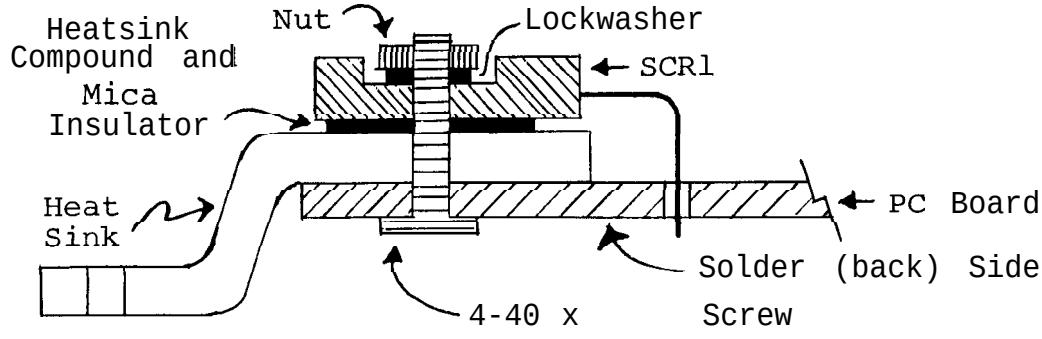
further from the body than the other two leads. Bend leads so that no contact is made with the heat sink when Ul is flat against the sink and its mounting hole is aligned with the holes in the sink and PC board. Apply heat sink compound per Assembly Tip 6, on page 11-5. Fasten U1 and sink to board using a 6-32 x 1/2 metal screw, lockwasher and nut. Insert screw from back (solder) side of board and drive nut finger tight.

( ) Position U3 (7912) on heat sink, determine how leads must be bent as you did for U1, and bend leads. Place a rectangular mica insulator over the leads of U3 so that it fully covers the bottom side of the U3 package. Apply heat sink compound to U3, the heat sink, and both sides of the mica insulator. Bend the two outside leads of U3 slightly in toward the center lead, insert leads in mounting holes as you did for U1, and fasten U3 to heat sink and PC board using a 6-32 x 1/2 Nylon screw, lockwasher and nut. Insert screw from back (solder) side of board and drive nut finger tight.

( ) Position heat sink, U1 and U3 as needed to obtain correct fit and tighten the U1 and U3 mounting screws. REMEMBER, NO LEADS CAN CONTACT THE SINK. Solder all leads and trim if required.

( ) Step 20. Install aluminum heat sink, SCR1, Q1 and bridge rectifier EWB1.

( ) Position aluminum heat sink (see Figure 2-3) along top of PC board so that the three holes in one side of the sink are aligned with the SCR1, Q1 and FWB1 mounting holes in the PC board.



(Left end, cross-section view)

Figure 2-3. Aluminum heat sink installation.

( ) Position Q1 (TIP41), with component nomenclature up, on heat sink so hole in Q1 package is aligned with the holes in sink and PC board. Observe how the leads of Q1 must be bent down to fit the pads for Q1 and bend them accordingly. Apply heat sink compound to Q1, the heat sink, and both sides of the rectangular mica insulator. Place mica insulator between heat sink and Q1, insert leads (emitter lead to right) and fasten Q1, insulator and heat sink to board with a 6-32 x 1/2 Nylon screw, lockwasher and nut. Insert screw from back (solder) side of board and drive nut finger tight.

( ) Position FWB1 (MDA970-1), with "+" lead to the right, on heat sink, determine how leads must be bent as you did for Q1, and bend leads. Apply heat sink compound. Insert leads ("+" lead to right) and fasten FWB1 and heat sink to PC board with a 4-40 x 5/8 screw, lockwasher and nut. Insert screw from back (solder) side of board and drive nut finger tight.

( ) Position SCR1 (IR106B2 or MCR106-2) on heat sink with component nomenclature up and prepare it for installation as you did Q1 and FWB1. Apply heat sink compound to SCR1, the heat sink, and both sides of the circular mica insulator. Place the mica insulator between the heat sink and SCR1, insert leads and fasten SCR1, insulator and heat sink to PC board with a 4-40 x 7/16" screw, lockwasher and nut. Insert screw from back (solder) side of board and drive nut finger tight.

( ) Check alignment of heat sink, SCR1, Q 1 and FWB2 and tighten the three mounting screws. Solder all leads and trim if required. Wipe off excess heat sink compound, if necessary. NOTE: The heat sink may have to be repositioned when you mount the Sol-REG on the power supply subchassis. This will require that you loosen the mounting screws for SCR1, Q1 and FWB2 and retighten them after repositioning the heat sink.

( ) Step 21. Connect two wire cable assembly (C8 to Regulator Board cable) to regulator. Tin ends without lugs and solder green (+) lead to pad X2 and white (-) lead to pad X3.

( ) Step 22. Test Sol-REG for short circuits. Check for continuity between FWB1 (MDA970-1) mounting screw and the following points: (The resistance should be greater than 20 ohms in all cases.)

x2	Q1, Base	D3, top lead
T2	Q1, Collector	D4, top lead
T1	D1, right-hand lead	*D3, bottom lead
Q1, Emitter	R1, left-hand lead	*D4, bottom lead

*Resistance will be initially low due to C4 and C5, but it should increase to greater than 20 ohms after a few seconds.

( ) Step 23. Set Sol-REG to one side.

2.7.3 Power Supply Subchassis Assembly and Test

( ) Step 24. Mount transformer (T1 for Sol-lo, T2 for Sol-20) on power supply subchassis (L-shaped chassis).

Position transformer as shown in drawing on Page X-2 and attach it to the subchassis with three 8-32 x 1/2 binder or pan head screws, #8 lockwashers and 8-32 hex nuts. Insert screws from bottom and outer side of chassis as shown. Place lockwasher on each screw and secure loosely with hex nuts. Slide transformer as close as possible to the edge of the chassis and tighten nuts.

NOTE

Only one of the holes in the side wall is used. Use the one that lines up with the transformer mounting tab.

( ) Step 25. Prepare transformer leads.

( ) Twist the two black wires together except for the last two inches at the commoning block lug end.

( ) Twist the two green wires together for their full length.

( ) Twist the two yellow wires together for their full length.

*( ) Twist the two blue wires together for their full length.

( ) Step 26. Connect Sol-PC power cable (4-wire cable which connects to J10 on Sol-PC) to Sol-REG. Tin ends of cable and solder green lead to pad X9, white lead to pad X1, red lead to pad X7 and white-yellow lead to pad X8.

*( ) Step 27. Connect Sol-20 DC power cable (5 wire) to Sol-REG. Tin ends of cable and solder white lead to pad X4 (above R8), red-white lead to pad X5 (between C5 and FWB2) and yellow-white lead to pad X6 (left of C5).

( ) Step 28. Connect transformer leads to Sol-REG.

( ) Solder green leads to pads T1 and T2, white-yellow lead to pad T3 and yellow leads to pads T4 and T5 on Sol-REG circuit board.

( ) Step 29. Prethread the three Sol-REG heat sink mounting holes in the power supply subchassis shown in drawing on page X-2 with #6 x 5/16 sheet metal screws. Remove screws.

( ) Step 30. Place #4 lockwashers on two 4-40 x 3/16 binder or pan head screws. Insert these screws from the bottom side of the power supply subchassis through the two mounting holes located near the middle of the bottom of the power supply subchassis, one on each side. Place another *4 lockwasher on the screws and drive each screw tightly into a 4—40 x ¼ tapped spacer.

( ) Step 31. Position Sol—REG PC board with top edge over the previously installed spacers. Place #4 lockwashers on two 4—40 x 3/16 binder or pan head screws and drive screws t through Sol-REG board into spacers.

( ) Step 32. Attach heat sink on Sol—REG to power supply sub-chassis as shown in drawing on Page X-2. At this point use only the two side screws which you used in Step 29 to pre—thread the holes. (The middle screw will be installed later.) Place a #6 lockwasher on each screw before driving it through the sink into the subchassis. Figure 2—4 shows an assembled Sol—lO power supply subchassis.

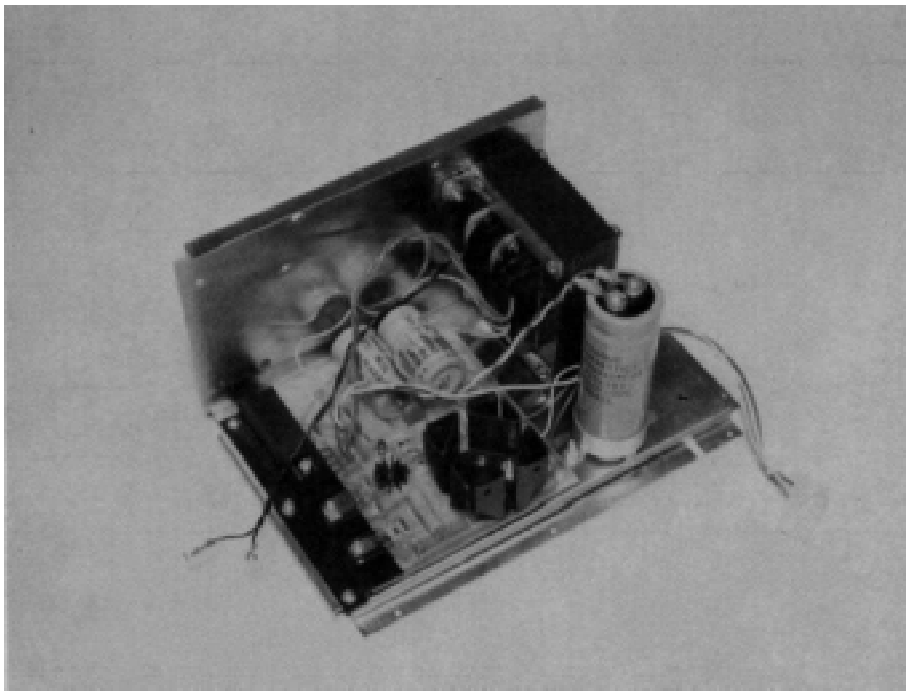


Figure 2—4. Sol-lO power supply subchassis assembly. (Rear of subchassis at left.)

*( ) SteP 33. Install bridge rectifier FWB3 on power supply subchassis.

(Step 33 continued on Page 11-16.)

Position FWB3 (MDA980-l) on power supply subchassis as shown in drawing on Page X-2. BE SURE NEGATIVE (-) TERMINAL OF FWB3 is next to transformer. Insert a 6—32 x. ½ binder or pan head screw from bottom of subchassis, place #6 lockwasher on screw and secure with 6—32 hex nut.

*( ) Step 34. Connect blue transformer wires to unmarked terminals of FWB3.

*( ) Step 35. Install large (2½") mounting ring for C9 (54,000 ufd capacitor) on side wall of power supply subchassis as shown in drawing on Page X-2.

Position ring over the three mounting holes in the side wall of subchassis so the clamping screw faces the bottom of subchassis and so it will be accessible from the Sol—REG end of the subchassis. Insert three 6—32 x ½ binder or pan head screws from outer side of side wall through the mounting holes. Place #6 lockwasher on each screw and secure with 6-32 hex nut. Figure 2-5 shows an assembled Sol-20 power supply subchassis.

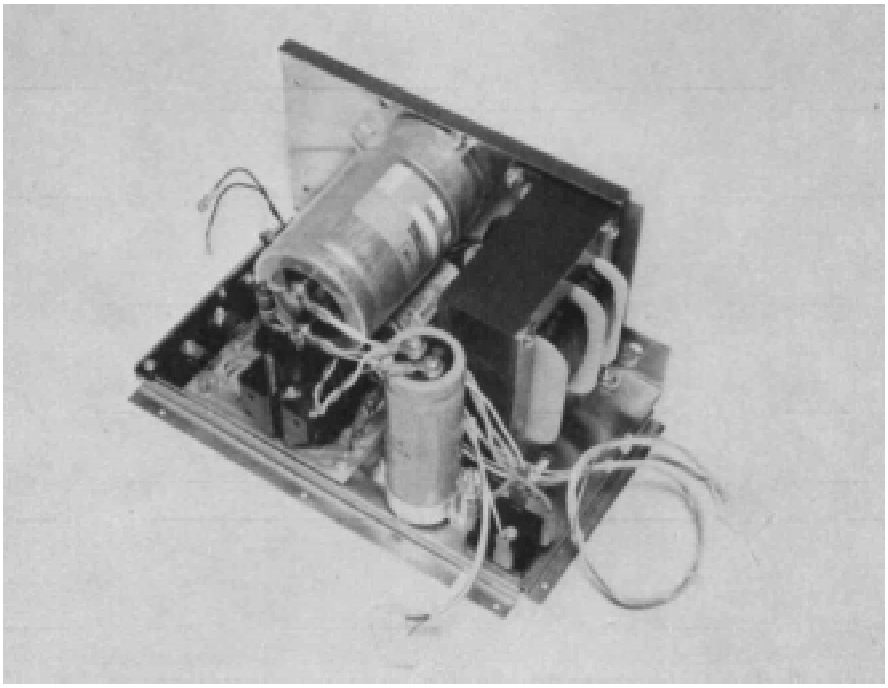


Figure 2-5. Sol—20 power supply subchassis assembly. (Rear of subchassis at left.)

( ) Step 36. Install small (1½") mounting ring for C8 (18,000 ufd capacitor) as shown in drawing on Page X—2.

(Step 36 continued on Page 11—17.)

Position ring over the two mounting holes located between FWB3 and the Sol-REG so that the clamping screw is positioned between the transformer and FWB3. Insert two 6-32 x 1/2 binder or pan head screws from bottom side of chassis through the mounting holes. Place #6 lockwasher on each screw and secure with 6-32 hex nut. (Refer to Figure 2-4.)

( ) Step 37. Route Sol-PC power cable between C8 mounting ring and the transformer, mount C8 in its mounting ring, and tighten clamping-screw. (See Figure 2-4.)

( ) Step 38. Connect white wire of C8 cable to negative (-) terminal of C8 and green wire to positive (+) terminal of C8. (This cable was soldered to the Sol-REG when you assembled it.) Remove terminal screws, place #10 lockwasher on each screw, place cable lugs on screws and drive screws tightly into appropriate terminals.

*( ) Step 39. Mount C9 in its mounting ring with its "+" terminal slightly toward C8 and tighten clamping screw. (See Figure 2-5.)

*( ) Step 40. Prepare R13 (39 ohm 2 watt) for installation on C9.

Solder a #10 lug to each lead of R13. Bend leads of R13 to fit the terminals of C9. (R13 should fit on C9 as shown in Figure 2-5.)

*( ) Step 41. Connect Sol-20 DC power cable (5 wire) and R13 to C9. Route cable between C8 and transformer.

Remove terminal screws from C9. Place lockwasher, terminal screw, blue lead of Sol-20 DC cable and one R13 lead on one terminal screw and drive it into the positive (+) terminal on C9. Attach lockwasher, white cable lead and other R13 lead to negative (-) terminal on C9 in the same manner. Tighten both capacitor terminals tightly.

CAUTION

LOOSE CONNECTIONS ON C9 CAN LEAD TO ARCING AND SUBSEQUENT POWER SUPPLY DAMAGE.

*( ) Step 42. Connect blue pigtail of Sol-20 DC cable to positive (+) terminal of FWB3. (This pigtail has a spade lug at its free end and is connected to the lug you just attached to the positive terminal of C9.) Connect white pigtail of Sol-20 DC cable to negative (-) terminal of FWB3. (This pigtail has a spade lug at its free end and is connected to the lug you just attached to the negative terminal of C9.)

( ) Step 43. Connect green lead from AC receptacle (mounted on fan closure plate) to power supply subchassis assembly as shown in drawing on Page X-2. (Use the #6 x 1/4 sheet metal screw with which you prethreaded the middle Sol-REG heat sink mounting hole in Step 29.) Place lug on screw and drive screw into the middle Sol-REG heat sink mounting hole.

( ) Step 44. Route black transformer leads along side wall of power supply subchassis out toward the Sol-REG heat sink. (See Figure 2-4.) Attach one lead to pin 2 of the commoning block (mounted on fan closure plate) nearest the fan. Attach other lead to pin 3 of the other commoning block.

( ) Step 45. Install cable tie wraps.

( ) Install one wrap around the wires that connect to Sol-REG pads T1,2,3,X2 and X3 as shown in the Detail A - Wiring portion of the drawing on Page X-2.

*( ) Install another wrap around the leads from C9 as shown in Detail B of drawing on Page X-2.

Two other wraps are supplied with your kit. Use them as appropriate to make your power supply cabling neater.

( ) Step 46. Using a #6 x 1/4 sheet metal screw, attach fan closure plate to power supply subchassis as shown in Drawing No. X-2.

( ) Step 47. Push on-off switch in and out to determine the OFF position (switch mechanically out). With switch in OFF position, connect AC power cord to AC receptacle. Then plug power cord into 110 V ac outlet.

( ) Step 48. Test power supply for proper operation.

( ) Make sure on-off switch is in OFF position.

( ) Install fuse in fuse holder. CAUTION: NEVER INSTALL OR REMOVE FUSE WITH POWER ON.

( ) Check connector on Sol-PC power cable (4 wire) to insure it is wired as shown in Figure 2-6.

*( ) Check connector on Sol-20 power cable (5 wire) to insure it is wired as shown in Figure 2-7.

( ) Turn on-off switch ON.

( ) Measure the voltages at the Sol-PC connector at the points indicated in Figure 2-6. The voltages must be as given in Figure 2-6. NOTE: Do not take voltage measurements at any other points in the power supply, even through they may be more accessible. It is important that the indicator voltages be available at the connector.

*( ) Measure the voltages at the Sol-20 connector at the points indicated in Figure 2-7. The voltages must be within the ranges given in Figure 2-7. (See preceding NOTE.)

( ) If the power supply fails any of the preceding tests, locate and correct the cause before proceeding.

If the power supply is operating correctly, turn on-off switch OFF, disconnect power cord, set power supply to one side and go on to Section III.

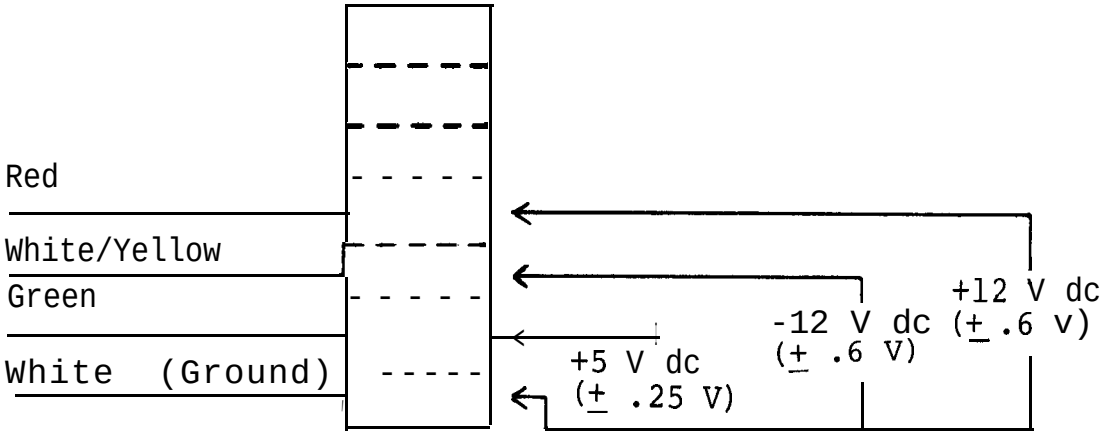


Figure 2-6. Sol-PC power connector and voltage measurements.

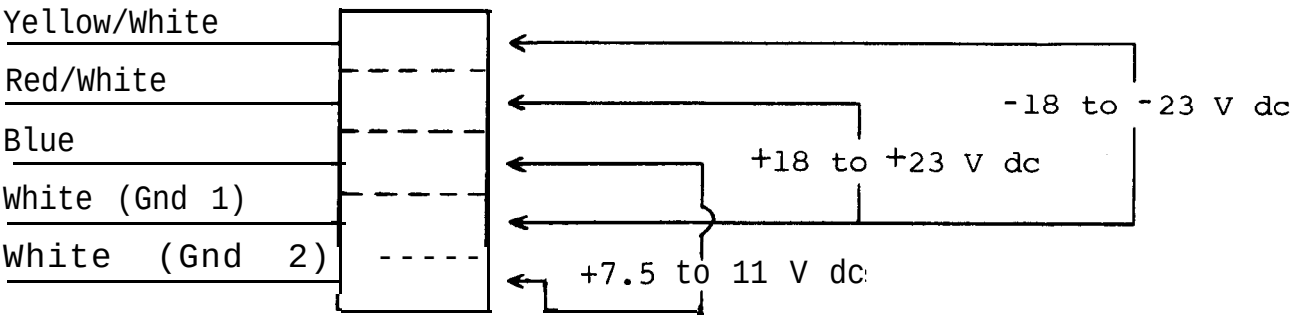


Figure 2-7. Sol-20 power connector and voltage measurements.

SECTION III

ASSEMBLY

and

TEST

Sol-PC SINGLE BOARD TERMINAL COMPUTER™

Processor Technology

III Sol-PC ASSEMBLY and TEST

3.1 Parts and Components III-1

3.2 Assembly Tips III-1

3.3 Assembly Precautions III-6

3.3.1 Handling MOS Integrated Circuits . . III-6
3.3.2 Soldering III-6

3.3.3 Power Connection (J10) III-6
3.3.4 Installing and Removing Integrated Circuits III-6
3.3.5 Installing and Removing Personalit Module III-6
3.3.6 Use of Clip Leads III-7

3.4 Required Tools, Equipment and Materials . . III-7

3.5 Orientation (Sol-PCB) III-7

3.6 Sol-PC Assembly-Test Procedure III-7

3.6.1 Circuit Board Check III-8
3.6.2 Personality Module Assembly III-9
3.6.3 Sol-PCb Assembly and Test III-9
3.6.4 Modification for 625 Line Video . . . III-40

3.1 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" on Pages III-2 through III-4 (Table 3-l). If you have difficulty in identifying any parts by sight, refer to Figure 3-l on Page 111-5.

3.2 ASSEMBLY TIPS

1. Scan Sections III and IV in their entirety before you start to assemble your Sol-PC kit.

2. In assembling your Sol-PC, you will be following an integrated assembly-test procedure. Such a procedure is designed to progressively insure that individual circuits and sections in the Sol-PC are operating correctly. IT IS IMPORTANT THAT YOU FOLLOW THE STEP-BY-STEP INSTRUCTIONS IN THE ORDER GIVEN.

3. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

4. When installing components, make use of the assembly aids that are incorporated on the circuit boards and the assembly drawings. (These aids are designed to assist you in correctly installing the components.)

   a. The circuit reference (R3, C10 and U20, for example) for each component is silk screened on the PC boards near the location of its installation.

   b. Both the circuit reference and value or nomenclature (1.5K and 74H00, for example) for each component are included on the assembly drawings near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that the color codes or imprints read from left to right and top to bottom as appropriate (boards oriented as defined in Paragraph 3.5 on Page 111-7).

6. Unless specified otherwise, install components, especially disc capacitors, as close as possible to the boards.

7. Should you encounter any problem during assembly, call on us for help if needed.

Table 3-1. Sol-PC Parts List.

INTEGRATED CIRCUITS

1 AM0026 or DMO026 (U104)	1 74S04 (U92)
1 4N26 (U39)	2 7406 (U57,87)
1 8T94 (U58)	2 74LS10 (U47,61)
5 8T97 (U67,68,77,80,81)	3 74LS20 (U23,59,83)
2 1458CP or 1558CP (U56,108)	1 74LS86 (U74)
1 1489A (U38)	8 74LS109 (U43,52,63,64,70, 72,73,75)
2 TMS6O11NC (U51,69)	1 74LS136 (U22)
1 MCM6574 or MCM6575 (U25)	3 74LS138 (U34,35,36)
1 4001 (U102)	3 74LS157 (U12,30,32)
2 4013 (U100,113)	4 74LS163 or 25LS163 (U28,31,33,40)
1 4019 (U111)	1 74166 (U41)
1 4023 (u98)	2 74173 (U95,96)
1 4024 (U86)	1 74175 (U97)
1 4027 (U101)	9 74LS175 or 25LS175 (U2,13,26,27,42,76,90,93,106
3 4029 (U1,11,84)	**4** 74LS253 (U65,66,78,79)
1 4030 (U99)	**7** 74LS367 (U29,37,50,71,89, 94,107)
2 4046 (U85,110)	**1** 8080, 8080A or 9080A (U105)
2 4049 (U88,109)	**1** 8836 or 8T380 (U46)
1 4520 (U112)	**16** 91L02APC or 2102L1PC (U3 - 10, U14 - 21)
1 74H00 (U91)	**1** 93L16 (U62)
3 74LS00 (U44,48,55)	
2 74LS02 or 9LS02 (U53,60)	
4 74LS04 (U24,45,49,54)	

TRANSISTORS

2 2N2222 (Q4 & Q5)
2 2N2907 or 2N3460 (Q1 & Q2)
1 2N4360 (Q3)

DIODES

9 1N4148 or 1N914 (D1,D3 - 10)
1 1N5231B Zener Diode (D11)
4 1N4001 (D2,12,13,14)

CRYSTAL

1 14.318 MHz in HC-18/U Case (XTAL)

RELAYS

2 DIP Reed, Sigma 19l-TE1A15S (K1 & K2)

Table 3-1. Sd—PC Parts List (Continued).

RESISTORS

2	6.8	ohm, ½ watt, 5%
2	47	ohm, ¼ watt, 5%
1	75	ohm, ¼ watt, 5%
1	100	ohm, ¼ watt, 5%
3	100	ohm, ½ watt, 5%
1	200	ohm, ¼ watt, 5%
13	330	ohm, ¼ watt, 5%
1	330	ohm, ½ watt, 5%
3	470	ohm, ¼ watt, 5%
2	470	ohm, ½ watt, 5%
9	680	ohm, ¼ watt, 5%
63	1.5K	ohm, ¼ watt, 5%
1	3.3K	ohm, ¼ watt, 5%
6	5.6K	ohm, ¼ watt, 5%
32	10 K	ohm, ¼ watt, 5%
1	15 K	ohm, ¼ watt, 5%
2	39 K	ohm, ¼ watt, 5%
1	47 K	ohm, ¼ watt, 5%
3	50 K	ohm, Potentiometer
4	100 K	ohm, ¼ watt, 5%
2	150 K	ohm, ¼ watt, 5%
2	1 M	ohm, ¼ watt, 5%
1	2.2M	ohm, ¼ watt, 5%
2	3.3M	ohm, ¼ watt, 5%

CAPACI TORS

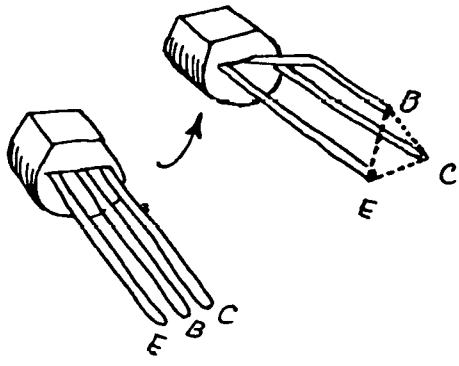
1	10	pfd, disc
1	330	pfd, disc
1	470	pfd, disc
3	680	pfd, monolythic or disc ceramic (labeled 681 and usually blue)
6	.001	ufd,
2	.001	ufd,
2	.01	ufd,
37	.047	ufd,
12	.1	Ufd,
1	.1	ufd,
1	.68	ufd,
1	1	ufd, tantalum dipped (usually orange or red)
5	15	ufd, tantalum dipped (usually orange or red)
1	100	ufd, aluminum electrolytic

CONNECTORS

1 25-pin Female, AMP206584—2 (J1)
1 25—pin Male, AMP206604—1 (J2)
2 20—pin Header, 3M3492-2002 (J3 & J4)
1 30-pin Right Angle Edge Connector, VIKING 3KH15/1JKC15 (J5)
2 Miniature Phone Jack (J6 & J7)
2 Subminiature Phone Jack (J8 & J9)
1 7-pin Male Locking Molex Connector (J1O)
1 100—pin Edge Connector, TI H322150-0306A (J11)
1 Molex-type DC Power Cable, mates with JlO (prefabricated)

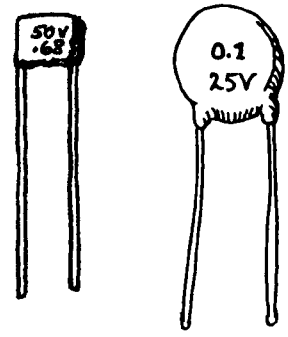
Table 3-1. Sal—PC Parts List (Continued).

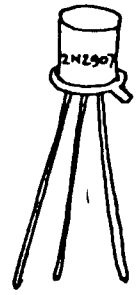
MISCELLANEOUS		
1	Sol—PCB Circuit Board	length of #24 bare wire
2	8-pin DIP Socket	
29	14-pin DIP Socket	
74	16-pin DIP Socket	
1	24-pin DIP Socket	
3	40-pin DIP Socket	
16	Augat Pins on Carrier	
2	DIP Switch, 6 position (Sl & S4)	
2	DIP Switch, 8 position (S2 & S3)	
1	4-foot Length 72-ohm Coaxial Cable	
1	Tie Wrap for Coaxial Cable	
2	Mounting Bracket, Sol-1040	
2	Card Guide, SAEl250F	
10	#4 Lockwasher, internal tooth	
2	#4 Insulating Washer	
4	4-40 x ¼ Binder Head Screw	
6	4-40 x 7/16 Binder Head Screw	
2	4-40 x 5/8 Binder Head Screw	
10	4-40 Hex Nut	
1	Length Solder	
1	Manual	
1	Personality Module Kit (See Section IV for contents.)	

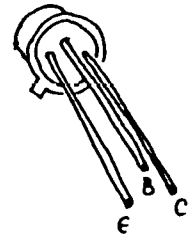


Transistor
TO-92 Package (Plastic)

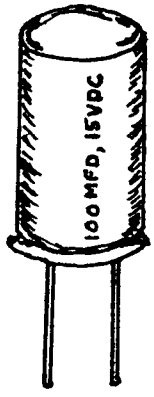
Monolythic (left)
and Ceramic Disc
Capacitors





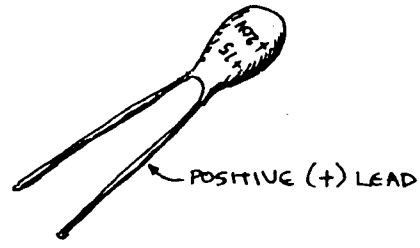


Transistor
TO-18 Package (Metal Can)

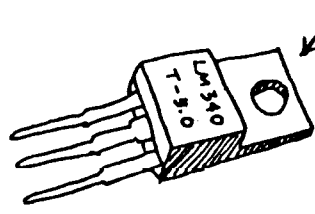


Electrolytic
Capacitor
(vertical mount)

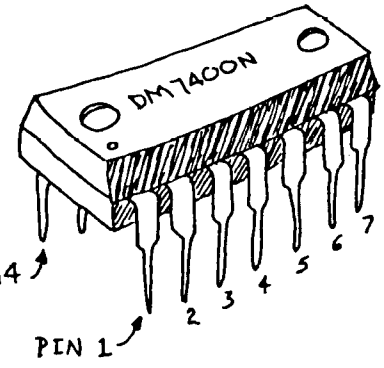
Mylar Tubular
Capacitor



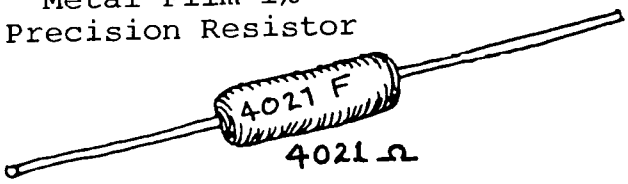
Dipped Tantalum
Electrolytic Capacitor

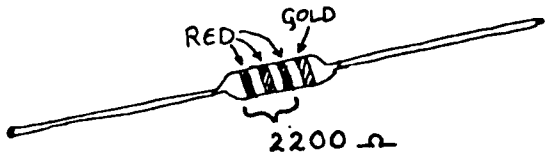


Regulator IC or
Power Transistor (TO-220)

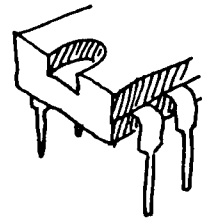


Metal Film 1%
Precision Resistor





Carbon Film Resistor
5% (gold), 10% (silver)



NOTE: PIN 1 MAY BE INDICATED BY CORNER DOT OR CUT-OUT

Dual Inline Package (DIP) IC
(8,14,16,24 or 40 pins)

Figure 3-1. Identification of components.

3.3 ASSEMBLY PRECAUTIONS

3.3.1 Handling MOS Integrated Circuits

Many of the IC's used in the Sol-PC are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC. Also, avoid unnecessary handling and wear cotton--rather than synthetic--clothing when you do handle these IC's.

3.3.2 Soldering **IMPORTANT**

1. Use a fine tip, low-wattage iron, 25 watts maximum.

2. DO NOT use excessive amounts of solder. DO solder neatly and as quickly as possible.

3. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.

4. To prevent solder bridges, position iron tip so that it does not touch adjacent pins and/or traces simultaneously.

5. DO NOT press tip of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage the board.

6. The Sol-PC uses circuit boards with plated-through holes. Solder flow through to the component (front) side of the board can produce solder bridges. Check for such bridges after you install each component.

7. The Sol-PC circuit boards have integral solder masks (a lacquer coating) that shield selected areas on the boards. This mask minimizes the chances of creating solder bridges during assembly. DO, however, check all solder joints for possible bridges.

8. Additional pointers on soldering are provided in Appendix IV of this manual.

3.3.3 Power Connection (J10)

NEVER connect the DC power cable to the Sol-PC when power supply is energized. To do so can damage the Sol-PC.

3.3.4 Installing and Removing Integrated Circuits

NEVER install or remove integrated circuits when power is applied to the Sol-PC. To do so can damage the IC.

Installing and Removing Personality Module

NEVER install or remove the plug-in personality module when power is applied to the Sol-PC. To do so can damage the module.

3.3.6 Use of Clip Leads

TARE CARE when using a clip lead to establish a ground connection when testing the Sol-PCB circuit board. Make sure that the clip makes contact only with the ground bus on the perimeter of the board.

3.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling and testing the Sol-PC:

1. Needle nose pliers
2. Diagonal cutters
3. Screwdriver
4. Sharp knife
5. Controlled heat soldering iron, 25 watt
6. 60-40 rosin-core solder (supplied)
7. Small amount of #24 solid wire
8. Volt-ohm meter
9. Video monitor or monochrome TV converted for video input.
10. IC test clip (optional)
11. Oscilloscope (optional)

3.5 ORIENTATION (Sol-PCB)

Location J5 (personality plug-in module connector) will be located in the upper right-hand area of the circuit board when location J10 (power connector) is positioned at the bottom of the board. In this position the component (front) side of the board is facing up and all IC legends (U1 through U10, U22 through U24, etc.) will read from left to right. Subsequent position references related to the Sol-PCB assume this orientation.

3.6 Sol-PC ASSEMBLY-TEST PROCEDURE

The Sol-PC is assembled and tested in sections and/or circuits. You will first test the Sol-PCB circuit board for shorts (solder bridges) between the power buses and ground. After assembling

the personality module (see Section IV), the clock and display control circuits are assembled. The bus, CPU, decoder and memory circuits are then assembled, followed by the parallel and serial input/output (I/O) and audio cassette I/O sections.

CAUTION

THE Sol-PC USES MANY MOS INTEGRATED CIRCUITS. THEY CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGE. HANDLE THESE IC's SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON, RATHER THAN SYNTHETIC, CLOTHING WHEN YOU DO HANDLE MOS IC's. (STATIC CHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY CONDITIONS.)

3.6.1 Circuit Board Check

( ) Visually check Sol-PCB board for solder bridges (shorts) between traces, broken traces and similar defects.

( ) Check board to insure that the +5-volt-bus, +12 volt-bus and -12-volt bus are not shorted to each other or to ground. Using an ohmmeter, on "OHMS X 1K" or "OHMS X 10K" scale, make the following measurements (refer to Sol-PC Assembly Drawing X-3).

( ) +5-volt Bus Test. Measure between positive and negative mounting pads for C58. There should be no continuity. (Meter reads close to "infinity" ohms.)

( ) +12-volt Bus Test. Measure between positive and negative mounting pads for C59. There should be no continuity.

( ) -12-volt Bus Test. Measure between positive and negative mounting pads for C60. There should be no continuity.

( ) 5/12/(-12) Volt Bus Test. Measure between positive mounting pads for C58 and C59, between positive pad for C58 and negative pad for C60, and between positive pad for C59 and negative pad for C60. You should measure no continuity in any of these measurements.

If visual inspection reveals any defects, or you measure continuity in any of the preceding tests, return the board to Processor Technology for replacement. If the board is not defective, proceed to next paragraph.

3.6.2 Personality Module Assembly

Since the personality module is required for testing the Sol-PC in the later stages of its assembly, we suggest that you assemble the personality module first. In so doing, your Sol-PC assembly will proceed uninterrupted. Assembly instructions for the personality module are provided in Section IV of this manual.

If you wish to wait to assemble the personality module until it is needed, go on to Paragraph 3.6.3.

3.6.3 Sol-PCB Assembly and Test

Refer to Sol-PC assembly drawing X-3.

( ) Step 1. Install DIP sockets. Install each socket in the indicated location with its end notch oriented as shown on the circuit board and assembly drawing. Take care not to create solder bridges between the pins and/or traces. (Refer to footnotes at end of this step before installing U105.)

INSTALLATION TIP

Insert socket pins into mounting pads of appropriate location. On solder (back) side of board, bend pins at opposite corners of socket (e.g., pins 1 and 9 on a 16-pin socket) outward until they are at a 45 angle to the board surface. This secures the socket until it is soldered. Repeat this procedure with each socket until all are secured to the board. Then solder the unbent pins on all sockets. Now straighten the bent pins to their original position and solder.

LOCATION	TYPE SOCKET
( ) U1 through 21	16 pin
( ) U22 through 24	14 pin
( ) U25	24 pin
( ) U26 through 37	16 pin
( ) U38	14 pin
( ) U39	None
( ) U40 through 43	16 pin
( ) U44 through 49	14 pin
( ) U50	16 pin
( ) U51	40 pin
( ) U52	16 pin
( ) U53 through 55	14 pin
( ) U56	8 pin
( ) U57 through 61	14 pin

(Continued on Page

LOCATION	TYPE SOCKET
( ) U62 through 68	16 pin
( ) U69	40 pin
( ) U70 through 73	16 pin
( ) U74	14 pin
( ) U75 through 81	16 pin
( ) U82#	None#
( ) U83	14 pin
( ) U84,85	16 pin
( ) U86,87	14 pin
( ) U88 through 90	16 pin
( ) U91,92	14 pin
( ) U93 through 97	16 pin
( ) U98 through 100	14 pin
( ) UlOl	16 pin
( ) U102	14 pin
( ) U103*	None#
( ) U104	None
( ) U105*	40 pin
( ) U106,107	16 pin
( ) UlOB	8 pin
( ) U109 through 112	16 pin
( ) U113	14 pin

#Spare locations, not used.
*Note that U105 notch is positioned at the top.

( ) Step 2. Install the following capacitors in the indicated locations. Take care to observe the proper value, type and orientation, if applicable, for each installation. Bend leads outward on solder (back) side oiI board, solder and trim.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacitor and clear the holes of any wax. Reinsert and install.

LOCATION	VALUE (ufd)	TYPE	ORIENTATION
( ) Cl	.047	Disc	None
( ) C2	.047	″	″
( ) C3	.047	″	″
( ) C4	.047	″	″
( ) C5	.047	″	″
( ) C6	.047	″	″
( ) C7	.047	″	″
( ) C8	.047	″	″

	LOCATION	VALUE (ufd)	TYPE	ORIENTATION
( )	C10	.047	Disc	None
( )	C11	.047	"	"
( )	C13	.047	"	"
( )	C14	.047	"	"
( )	C15	15	Tantalum	"+" lead bottom
( )	C16	.047	Disc	None

( ) Step 3. Check for +5-volt bus to ground shorts. Using an ohmmeter, measure between positive and negative mounting pads for C58. There should be no continuity. If there is, find and correct the problem before proceeding to Step 4.

( ) Step 4. Install the following capacitors in the indicated locations. Take care to observe the proper value1 type and orientation, if applicable, for each installation. Bend leads outward on solder (back) side of board, solder and trim. (refer to NOTE in Step 2.)

	LOCATION	VALUE (ufd)	TYPE	ORIENTATION
( )	C19	.047	Disc	None
( )	C20	.047	"	"
( )	C21	.047	"	"
( )	C24	.047	"	"
( )	C25	.047	"	"
( )	C26	.047	"	"
( )	C33	.047	"	"
( )	C38	.047	"	"
( )	C40	15	Tantalum	+" lead bottom
( )	C41	.047	Disc	None
( )	C42	.047	"	"
( )	C45	.047	"	"
( )	C56	.047	"	"
( )	C58	15	Tantalum	"+" lead top
( )	C59	15	Tantalum	"+" lead top
( )	C60	15	Tantalum	"+" lead top
( )	C65	.047	Disc	None

( ) Step 5. Check for +5-volt bus to ground shorts. Using an ohmmeter, measure between the positive and negative leads of C58. You should measure at least 100 ohms. Less than 100 ohms indicates a short. If required, find and correct the problem before proceeding to Step 6. NOTE: In this and subsequent resistance measurements, any value greater than the minimum may normally occur, even much higher, unless otherwise indicated.

( ) Step 6. Install the following capacitors in the indicated locations. Take care to observe the proper value and type for each installation. Bend leads outward on solder (back) side of board, solder and trim. (Refer to NOTE in Step 2.)

(Step 6 continued on Page 111–12.)

	LOCATION	VALUE (ufd)	TYPE	ORIENTATION
( )	C9	.047	Disc	None
( )	C12	.047	"	"
( )	C17	.047	"	"
( )	C18	.047	"	"
( )	C22	.047	"	"
( )	C23	.047	"	"
( )	C27	.047	"	"
( )	C28	.047	"	"
( )	C46	.047	"	"

( ) Step 7. Check for +5-volt bus to ground shorts. Using an ohmmeter, measure between the positive and negative leads of C58. You should measure some resistance. Zero resistance indicates a short. If required, find and correct the problem before proceeding to Step 8.

( ) Step 8. Install diodes D8 (1N4148 or 1N914), D11 (1N5231B) and D12 (1N4001) in their locations (in the area below U90 through U92). Position D8 with its dark band (cathode) to the right, Dll with its band at the bottom, and D12 with its band at the top.

NOTE

The leads of D12 and its mounting holes are a snug fit. Take care when instal-ling this diode.

( ) Step 9. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

	LOCATION	VALUE ohms	COLOR CODE
( )	R104	10 K	brown-black-orange
( )	R105	1.5K	brown-green-red
( )	R106	1.5K	" " "
( )	R130	100, ½ watt	brown—black—brown
( )	R131	100, ½ watt	" " "
( )	R132	100, ½ watt	" " "
( )	R133	330	orange-orange-brown
( )	R134	330	" " "
( )	R135 & 136	10 K	brown-black-orange
( )	R137 & 138	47	yellow—violet—black

( ) Step 10. Install the following capacitors in the indicated locations. Take care to observe the proper value and type for each installation. Bend leads outward on solder (back) side of board, solder and trim. (Refer to NOTE in Step 2.)

LOCATION	VALUE	TYPE
( ) C39	.1 ufd	Disc
( ) C43	680 pfd	Monolythic or Disc
( ) C44	680 pfd	Monolythic or Disc
( ) C61	.001 ufd	Disc
( ) C62	.68 ufd	Monolythic
( ) C63	.1 ufd	Disc
( ) C64	10 pfd	Disc

( ) Step 11. Install 14.318 MHz crystal in its location just above C61. Insert leads and pull down until the case is 1/16" above the front surface of the board. Solder quickly and trim.

( ) Step 12. Install male Molex connector in location J10. Position connctor so the locking clip is facing the crystal (XTAL), insert shorter pins in mounting holes and solder.

( ) Step 13. In the jumper area labeled CLK on the assembly drawing (between U90 and U91), install Augat pins in mounting holes A,B,C,D and E. (Refer to "Installing Augat Pins" in Appendix IV.) Using #24 bare wire, install a jumper between the A and B pins and another jumper between the D and E pins.

( ) Step 14. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation. DO NOT SUBSTITUTE FOR ANY OF THESE IC's.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( ) U77	8T97
( ) U90	74L5175 or 25L5175
( ) U91	74H00
( ) U92	74S04
( ) U104*	AM0026 or DM0026*

*Solder this IC in its location. See "Loading DIP Devices" in Appendix IV.

( ) Step 15. Connect power to power connector J10. Power and interconnection requirements are as follows:

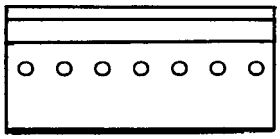
(Step 15 continued on Page 111-14.)

CAUTION 1

NEVER CONNECT POWER CABLE TO J10 WITH POWER SUPPLY ENERGIZED.

CAUTION 2

MAKE SURE POWER CABLE CONNECTOR MATES EXACTLY WITH J10; THAT IS, PIN 1 TO PIN 1, PIN 2 TO PIN 2, ETC. ANY OTHER MATING RELATIONSHIP WILL "BLOW" THE IC' s.



1 2 3 4 5 6 7
(J10, Top View)

J10 PIN NO.	POWER
1	Ground
2and6	+5Vdc+5%, 2 Amax
3and5	-l2Vdc+5%, 300mAmax
4	+l2Vdc+5%, l00mAmax
7	Ground

NOTE

Though not labeled on the connector, J10 pins are designated 1 through 7, reading from left to right.

( ) Step 16. Check clock circuits. If you have an oscilloscope, use part A of this step. If you do not, use part B.

A. Oscilloscope Check

( ) Using an oscilloscope, check for the waveforms given in Figure 3-2 on Page 111-15 at the indicated observation points and in the order given. The waveforms shown in Figure 3—2 approximate actual waveforms. If any waveforms are incorrect, determine and correct the cause before proceeding with assembly.

NOTE

Irregularities up to 1 volt are acceptable on positive portions of waveforms. Negative portions, however, should be relatively flat.

B. Volt-ohm Meter Check

( ) Using the test probe shown in Figure 3-3 on Page 111-16, set meter to DC volts and make the following measurements:

(Volt-ohm Meter Check continued on Page 111—16.)

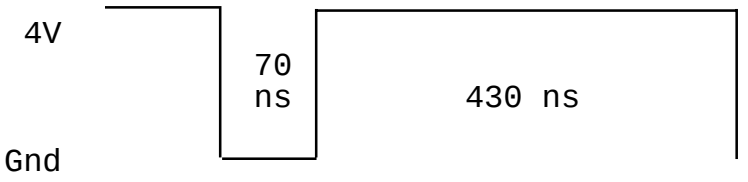
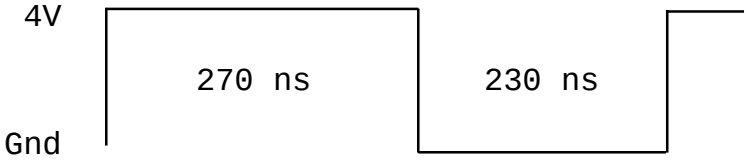
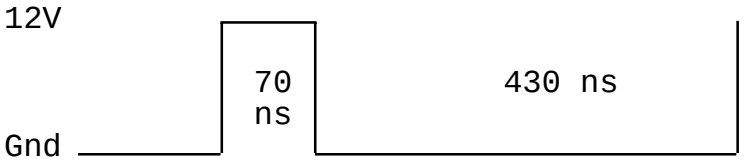
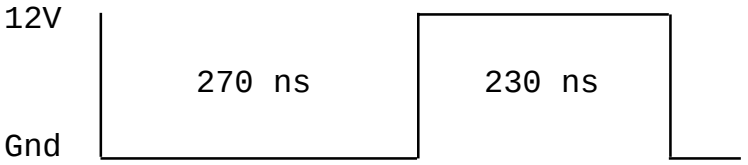
CHECK POINT	SIGNAL	WAVEFORM
( ) U77, Pin 7	Oscillator Output	14.3 MHz square wave. (This is not a perfect square wave. It in fact more resembles a poor sine wave.)
( ) U91, Pin 6	Clock Divider Output	
( ) U91, Pin 11	Clock Divider Output	
( ) U104, Pin 7	CPU Clock Ø1	
( ) U104, Pin5	CPU Clock Ø2	

Figure 3—2. Clock circuit waveforms.

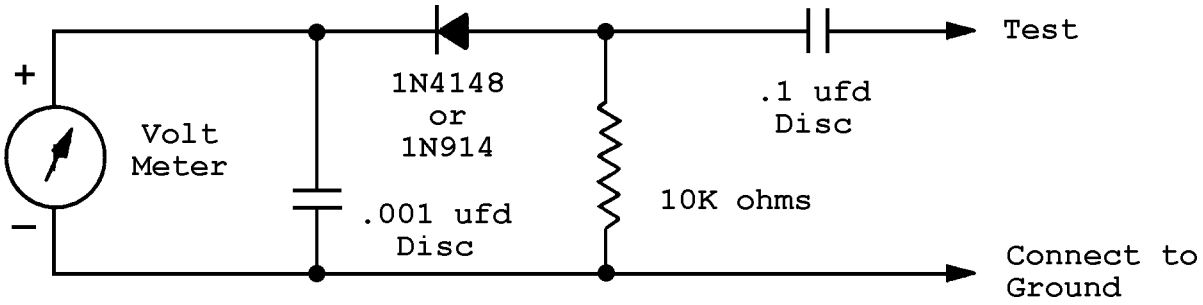


Figure 3-3. Test probe for Steps 16B and 25B.

NOTE 1

The probe shown in Figure 3-3 can be made using parts supplied with your Sol-PC kit. Since these parts will be used later in the Sal-PC assembly, DO NOT shorten the leads or otherwise alter the components. Assemble the probe using tack soldering technique.

NOTE 2

Make sure you have a good ground connection between the meter, probe and Sol—PCB.

( ) At pin 7 of U77 you should measure 1.5 V dc or higher. (A significantly lower reading indicates a faulty oscillator circuit.)

( ) At pin 6 of U91 you should measure 0.25 V dc or higher. (A significantly lower reading indicates a faulty clock divider, U90.)

( ) At pin 11 of U91 you should measure 1.25 V dc or higher. (A significantly lower reading indicates a faulty clock divider, U90.)

( ) At pin 5 of U104 you should measure 4 V dc or higher. (A significantly lower reading indicates a problem with U104.)

( ) At pin 7 of U104 you should measure 8 V dc or higher. (A significantly lower reading indicates a problem with U104.)

( ) If any voltages are incorrect, correct the problem before proceeding; if correct, turn off the power supply and disconnect the power cable.

( ) Step 17. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R1	1.5K	brown-green-red
( )	R2	1.5K	″ ″ ″
( )	R3	1.5K	″ ″ ″
( )	R4	1.5K	″ ″ ″
( )	R5	1.5K	″ ″ ″
( )	R6	1.5K	″ ″ ″
( )	R7	1.5K	″ ″ ″
( )	R8	1.5K	″ ″ ″
( )	R9	1.5K	″ ″ ″
( )	R10	1.5K	″ ″ ″
( )	R11	1.5K	″ ″ ″
( )	R16	1.5K	″ ″ ″
( )	R17	1.5K	″ ″ ″
( )	R19	1.5K	″ ″ ″
( )	R30	1.5K	″ ″ ″
( )	R80*	330, ½ watt	orange-orange-brown
( )	R81	75	violet—green-black
( )	R82	200	red-black-brown
( )	R83	1.5K	brown-green-red
( )	R84	3.3M	orange—orange—green
( )	R85	1.5K	brown-green-red
( )	R86	1.5K	″ ″ ″
( )	R87	330	orange-orange-brown
( )	R88	680	blue-gray-brown
( )	R89	1.5K	brown-green-red
( )	R90	1.5K	″ ″ ″
( )	R96	1.5K	″ ″ ″
( )	R97	1.5K	″ ″ ″
( )	R98	10 K	brown-black-orange
( )	R99	1.5K	brown-green-red
( )	RlOO	10 K	brown-black-orange
( )	RlOl	1.5K	brown-green-red
( )	R102	3.3M	orange-orange-green
( )	R103	1.5K	brown-green—red
( )	R120	100 K	brown-black-yellow
( )	R121	10 K	brown-black-orange
( )	R122	10 K	″ ″ ″
( )	R123	39 K	orange-white-orange
( )	R124	1.5K	brown-green—red
( )	R125	1.5K	″ ″ ″
( )	R126	39 K	orange-white-orange
( )	R127	10 K	brown-b1ack-orange
( )	R128	3.3K	orange—orange-red
( )	R129	10 K	brown-black-orange
( )	VRl & VR2	50 K	Potentiometer

*The leads of R80 and its mounting holes form a snug fit. Take care when installing this resistor.

( ) Step 18. Install the following capacitors in the indicated locations. Take care to observe the proper value and type for each installation. Bend leads outward on solder (back) side of board, solder and trim. (Refer to NOTE in Step 2.)

CAUTION

REFER TO FOOTNOTE AT END OF THIS STEP BEFORE INSTALLING C31.

	LOCATION	VALUE		TYPE
( )	C31*	100	ufd	Aluminum Electrolytic
( )	C32	.1	ufd	Disc
( )	C34	680	pfd	Monolythic or Disc
( )	C35	.1	ufd	Mylar Tubular
( )	C36	.1	ufd	Disc
( )	C37	.1	ufd	Disc
( )	C52	.001	ufd	Mylar Tubular
( )	C53	.01	ufd	Mylar Tubular
( )	C54	.001	ufd	Disc
( )	C55	.001	ufd	Disc
( )	C57	.1	ufd	Disc

*Install C31 with “+” lead at the top.

( ) Step 19. Install Q2 (2N2907 or 2N3460) in its location below and to the right of U88. The emitter lead (closest to tab on can) is oriented toward the left of the board and the base is oriented toward the bottom. Push straight down on transistor until it is stopped by the leads. Solder and trim.

( ) Step 20. Install diodes D9 and DlO (1N4148 or 1N914) in their locations below U88. Position D9 with its dark band (cathode) to the left and DlO with its band to the right.

( ) Step 21. Install coaxial cable, composite video output. (See Figure 3-4 for details on how to prepare cable.)

( ) Strip away about 1¼” of the outer insulation to expose shield. Unbraid shield, gather and twist into a single lead. Then strip away the inner conductor insulation, leaving about ¼” at the shield end.

CAUTION

WHEN PREPARING AND INSTALLING SHIELD, BE SURE BITS OF BRAID DO NOT FALL ONTO BOARD. SUCH DEBRIS CAN CREATE HARD-TO-FIND SHORT CIRCUITS.

( ) Insert inner conductor in mounting hole P1 (left side of board), solder and trim.

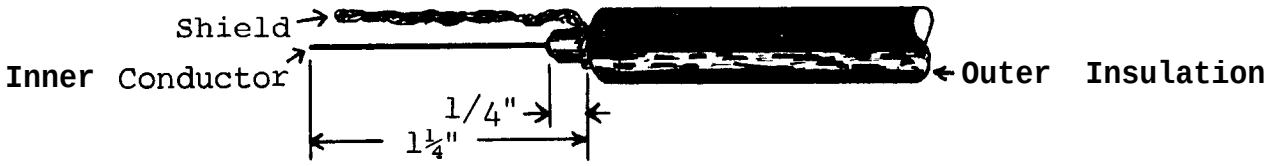


Figure 3-4. Coaxial cable preparation.

( ) Insert twisted shield in mounting hole P2, solder and trim. Using the two large holes to the right of VR1 and VR2, tie cable to board with tie wrap (see CAUTION below).

CAUTION

AFTER INSTALLATION, FINE BITS OF THE BRAID FROM THE SHIELD MAY WORK LOOSE AND FALL ONTO THE BOARD AND CREATE HARD-TO-FIND SHORT CIRCUITS. TO PREVENT THIS, COAT ALL EXPOSED BRAID WITH AN ADHESIVE AFTER SOLDERING AND TIEING. USE AN ADHESIVE SUCH AS SILICONE, CONTACT CEMENT OR FINGERNAIL POLISH. DO NOT USE WATER BASE ADHESIVES.

( ) Step 22. Install 6-position DIP switch in location S1 on left end of board. Position Switch No. 1 at the bottom.

( ) Step 23. Install 20-pin header in location J4 (video sion connector) between U28 and U29. Position header so pin 1 is in the lower right corner. (An arrow on the connector points to pin 1.)

( ) Step 24. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( ) U28	74LS163 or 25LS163
( ) U31	74LS163 or 25LS163
( ) U33	74LS163 or 25LS163
( ) U40	74LS163 or 25LS163
( ) U43	74LS109
( ) U47	74LS10
( ) U49	74LS04

(Step 24 continued on Page 111-20.)

IC NO.	TYPE
( ) U59	74LS20
( ) U60	74LS02 or 9LS02
( ) U62	93L16
( ) U74	74LS86
( ) U75	74LS109
( ) U87	7406
( ) U88*	4049*
( ) U102*	4001*

*MOS device. Refer to CAUTION on Page 111-8.

( ) Step 25. Apply power to Sol-PC and check display section timing chain operation. If you have an oscilloscope, use part A of this step. If you do not, use part B.

A. Oscilloscope Check

( ) Using an oscilloscope, check for the waveforms given in Figure 3-5 at the indicated observation points and in the order given. The waveforms shown in Figure 3-5 approximate actual waveforms. If any waveforms are incorrect, determine and correct the cause before proceeding with assembly.

NOTE

Irregularities up to 1 volt are acceptable on positive portions of waveforms. Negative portions, however, should be relatively flat.

B. Volt-ohm Meter Check

( ) Using the test probe made in Step 16B, measure the voltage at pin 12 of U28. You should measure approximately 1 V dc. If you get a significantly lower reading, find and correct the cause before you proceed with assembly.

( ) Turn off power supply and disconnect power connector.

( ) Step 26. Check synchronization circuits.

( ) Set all S1 switches to OFF.

( ) Connect Sol-PC video output cable to video monitor.

SEE CAUTION ON PAGE III-22 BEFORE CONNECTING MONITOR.

(Step 26 continued on Page 111-22.)

CHECK POINT WAVEFORM

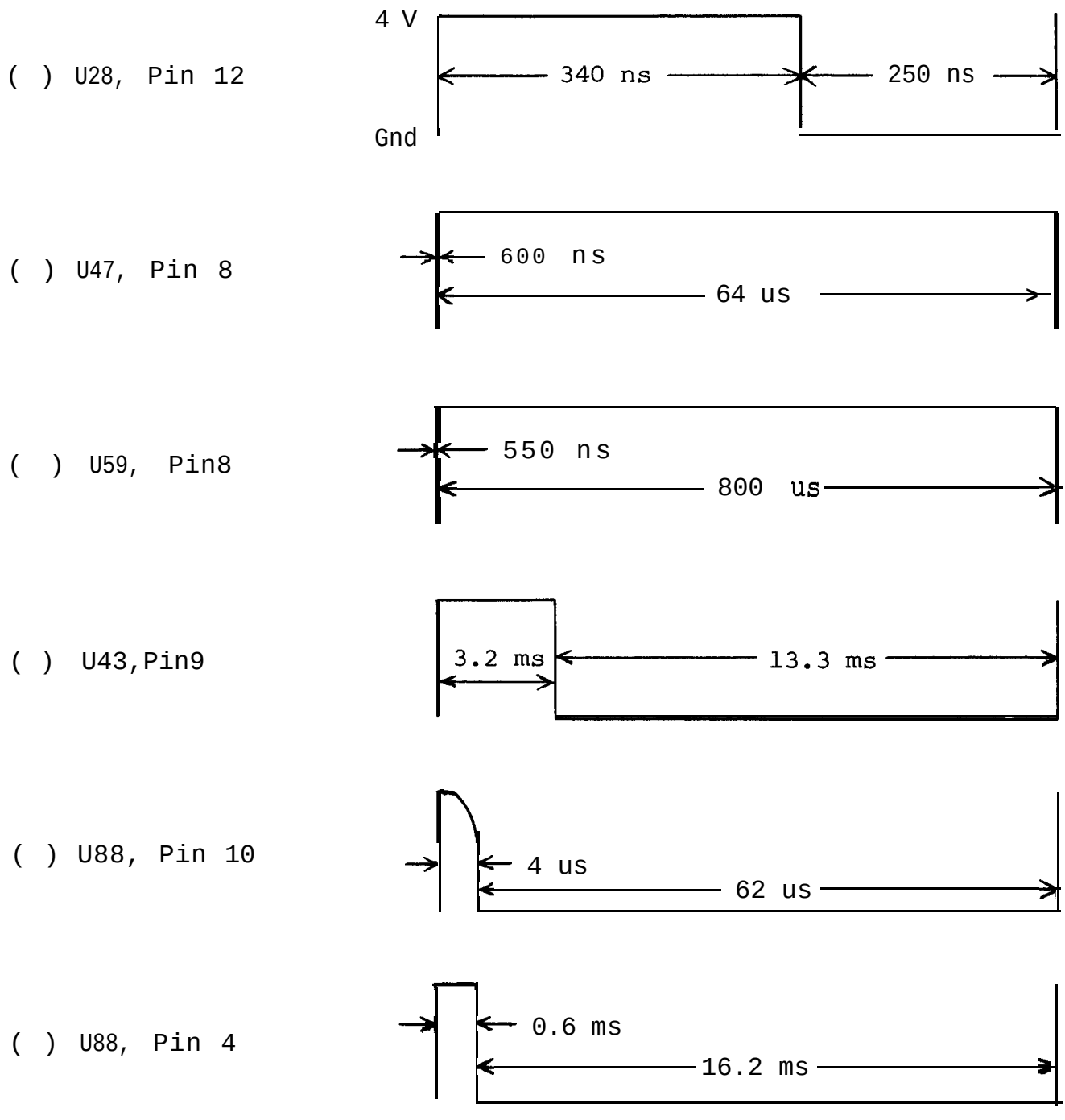


Figure 3-5. Display section timing waveforms.

CAUTION

DO NOT CONNECT THE Sol-PC VIDEO OUTPUT TO A MONITOR OR TV RECEIVER THAT IS NOT EQUIPPED WITH AN ISOLATION TRANSFORMER. (SEE PAGE AVI-7 IN APPENDIX VI.)

( ) Set VR2 (VERT) and VR1 (HORIZ) on the Sol-PC to their mid-range settings. Turn monitor on and apply power to the Sol-PC.

( ) The display raster will be pulled in. Using the monitor Vertical Hold, you should be able to obtain a slow roll (black horizontal bar moves slowly down the screen) and a stationary raster. Using the monitor Horizontal Hold, you should be able to adjust for an out of sync raster (numerous black lines cutting across the raster) and a stable raster. If you cannot obtain these conditions, locate and correct the cause before proceeding.

NOTE

For a stable presentation, a few monitors (especially modified TV sets) may require a higher sync amplitude than that supplied by the Sol-PC. In such cases, increase sync amplitude by reducing the value of R80. DO NOT DECREASE R80 BELOW 225 OHMS.

( ) If the synchronization circuits are operating correctly, turn monitor and power supply off, disconnect the power cable and go on to Step 27.

( ) Step 27. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

(Step 27 continued on Page 111-23.)

IC NO.	TYPE		
( ) U1*	4029*		
( ) U2	74L5175	or	25L5175
( ) U1l*	4029*		
( ) U12	74L5157		
( ) U13	74L5175	or	25L5175
( ) U25*	MCM6574	or	MCM6575*
( ) U26	74L5175	or	25L5175
( ) U27	74L5175	or	25L5175
( ) U29	74L5367		
( ) U30	74L5157		
( ) U32	74LSl57	or	25L5157
( ) U41	74166		
( ) U42	74L5175	or	25L5175
( ) U44	74L500		
( ) U61	74L510		
( ) U89	74L5367		

*MOS device. Refer to CAUTION on Page 111-8.

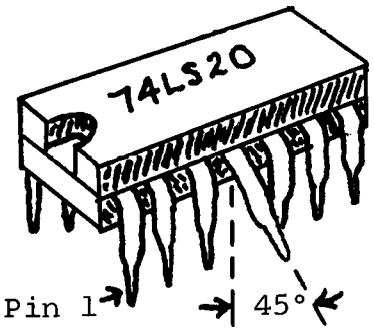
( ) Step 28. Check display circuits.

( ) Set Si switches as follows:

No. 1 through 5: OFF

No. 6: ON

( ) Remove U42 and bend pin 6 out 450 to its normal position. (See Figure 3—6.) Re—install U42 with pin 6 out of the socket.



Bend desired pin out 450 to vertical.

Figure 3-6. Bending selected pins on U42, 59 and 75 (U59 shown).

( ) Remove U59 and bend pin 4 in same manner as U42. Re-install U59 with pin 4 out of the socket.

(Step 28 continued on Page 111—24.)

( ) Remove U75 and bend pin 5 in same manner as U42. Re-install U75 with pin 5 out of the socket.

( ) Using #24 wire, install the following TEMPORARY jumpers in the sockets for U14 through U21. Double check jumpers after installing for correctness. (See Figure 3—7.)

IC SOCKET	JUMPER
( )U14	Pin l2 to 6
( )UlS	Pin 12 to 5
( )1J16	Pin l2 to 4
( )U17	Pin 12 to 8
( )U18	Pin l2 to 2
( )U19	Pin 12 to 7
( )U20	Pin l2 to 1
( )U21	Pin l2 to l6

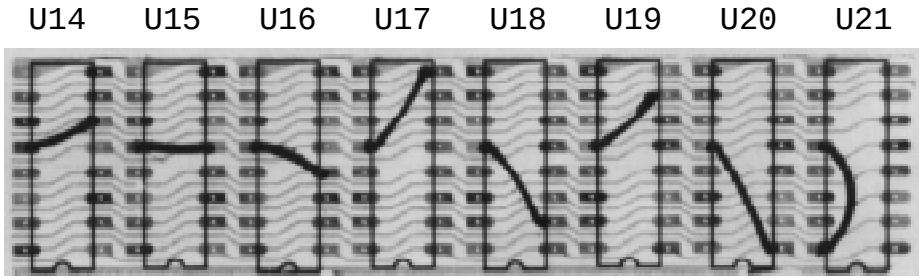


Figure 3-7. U14 through U21 socket jumpers.

( ) Turn monitor on and apply power to Sol-PC.

( ) Momentarily ground pin 1 of U2 and pin 5 of U75. The display shown in Figure 3-8 should appear on the monitor screen.

( ) If the display circuits do not pass this test, determine and correct the cause before proceeding with assembly.

( ) If the display circuits are operating correctly:

  ( ) Turn monitor and power supply off and disconnect the power cable.

  ( ) Remove jumpers from U14 through U21 sockets.

  ( ) Bend pin 6 on U42, pin 4 on U49 and pin 5 on U75 back to their normal position arid re-install these three IC’s in their appropriate sockets.

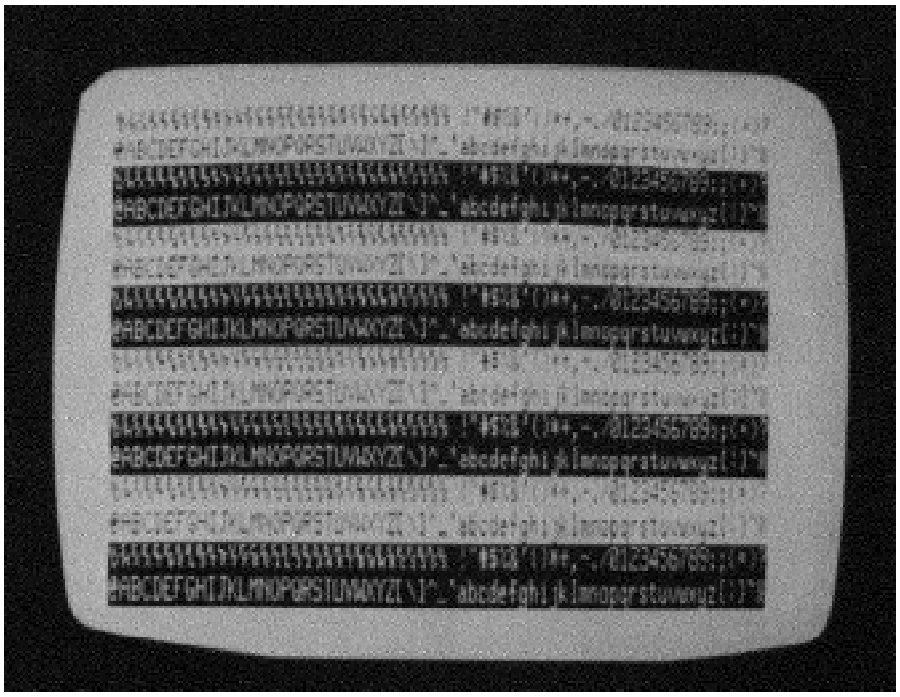


Figure 3-8. Display circuits test pattern with 6575 character generator as U25. 6574 is the same except graphic control characters are displayed.

( ) Step 29. Install 91LO2APC or 21O2L1PC IC's in locations U14 through U21. Dots on the assembly drawing and PC board legend indicate the location of pin 1 of each IC.

CAUTION

IC's U14 THROUGH U21 ARE MOS DEVICES. REFER TO CAUTION ON PAGE 111-8 BEFORE YOU INSTALL THESE IC's.

( ) Step 30. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R12	1.5K	brown-green-red
( )	R18	10 K	brown-black-orange

(Step 30 continued on Page 111—26.)

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R20	1.5K	brown-green-red
( )	R31	1.5K	" " "
( )	R32	1.5K	" " "
( )	R33	1.5K	" " "
( )	R34	1.5K	" " "
( )	R35	1.5K	" " "
( )	R36	1.5K	" " "
( )	R41	1.5K	" " "
( )	R50	1.5K	" " "
( )	R51	1.5K	" " "
( )	R52	1.5K	" " "
( )	R53	1.5K	" " "
( )	R54	1.5K	" " "
( )	R55	1.5K	" " "
( )	R56	1.5K	" " "
( )	R57	1.5K	" " "
( )	R58	330	orange-orange-brown
( )	R107	10 K	brown-black-orange
( )	R108	10 K	
( )	R109	10 K	" " "
( )	R110	10 K	" " "
( )	R111	10 K	" " "
( )	R112	10 K	" " "
( )	R113	10 K	" " "
( )	R114	10 K	" " "
( )	R11S	1.5K	brown-green-red

( ) Step 31. Install diode D7 (1N4148 or 1N914) in its location between U46 and U47. Position D7 with its dark band (cathode) at the bottom.

( ) Step 32. Install 20-pin header in location J3 (keyboard interconnect) between U64 and U65. Position header so pin 1 is in the upper left corner. (An arrow on the connector points to pin 1.)

( ) Step 33. In the jumper area labeled $\overline{\text{PHTM}}$ on the assembly drawing (below U64), install Augat pins in mounting holes F and G. (Refer to "Installing Augat Pins" in Appendix IV.) Using #24 bare wire, install a jumper between pins F and G.

( ) Step 34. In the jumper area labeled RST on the assembly drawing (between U76 and U77), install Augat pins in mounting holes N and P. (Refer to "Installing Augat Pins" in Appendix IV.) Using #24 bare wire, install a jumper between pins N and P.

( ) Step 35. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( ) U45	74LS04
( ) U46	8T380 or 8836
( ) U48	74LS00
( ) U50	74LS367
( ) U54	74LS04
( ) U63	74LS109
( ) U64	74LS109
( ) U67	8T97
( ) U68	8T97
( ) U76	74LS175
( ) U94	74LS367
( ) U107	74LS367

( ) Step 36. Apply power to Sol-PC and make the following voltage measurements:

MEASUREMENT POINT	VOLTAGE*
Pin 11 of U105 Socket	-5 V dc +- .25v
Pin 20 of U105 Socket	+5 V dc +- .25v
Pin 28 of U105 Socket	+12 V dc +- .6 V
Pin 1 of U51 Socket	+5 V dc +- .25V
Pin 2 of U51 Socket	-12 V dc +- .6 V

*All voltages referenced to ground.

( ) If any voltages are incorrect, locate and correct the cause before going on to Step 37.

( ) If voltages are correct, turn power supply off, disconnect power cable and go on to Step 37.

( ) Step 37. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

(Step 37 continued on Page 111-28.)

IC NO.	TYPE
( ) U51*	TMS6011NC*
( ) U105*#	8080,808OA or 9080A*#

*MOS device. Refer to CAUTION on Page 111-8.

#Note that pin 1 of this IC is in the upper left corner-

( ) Step 38. Perform Functional Test No. 1 of CPU circuits.

( ) Set S1 switches as follows:

No. 1 through 5: OFF

No. 6: ON

( ) Turn monitor on and apply power to Sol-PC.

( ) Momentarily ground pin 1 of U2. You should see a full display (64 characters x 16 lines) on the monitor.

( ) Momentarily ground pin 2 of U75. The display should blank while pin 2 of U75 is grounded. When you remove the ground, the display shown in Figure 3-9 on Page III-29 should appear.

NOTE

The pattern shown in Figure 3-9 (delete characters) results from all bits of the DIO Bus being high. If you do not see the delete characters, one or more bits of the DIO bus are low. Consult the MCM6575 or MCM6574 pattern, as appropriate, in Section VIII of this manual to determine which bits are low.

( ) If the test fails, determine and correct the cause before proceeding with assembly.

( ) If the Sol-PC passes this test, turn monitor and power supply off, disconnect power cable and proceed to Step 39.

( ) Step 39. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

(Step 39 continued on Page 111-29.)

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( )U80	8T97#
( )U81	8T97#

#DO NOT substitute.

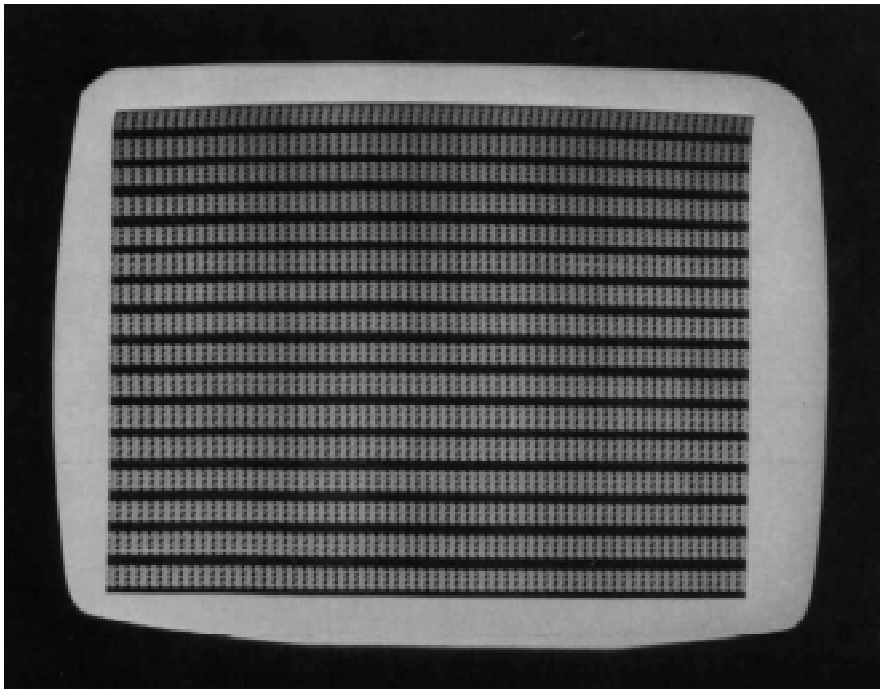


Figure 3-9. CPU Functional Test No. 1 display, 6574 or 6575 character generator (U25)

( ) Step 40. Perform Functional Test No. 2 of CPU circuits.

( )Check that Sl switches are set as specified in Step 38.

( )Turn monitor on and apply power to Sol-PC.

( )Momentarily ground pin 1 of U2 and pin 2 of U75. The display shown in Figure 3-10 on Page 111-31 should appear on the monitor.

( )If the test fails, determine and correct the cause before proceeding with assembly.

( )If the Sol-PC passes this test, turn monitor and power supply off, disconnect power cable and proceed to Step 41.

( ) Step 41. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin l of each IC.

IC NO.	TYPE
( ) U65	74LS253
( ) U66	74LS253
( ) U78	74LS253
( ) U79	74LS253
( ) U93	74LS175
( ) U106	74LS175
( ) U70	74LS109

( ) Step 42. Turn monitor on, apply power to Sol-PC and perform the test described in Step 40, except ground ~in S of U75 instead of pin 2. You should get the same results.

( )If the test fails, determine and correct the cause before proceeding with assembly.

( )If the Sol-PC passes this test, turn monitor and power supply off, disconnect power cable and proceed to Step 43.

( ) Step 43. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

LOCATION	VALUE (ohms)	COLOR CODE
( ) R13	1.5K	brown-green-red
( ) R14	1.5K	" " "
( ) R15	1.5K	" " "
( ) R60	1.5K	" " "

( ) Step 44. Using two 4-40 x 5/8 binder head screws, two #4 insulating washers, two lockwashers and hex nuts, install 30-pin right angle edge connector in location J5. Insert screws from back (solder) side of board and place an insulating washer on each screw on front (component) side of board. Position connector with socket side facing right, place over screws and seat pins in mounting holes. Then place lockwasher on each screw, start nuts and tighten. Solder pins to board.

( ) Step 45. Using four 4-40 x 1/4 binder head screws, lockwashers and hex nuts, install two brackets (Sol-1040) for personality module in area to right of J5. Position brackets over the mounting holes as shown in Figure 3-11. Insert screws from front (component) side of board, place lockwasher on each screw on back (solder) side of board, start nuts and tighten.

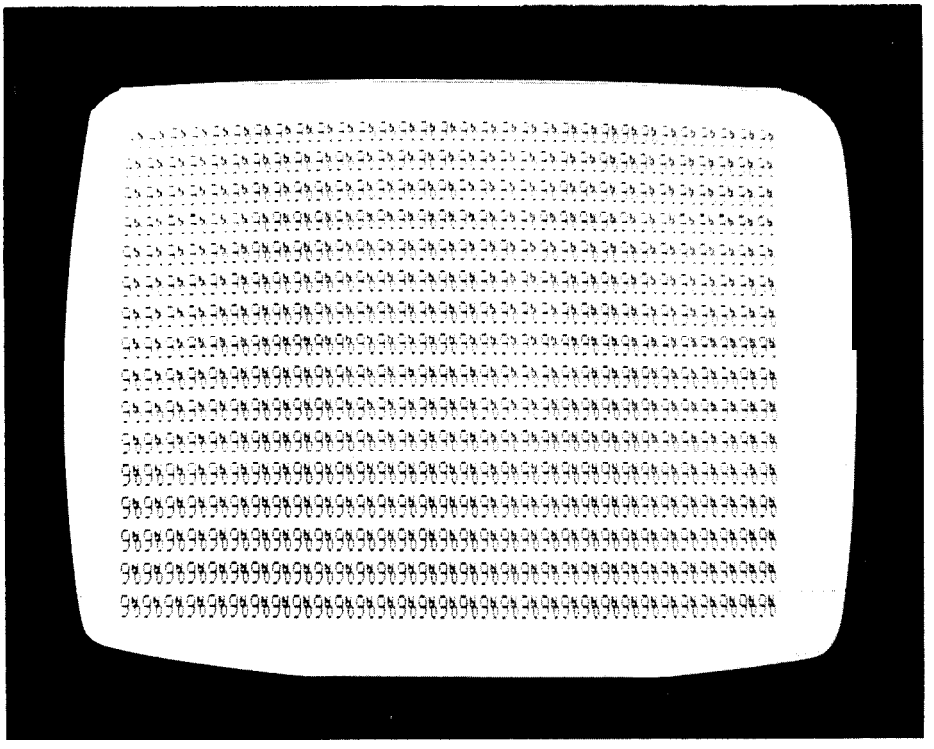


Figure 3-10. CPU Functional Test No. 2 display, 6575 character generator (U25). 6574 displays: 9 □ 9 □ 9 □ etc.

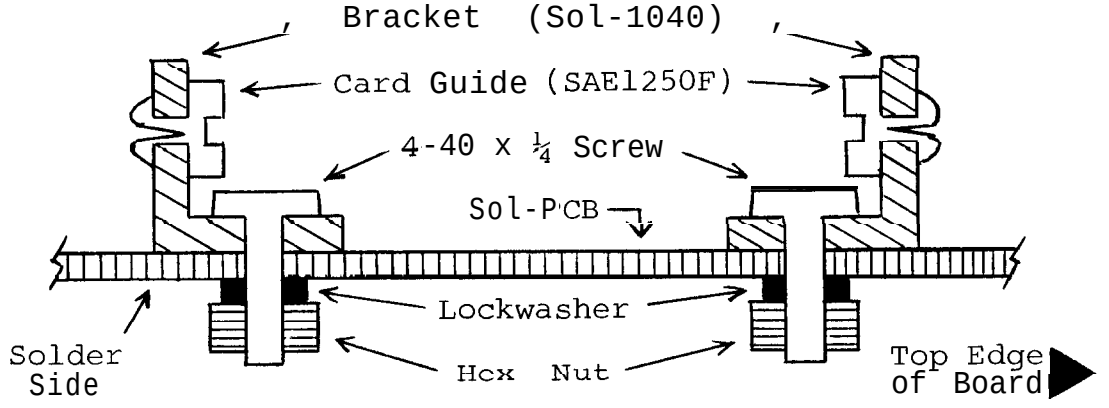


Figure 3-11. Personality module bracket/guide installation (Viewed from right end of Sol-PCB).

( ) Step 46. Attach plastic card guide (SAEl25OF) to each of the brackets installed in Step 45. (See Figure 3-11.) Insert posts on guides into bracket holes and push in until they snap into place.

( ) Step 47. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( ) U3*	91LO2APC or 21O2L1PC*
( ) U4*	91LO2APC or 21O2L1PC*
( ) U5*	91LO2APC or 2102L1PC*
( ) U6*	91LO2APC or 21O2L1PC*
( ) U7*	91LO2APC or 21O2L1PC*
( ) U8*	91LO2APC or 21O2L1PC*
( ) U9*	91LO2APC or 21O2L1PC*
( ) U1O*	91LO2APC or 2102L1PC*
( ) U22	74LS136
( ) U23	74LS20
( ) U24	74LS04
( ) U34	74LS138
( ) U35	74LS138
( ) U36	74LS138
( ) U53	74LS02 or 9LS02
( ) U71	74LS367
( ) U83	74LS20

*MOS device. Refer to CAUTION on Page III-8.

( ) Step 48. Test memory and decoder circuits.

( ) Set Sl switches as specified in Step 38.

( ) Turn monitor on and apply power to Sol-PC.

( ) Ground pin 1 of U2. You should see the same display as shown in Figure 3-10 on Page III—31. In this case, however, there should be a vertical "flickering" movement with an apparent flicker rate of approximately three times per second.

( ) Turn Switch No. 1 of 51 to ON. The flicker should stop.

(Step 48 continued on Page III-33.)

( ) If the test fails, determine and correct the cause before proceeding with assembly.

( ) If the Sol—PC passes this test, turn monitor and power supply off, disconnect power cable, set Switch No. 1 of S1 to OFF and go on to Step 49.

( ) Step 49. Assemble personality module if you have not yet done so. (See Section IV.) If you have, go to Step 9 in Section IV and complete the personality module assembly.

( ) Step 50. Install the following resistors in the indicated locations. Bend leads Co fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

LOCATION	VALUE (ohms)	COLOR CODE
( ) R21	470	yellow—violet-brown
( ) R22	470, ½ watt	" " "
( ) R23	470, ½ watt	" " "
( ) R24	1.5K	brown-green—red
( ) R25	10 K	brown-black-orange
( ) R26	10 K	" " "
( ) R27	470	yellow-violet-brown
( ) R28	10 K	brown—black-orange
( ) R29	10 K	" " "
( ) R37	1.5K	brown-green—red
( ) R38	1.5K	" " "
( ) R39	5.6K	green-blue-red
( ) R40	1.5K	brown-green-red
( ) R42	1.5K	" " "
( ) R43	1.5K	" " "
( ) R44	1.5K	" " "
( ) R45	330	orange-orange-brown
( ) R46	5.6K	green-blue-red
( ) R47	10 K	brown-black-orange
( ) R48	10 K	" " "
( ) R49	1.5K	brown-green-red
( ) R59	1.5K	" " "
( ) R61	1.5K	" " "
( ) R62	5.6K	green-blue-red
( ) R63	5.6K	" " "
( ) R64	330	orange—orange—brown
( ) R65	330	" " "
( ) R66	330	" " "
( ) R67	330	" " "
( ) R68	330	" " "
( ) R69	330	" " "
( ) R70	330	" " "
( ) R71	330	" " "

(Step 50 continued on Page III-34.)

LOCATION	VALUE (obms)	COLOR CODE
( ) R72	680	blue-gray-brown
( ) R73	680	″ ″ ″
( ) R74	680	″ ″ ″
( ) R75	680	″ ″ ″
( ) R76	680	″ ″ ″
( ) R77	680	″ ″ ″
( ) R78	680	″ ″ ″
( ) R79	680	″ ″ ″
( ) R92	5.6K	green—blue—red
( ) R93	1.5K	brown-green-red
( ) R94	10 K	brown-black-orange
( ) R95	15 K	brown-green-orange
( ) R116	1.5K	brown—green—red

( ) Step 51. Install the following capacitors in the indicated locations. Take care to observe the proper value and type for each installation. Bend leads outward on solder (back) side of board, solder and trim. (Refer to NOTE in Step 2.)

LOCATION	VALUE	TYPE
( ) C29	.1 ufd	Disc
( ) C30	330 pfd	Disc

( ) Step 52. Install diodes Dl (1N4148 or 1N914), D2 (1N4001) and D3 through D6 (1N4148 or 1N914) in their locations in the area of U39. Position all diodes with their dark band (cathode) to the right.

( ) Step 53. Install the following DIP switches in the indicated locations. Take care to observe proper orientation.

LOCATION	TYPE	ORIENTATION
( ) S2	8-position	Switch No. 1 at top
( ) S3	8-position	Switch No. 1 at top
( ) S4	6-position	Switch No. 1 at top

( ) Step 54. Install Q1 (2N2907 or 2N3460) in its location between U55 and U56. The emitter lead (closest to tab on can) is oriented toward the bottom and the base lead toward the right. Push straight down on transistor until it is stopped by the leads. Solder and trim.

( ) Step 55. Using two 4-40 x 7/16 binder head screws, hex nuts and lockwashers, install 25—pin female connector in location J1 (serial I/O interface). Position connector with socket side facing right and insert pins into their holes in the circuit board. Insert screws fro~n back (solder) side of board, place lockwasher on each screw, start nuts and tighten. Then solder connector pins to board.

( ) Step 5.6. Using two 4-40 x 7/16 binder head screws1 hex nuts and lockwashers, install 25—pin male connector in location J2 (parallel I/O interface). Install J2 in the same manner as you did Jl.

( ) Step 57. Install Augat pins in mounting holes K, L and M. (Refer to “Installing Augat Pins” in Appendix IV.) These holes are located between u85 and U86. No juniper will be installed.

( ) Step 58. Install the following IC’s in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( ) U37	74L5367
( ) U38*	1489A*
( ) U39#	4N26#
( ) U52	74L5109
( ) U55	74L500
( ) U56	1458CP or 1558CP
( ) U57	7406
( ) U58	8T94
( ) U72	74L5109
( ) U73	74L5109
( ) U84*	4029*
( ) U85*	4046*
( ) U86*	4024*
( ) U95	74173
( ) U96	74173
( ) U97	74175

*MOS device. Refer to CAUTION on Page III-8.

#Solder this IC in its location. See “Loading

DIP Devices” in Appendix IV.

( ) Step 59. Check input/output (I/O) circuits.

NOTE

The parallel I/O interface should be tested with the device you will be using. Refer to “I/O Interfacing” in Section VII.

(Step 59 continued on Page III-36.)

To check the serial I/O circuits, proceed as follows:

( ) Set S1 as in previous test,
Set S2 switches all OFF,
Set S3 switches all OFF, except S3-1 ON,
Set S4 switches all OFF

( ) Set all S4 switches to OFF.

( ) Connect Sol—PC video output cable to monitor, turn monitor on and apply power to Sol-PC.

( ) Set Sol-PC to local by depressing LOCAL key on keyboard to turn keyboard indicator light on.

( ) Data entered from the keyboard should appear on the monitor.

( ) If the Sol—PC fails this test, locate and correct the cause before proceeding.

( ) If the Sol-PC passes this test, turn monitor and power supply off, disconnect power cable and video output cable and go on to Step 60.

( ) Step 60. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

LOCATION	VALUE (ohms)	COLOR CODE
( ) R117	10 K	brow-n-black-orange
( ) Rll8	10 K	" " "
( ) R119	10 K	" " "
( ) R139	l.0M	brown—black-green
( ) R140	10 K	brown-black-orange
( ) R141	150 K	brown-green-yellow
( ) R142	10 K	brown-black-orange
( ) R143	1 M	brown-black-green
( ) R144	47 K	yellow-violet-orange
( ) R145	10 K	brown-black-orange
( ) R146	10 K	" " "
( ) R147	2.2M	red-red-green
( ) R148	100 K	brown-black-yellow
( ) R149	100	brown-black-brown
( ) R150	470	yellow—violet—brown
( ) R151	5.6K	green-blue—red
( ) R152	150 K	brown—green—yellow
( ) R153	100 K	brown-black-yellow
( ) R154	100 K	" " "
( ) R155	6.8, ½ watt	blue-grey-gold
( ) R156	6.8, ½ watt	blue-grey-gold
( ) VR3	50 K	Potentiometer

( ) Step 61. Install the following capacitors in the indicated locations. Take care to observe the proper value and type for each installation. Bend leads outward on solder (back) side of board, solder and trim. (Refer to NOTE in Step 2.)

CAUTION

REFER TO FOOTNOTE AT END OF THIS STEP BEFORE INSTALLING C67.

	LOCATION	VALUE (ufd)	TYPE
( )	C47	.001	Disc
( )	C48	.047	"
( )	C49	.001	"
( )	C50	.01	Mylar TQbular
( )	C51	.1	Disc
( )	C66	.1	"
( )	C67*	1	Tantalum
( )	C68	.1	Disc
( )	C69	.1	"
( )	C70	.1	"
( )	C71	.001	"
( )	C72	.001	Mylar Tubular
( )	C73	.047	Disc
( )	C74	470 pfd	

*Install C67 with "+" lead at top right.

( ) Step 62. Install miniature phone jacks in locations J6 and J7 located to the right of UlOl. Position J6 and J7 with jack facing right, insert pins in mounting holes and solder.

( ) Step 63. Install subminiature phone jacks in locations J8 and J9 in lower right corner of board. Install J8 and J9 as you did J6 and J7.

( ) Step 64. Install Q3 (2N4360) in its location to the left of C67. Install Q3 with its flat "side" at the bottom. Push straight down on transistor until it is stopped by the leads, solder and trim.

CAUTION

THE 2N4360 IS STATIC SENSITIVE. REFER TO CAUTION ON PAGE III-8.

( ) Step 65. Install Q4 and Q5 (2N2222) in their locations above and to the left of U108. For both transistors, the emitter lead (closest to tab on can) is oriented toward the left and the base lead toward the right. Push straight down on transistor until it is stopped by the leads, solder and trim.

( ) Step 66. Install diodes Dl3 and Dl4 (lN400l) in their locations in the lower right corner of the board. Position both diodes with their dark band (cathode) at the bottom.

( ) Step 67. Install DIP reed relays in locations K1 and K2 to the right of U113. Be sure to install Kl and K2 with their end notch at the bottom)pin 1 in lower right corner). These relays are soldered to the board. (Refer to “Loading DIP Devices” in Appendix IV.)

( ) Step 68. Install the following IC’s in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

IC NO.	TYPE
( ) U69*	TMS6011NC*
( ) U98*	4023*
( ) U99*	4030*
( ) U100*	4013*
( ) U10l*	4027*
( ) U10S	1458CP or 1558CP
( ) U109*	4049*
( ) U110*	4046*
( ) U111*	4019*
( ) U112*	4520*
( ) U113*	4013*

*MOS device. Refer to CAUTION on Page III-8.

( ) Step 69. Install Augat pins in mounting holes H, I and J (located to left of C70). (Refer to “Installing Augat Pins” in Appendix IV.) Using #24 bare wire, install a jumper between pins I and J.

( ) Step 70. Adjust VR3.

( ) Using a cable with a male phono jack on both ends, connect ACI audio output (J6) to ACI audio input (J7).

( ) Apply power to Sol-PC.

( ) Set VR3 fully clockwise (CW).

( ) Measure the DC voltage at pin 13 of U11O and write the measured voltage down. (Call this Voltage A.)

( ) Set VR3 fully counterclockwise (CCW).

(step 70 continued on Page III—39.)

( ) Measure the DC voltage at pin 13 of UllO and write the measured voltage down. (Call this Voltage B.)

( ) Add Voltages A and B and divide the sum by 2. (Call the result Voltage C.) An example follows:

Voltage A (VR3 full CW):	3.45 V dc
Voltage B (VR3 full CCW):	1.80 V dc
A + B =	5.25 V dc

Voltage C = 5.25 V dc / 2 = 2.63 V dc

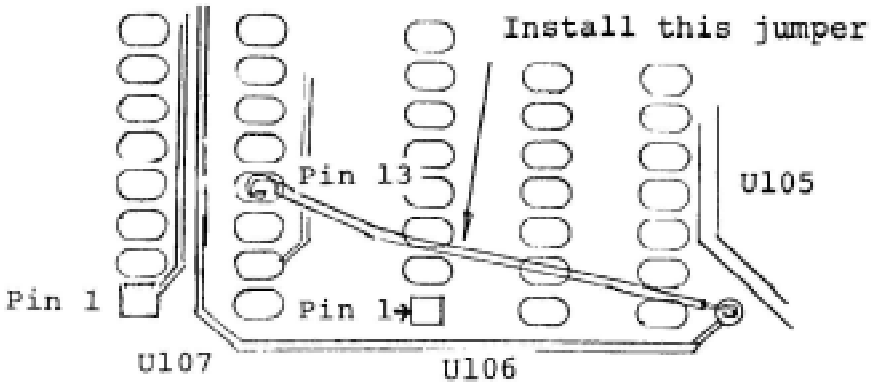
( ) Adjust VR3 so that the voltage at pin 13 of UllO equals Voltage C. (In the preceding example this would be 2.63 V dc.)

( ) Step 71. If your recorder has only a microphone input, remove the I-to-J jumper you installed in Step 69 and install a jumper (#24 bare wire is recommended) between the I and H pins.

Otherwise, leave the I—to—J jumper in and go on to Step 72.

( ) Step 72. Install 100-pin edge connector, Jll. Using two 4-40 x 7/16 binder head screws, install 100-pin edge connector in location Jil (center of PC board). Seat the pins in the mounting holes. Then thread screws from front (component) side of board into the threaded inserts that are pre-installed in the Jll mounting holes. Tighten screws and solder pins to board.

( ) Step 73. Look on the rear of the board, on the component side, where the Personality Module plugs in, for a mark “Rev E”. If your board is marked this way, complete this step, otherwise ignore this step. Connect a jumper of #24 a.w.g. insulated wire between pin 13 of U107 and the feed—through pad adjacent to pin 21 of U105. Solder, check for solder bridges, and trim excess wire strands if needed. The installed jumper is shown below.



Solder side of board shown

3.6.4 Modification for 625 Line Video

The European televisions standard defines a raster of 625 lines at a field rate of 50 Hz. The horizontal rate of the U.S. standard, 15,750 Hz., is maintained. Only the number of scan lines on the screen is increased.

The Video Display Generator section may be modified f or the 50 Hz. standard by following the additional steps below. The effect of the modification is to increase the modulus of the counter U62 to eight during VDISP. This results in four extra character lines (52 scan lines) between the bottom and top of the display area, for a total of 312 scan lines per field and 624 scan lines per frame.

The field rate should be close enough to 50 Hz. to reduce any swim effects to less than 0.1 Hz. Some difficulty may be encountered in obtaining centering of the display within the frame. This is because the stand-off time to VSYNC from the bottom of the display is unchanged from the 60 Hz. standard. If objectionable, increase the value of resistor Rl00 which is in series with the VPOS control.

To convert for 50 Hz., perform these additional steps:

( ) Locate U62 on the component side legend. Find pin 5 of this IC on the component (front) side of the board. Cut the “V”-shaped trace connecting pin 5 to the near-by pad designated “AF”, using a sharp exacto blade or scribe, so that there is no continuity between these pads.

( ) Bend a small piece of bare wire, such as a resistor clipping, into a loop to form a jumper between pad “AF”, and the adjacent pad “AG”. Insert the jumper, pull close to the board, solder, and trim the leads.

If this modification is made, change the schematic, X-18, to show that pin 5 of U62 now connects to pin 4 (ground), instead of pin 6 as shown.

Processor Technology

*** NOTICE TO ALL Sol-PC OWNERS ***

The "Parts List" (Table 3-1 on Pages III-2, 3 & 4 in this manual) includes components for the Sol-ACI Audio Cassette Interface section of the Sol-PC Single Board Terminal Computer™ as well as sockets (Sol-SS IC Socket Kit) for the IC's used in the unit.

If you did not order sockets with your original purchase, ignore Step 1 of the Sol-PC Assembly and Test instructions (Section III in this manual); if you did not order the ACI option, ignore Steps 58 through 66. Also delete the following items as appropriate from Table 3-1:

INTEGRATED CIRCUITS

1 1458CP or 1558CP (U108)
1 TMS6011NC (U69)
2 4013 (U100,113)
1 4019 (U111)
1 4023 (U98)
1 4027 (U101)
1 4030 (U99)
1 4046 (U110)
1 4049 (U109)
1 4520 (U112)

RESISTORS

1 100 ohm, ¼ watt, 5%
1 470 ohm, ¼ watt, 5%
1 5.6K ohm, ¼ watt, 5%
7 10K ohm, ¼ watt, 5%
1 47K ohm, ¼ watt, 5%
1 50K ohm, Potentiometer
3 100K ohm, ¼ watt, 5%
2 150K ohm, ¼ watt, 5%
1 1M ohm, ½ watt, 5%
1 2.2 ohm, ¼ watt, 5%

CONNECTORS

2 Miniature Phone Jack (J6,7)
2 Subminiature Phone Jack (J8,9)

TRANSISTORS

1 2N4360 (Q3)
2 2N2222 (Q4,5)

DIODES

2 1N4001 (D13,14)

RELAYS

2 DIP Reed, Sigma 191-TE1A15S (K1,2)

CAPACITORS

3 .001 ufd disc
1 .001 ufd Mylar Tubular
1 .01 ufd Mylar Tubular
3 .047 ufd disc
5 .1 ufd disc
1 1 ufd, tant dip

MISCELLANEOUS

4 8-pin DIP Socket
29 14-pin DIP Socket
74 16-pin DIP Socket
1 24-pin DIP Socket
3 40-pin DIP Socket

Both the Sol-ACI and Sol-SS are available from Processor Technology at the following prices*: (The Sol-SS IC socket kit is highly recommended for kit construction.)

Sol-SS IC Socket Kit	$40
Sol-ACI Audio Cassette Interface	$55

*Prices are net and subject to change without notice.

PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080
CABLE ADDRESS "PROCTEC"

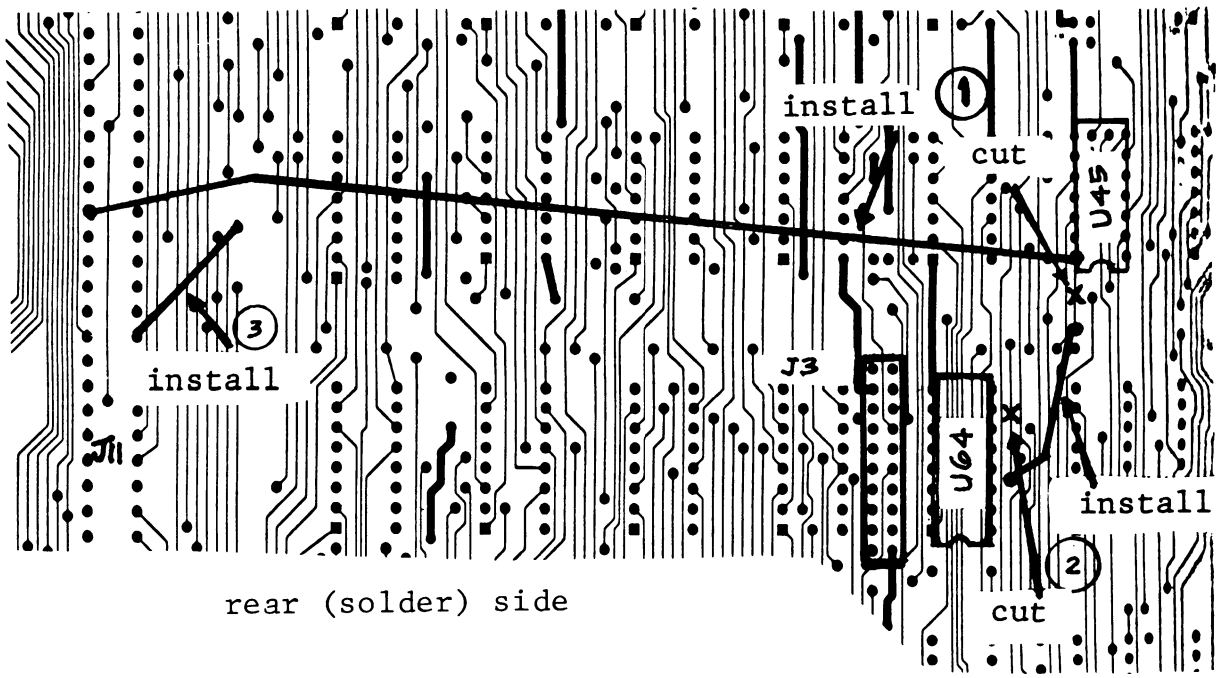
SOL - PC MODIFICATION REVISION LEVEL D

Due to layout errors connections to pins 28, 73 and 74 have been interchanged. These signals are used by DMA and interrupt devices. Correction requires three cuts and installation of three jumpers. Use 24 gauge wire supplied with the kit for these changes.

1. Cut trace on rear side of board connecting pin 1 of U45 with feedthrough directly below. Install jumper wire on rear side of board connecting pin 1 of U45 with pin 73 of J11.

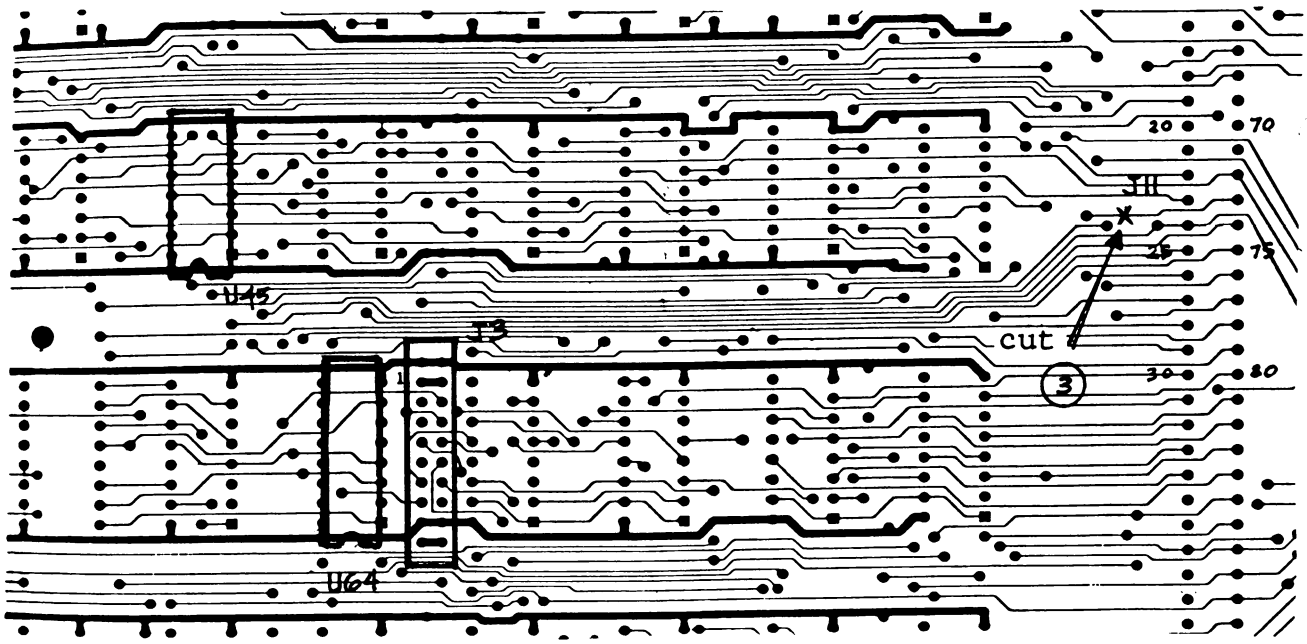
2. Cut trace connecting the feedthrough adjacent to pins 13 and 14 of U64 with the feedthrough directly above (on rear side of board). Install jumper wire as shown on the rear side of the board.

3. Cut trace on front side of the board connecting the feedthrough immediately below and to the left of the "J11" designation with pin 73 of J11. Install a jumper wire from this feedthrough to pin 28 of J11 on the rear side of the board.



rear (solder) side

front (component) side



SECTION IV

ASSEMBLY
and
TEST

Sol PERSONALITY MODULE

Processor Technology

IV PERSONALITY MODULE ASSEMBLY

4.1 Parts and Components IV-1

4.2 Assembly Tips IV-1

4.3 Assembly Precautions IV-1

4.4 Required Tools, Equipment and Materials . . IV-1

4.5 Orientation IV-1

4.6 Assembly-Test IV-2

4.6.1 Circuit Board Check IV-2
4.6.2 Assembly-Test Procedure IV-2

4.1 PARTS AND COMPONENTS

When ordering your Sol, you selected one of two types of Personality Modules: CONSOL Or SOLOS. The outer carton of your kit is stamped with the Personality Module type. Both use the same PC board marked 2708, assembly #107000, and differ only in the type of ROM's and their programming. (An alternative PC board marked 5204 and designed for type 5204 EPROM's is also available but not supplied with this kit. Schematic diagram X—4 and assembly drawing X20 refer to this alternative board.) Check all parts against Table 4-1 below. If you have difficulty identifying any parts, refer to Figure 3-1 on page 111-5.
One of two kits, using the same PC board: 2708-0 or 2708-1 may be supplied. The 2708-0 version uses one 9216 masked ROM which has no window on top of the IC package. The 2708-1 version uses two 2708 EPROM's which have windows.

Table 4-1. PM2708 Personality Module Parts List.

1	PM2708 PC Board	1 or 4*	l-ufd Capacitor, Tantalum Dipped
1 or 2*	9216 ROM or 2708 EPROM's with Personality program	1 or 2*	24-pin DIP Socket
1	74LS08	1	14-pin DIP Socket
0 or 2*	1.N523]B Zener Diode	1	Handle Bracket (Sol—1045)
3 or 4*	10K ohm, ¼ watt, 5% Res.	2	2—56X1/8 Binder Head Screw
0 or 2*	100 ohm, ½ watt, 5% Res.		
1	.047-ufd Disc Ceramic		

* These are the quantities of parts used in the 2708—1 version.

4.2 ASSEMBLY TIPS

For the most part the assembly tips given in Paragraph 3.2 of Section III (Page III-1) apply to assembling the personality module.

4.3 ASSEMBLY PRECAUTIONS

For the most part the assembly precautions given in Paragraph 3.3 in Section III (Page III—6) apply.

4.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the personality module.

1. Needle nose pliers
2. Diagonal cutters
3. Screwdriver
4. Soldering iron, 25 watt
5. 60—40 rosin—core solder (supplied)
6. Small amount of #24 solid wire

4.5 ORIENTATION

Capacitor location C2 will be located in the upper left hand corner of the board when the edge connector is positioned at the

left end of the board. In this position the component (front) side of the board is facing up. Subsequent position references related to the personality module circuit board assume this orientation.

4 . 6 ASSEMBLY—TEST

4.6.1 Circuit Board Check

( ) Visually check circuit board for broken traces, shorts (solder bridges) between traces and similar defects.

( ) Check circuit board to insure that the +5—volt bus, +12 volt bus and -12-volt bus are not shorted to each other or to ground. Using an ohmmenter, make the following measurements (refer to personality module assembly drawing in Scction X)

( ) +5 volt Bus Test. On Ul, measure between pin 12, (ground) and pin 24 (+5 volts). There should be no continuity.

( ) -5 volt Bus Test. On Ul and U2, measure between pin 12 (ground) and pin 21 (-5 volts) . Thcrc should be no continuity.

( ) +12 volt Bus Test. Also on Ul, measure between pin 12 (ground) and the bottom edge connector pin on the component side of the board marked Al.

( ) Inter—bus Test. On Ul, measure between pins 12 and 21, then between edge connector pin Al and pins 21, then 12. There should be no continuity in any of these measurements.

If visual inspection reveals any defect, or you measure continuity in any of the preceding tests, return the board to Processor Technology for replacement. If the board is not defective, proceed to next paragraph.

4.6.2 Assembly-Test Procedure

Refer to personality module assembly drawing X-6.

CAUTION

THE MEMORY IC’S USED ON THE PERSONALITY MODULE ARE MOS DEVICES. THEY CAN BE
(CAUTION continued on Page IV-3)

DAMAGED BY SIATIC ELECTRICITY DISCHARGE. HANDLE THESE IC's SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON, RATHER THAN SYNTHETIC, CLOTHING WHEN HANDLING MOS IC's. (STATIC DISCHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY CONDITIONS.)

( ) Step 1. Install DIP sockets. Install each socket in the indicated location with its end notch oriented as shown on the circuit board and assembly drawing. Take care not to create solder bridges between the pins and/or traces.

INSTALLATION TIP

Insert socket pins into mounting pads of appropriate Location. On back (solder) side of hoard, bend pins at opposite corners of socket (e.g. pins 1 and 9 on a 16—pin socket) outward until they are at a 45 angIe to the board surface. This secures the socket until it is soldered. Repeat this procedure with each socket until all are secured to the board. Then solder the pins on all sockets.

LOCATION	TYPE SOCKET
( ) U1	24 pin
( ) U2*	24 pin*
( ) U3	14 pin

*Used on 2708— 1 vers ion only.

( ) Step 2. Install the following resistors in the indicated locations. Instal I these resistors parallel with the board. Bend leads by using needle nose pliers to grip the resistor lead right next to tlie resistor body, and bend the portion of the lead on the other side of the pliers with your finger. The bend must he the right distance from the resistor body for the resister to Fit easily into its two holes. Insert the leads into the two holes, and from the opposite side of the hoard poll the leads to bring the resistor body down to touch the hoard, head the leads outward on the solder (back) side of the board so the resistors do not slip out of position.

LOCATION	VALUE	COLOR CODE
( ) R1*	100 ohms	brown—black—brown
( ) R2*	100 ohms	brown-black-brown
( ) R3	10K	brown-black-orange
( ) R4*	10K	brown-black-orange
( ) R5	10K	brown-black-orange
( ) R6	10K	brown—black—orange

*not used on 2708-0 version

( ) Step 3. Install 1N5231B Zener Diodes in locations Z1, and Z2 if you have the 2708-1 version. Form the leads as in Step 2. Insert the diodes so that the white band on the diode is in the position indicated by the legend. Bend the leads outward to retain the diodes, then solder and trim the leads.

( ) Step 4. Install the following capacitors in the indicated locations. Take care to observe the proper value, type and orientation for each installation. On the dipped tantalum capacitors, the “+” lead is the one which is closest to the “+” marking on the body of the capacitor. Insert this lead in the hole marked “+” on the PC board legend. After inserting C5, remove it from the board before soldering to clear wax from the leads and holes. After inserting all capacitors, pull them close to the board and bend the leads outward to secure them. Solder and trim all leads.

LOCATION	VALUE (ufd)	TYPE
( ) C1*	1	Dipped Tantalum
( ) C2	1	Dipped Tantalum
( ) C3*	1	Dipped Tantalum
( ) C4*	1	Dipped Tantalum
( ) C5	.047	Disc Ceramic

*not used on 2708—0 version

( ) Step 5. Check for +5, ±12, and -12 volt bus—to-ground shorts. Using an ohmmeter on OHMS times 1K or OHMS times 10K scale, make the following measurements. A typical reading is 1 Megohm. A reading less than 10K indicates a short.

( ) Measure between edge connector pins A2 and A15.

( ) Measure between edge connector pins A14 and A15.

( ) Measure between edge connector pins Al and A15.

( ) If any measurement indicates a short, find and correct the problem before proceeding.

Rev C ( ) Step 6. Using two 2-56 x 1/8" binder head screws, install

handle bracket (Sol-lO 45) . Position bracket on front (component) side of board at the right end as shown in Figure 4-2. Align bracket holes with mounting holes in board, insert screws from back (solder) side of board and drive into bracket. No nuts are needed since the bracket holes are tapped.

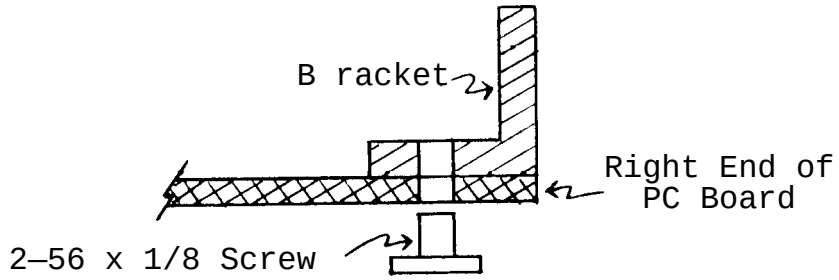


Figure 4-2. Handle bracket (Sol-1045) installation.

( ) Step 7. If you have a 2708-0 version with the 9216 ROM (windowless) , omit this step. If you have the 2708-1 version, find the area above the Ul socket where the legend reads “-5V 21 CO 19 +12V.” This legend designates five PC pads in a row directly underneath. On the back (solder) side of the board, there is a small trace which connects the “CO” and “21” pad. Cut this trace with a sharp knife or scribe point so there is no longer continuity between these pads. Form the clipping from a resistor lead, or other small bare wire into a loop and insert this jumper between the “-5V” pad and the “21” pad. Solder and trim the leads. Next find the two pads between C2 and R6, with legend “-16” under the right pad of the pair. On the back (solder) side of the board, cut the trace which connects these pads.

( ) Step 8. Stop assembly at this point and proceed with Sol-PC assembly and test up through Step 48. (See Section III.) Then go on to Step 9 of this procedure.

( ) Step 9. Plug personality module into J5 on Sol-PC, apply power to Sol—PC and make the following voltage measurements on the personality module, with respect to chassis ground:

MEASUREMENT POINT	VOLTAGE
Pin 24 of Ul, U2	+5 V dc ± 5%
Pin 14 of U3	+5 V dc ± 5%
Pin 21*of Ul, U2	-5 V dc ± 5%
Pin 12 of Ul, U2	Ground
Pin 7 of U3	Ground

*For 2708-1 version only

( ) Measure between edge connector pin B14 and pin B15. You should measure more than 1M ohms. A reading less than 10K ohms indicates a short.

( ) If any voltages are incorrect, locate and correct the cause before proceeding to Step 10.

( ) If the voltages are correct, turn power off, disconnect power cable, unplug personality module and go on to Step 10.

( ) Step 10. Install IC's in the sockets numbered Ul through U3. Make sure the dot or notch indicating pin 1 on the IC package is in the correct position as indicated on the PC board component legend and the assembly drawing X-6. Socket U2 is left empty on 2708—0 versions (9216 ROM with no window). As shown in the table, the 2708 EPROM's have paper labels with the designation shown, while 9216 ROM's have the designation printed on the IC package itself.

			IC LABEL	
	IC NO.	TYPE	CONSOL	SOLOS
	( ) U1*	2708	C	S4
2708—0	( ) U2*	2708	Empty	S5
version	( ) U3	74LS08	--	--
	( ) U1*	9216		SOLOS
2708—1	( ) U2	Empty	--	--
version	( ) U3	74LS08	--	--

*MOS devices. See CAUTION on pages IV-2, 3.

( ) Step 11. Plug personality module into J5 on Sol-PC and connect Sol-PC video output cable to video monitor. (Refer to CAUTION on Page III-22 in Section III.)

( ) Set S1 switches as follows:

No. 1 through 4: OFF

No. 5: ON

No. 6: OFF

( ) Turn monitor on and apply power to Sol-PC

( ) With both the CONSOL and SOLOS modules, you should see the cursor, preceded by a prompt character, like this: ⟩

( ) If you do not see a cursor, locate and correct the problem before proceeding.

( ) If a blinking cursor is present, the ENter and DUmp commands should operate as described in Section IX of this manual.

( ) If the ENter and Dump commands do not operate correctly, locate and correct the problem before proceeding.

( ) If the personality module is operating correctly, turn monitor and power off, disconnect power cable and video output cable and go on to Step 50 in Section III. (The personality module can be left plugged in.)

SECTION V

Sol KEYBOARD

Sol TERMINAL COMPUTER™

V KEYBOARD ASSEMBLY and TEST

5.1 Parts and Components V-1

5.2 Assembly Tips V-1

5.3 Assembly Precautions V-1

5.4 Required Tools, Equipment and Materials . . V-1

5.5 Orientation V-1

5.6 Assembly-Test V-3

5.6.1 Circuit Board Check V-3
5.6.2 Assembly-Test Procedure V-3

5.1 PARTS AND COMPONENTS

Check all parts and components against the “Parts List”, Table 5-1. If you have difficulty in identifying any parts by sight, refer to Figure 3—1 on Page Ill—S in Section III of this manual.

5.2 ASSEMBLY TIPS

For the most part the assembly tips given in Paragraph 3.2 of Section III (Page III—1) apply to assembling the Sol keyboard.

In addition, be sure your hands are clean before handling the circuit board, especially the area containing the keyboard switch pads.

5.3 ASSEMBLY PRECAUTIONS

For the most part the assembly precautions given in Paragraph 3.3 in Section III (Page III-6) apply to assembling the Sol keyboard.

5.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the personality module:

1. Needle nose pliers
2. Diagonal cutters
3. Screwdriver (thin blade)
4. Controlled heat soldering iron, 25 watt
5. 60—40 rosin—core solder (supplied)

5.5 ORIENTATION

Light emitting diode location LED3 will be located in the lower left—hand corner of the board when locations JI and U4 through U16 are at the top of the board. In thin position the component (front) side of the board is facing up and all horizontal reading legends will read from left to right. Subseqeent position references related to the keyboard circuit board assume this orientation.

Table 5—I. Sol Keyboard Parts List.

INTEGRATED CIRCUITS

1	555 (U3)	1	74LS30 (U25)
1	2101 or 9101 (U20)	2	7442 (U17 & 21)
2	4051A (U19 & 22)	5	74LS74 (U8,9,ll,l5,26)
4	74LS00 (U4,10,14,16)	2	7493 (U6,U5)
1	74LS04 (U23)	1	74LSI32 (U7)
1	7406 (U24)	2	74LS175 (Ul,U2)
2	74LS10 (U13 & 27)	1	8334, 9334 or 83L34 (U12)
		1	8574, 74S287, or 82S129 (U18)

TRANSISTORS	DIODES (ZENER)	DIODES (LIGHT EMITTING)
6 2N3640	1 1N5221B (D1)	3 MV5752 (LED1,2,3)
3 2144274		

RESISTORS			CAPACITORS		
1	10	ohm, ¼ watt, 5%	2	220	pfd, disc
3	150	ohm, ¼ watt, 5%	1	470	pfd, disc
1	390	ohm, ¼ watt, 5%	1	.0022	ufd, disc
1	680	ohm, ¼ watt, 5%	2	.01	ufd, disc
7	1 K	ohm, ¼ watt, 5%	5	.047	ufd, disc
10	1.5K	ohm, ¼ watt, 5%	1	.1	ufd, Mylar tubular
1	2.2K	ohm, ¼ watt, 5%	2	15	ufd, tantalum dipped
5	3 K	ohm, ¼ watt, 5%			
2	33 K	ohm, ¼ watt, 5%			
2	68 K	ohm, ¼ watt, 5%			
2	2.2K	ohm resistor network			
2	33 K	ohm resistor network			

Table 5-1. Sol Keyboard Parts List (Continued).

MISCELLANEOUS	
1	Sol-KBD Printed Circuit Board
1	8—pin DIP Socket
17	14—pin DIP Socket
8	16—pin DIP Socket
1	22—pin DIP Socket
1	20—pin Header, 3M3492—2002
1	9-3/4" 20-conductor Rainbow Cable Assembly
1	70-key (Sol-lO) or 85-key (Sol-2O) Keyboard Assembly
1	Plastic Insert (Sol—lO) for Key Pad
18	Torx Screw (Similar to #4 by 3/8" sheet metal screws.)
3	Fiber Spacer
1	Length Solder

5.6 ASSEMBLY-TEST

5.6.1 Circuit Board Check

( ) Visually inspect circuit board for obvious flaws. (The design of the board includes numerous unconnected traces and traces that are shorted to each other.)

( ) Check circuit board to insure that the +5—volt bus is not shorted to ground. Using an ohmmeter, measure between the GND and +5V pads located in the upper left corner of the board. There should be no continuity.

If no visual inspection reveals any defect, or you measure continuity between the GND and +5v pads, return the board to Processor Technology for replacement. If the board is not defective, proceed to next paragraph.

5.6.2 Assembly-Test Procedure

Refer to keyboard assembly drawing X-7.

CAUTION

SOME MOS INTEGRATED CIRCUITS ARE USED ON THE Sol KEYBOARD. THEY CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGE. HANDLE MOS IC's SO THAT NO DISCHARGE FLOWS THROUGH TEE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON, RATHER THAN SYNTHETIC, CLOTHING WHEN YOU DO HANDLE MOS IC's. (STATIC CHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY CONDITIONS.)

( ) Step 1. Install DIP sockets. Install each socket in the indicated location with its end notch oriented as shown on the circuit board and assembly drawing. Take care not to create solder bridges betwean the pins and/or traces. (Refer to "Installation Tip" on Page 111—9 in Section III.)

	LOCATION	TYPE SOCKET
( )	U1 and 2	16 pin
( )	U3	8 Pin
( )	U4 through U11	14 pin
( )	U12	16 pin
( )	U13 through U16	14 pin
( )	U17 through U19	16 pin
( )	U20	22 pin
( )	U21 and 22	l6 pin
( )	U23 through U27	14 pin

( ) Step 2. Install the following Capacitors in the indicated locations. Take care. to observe the proper value, type and orientation (if applicable) for each installation. Insert leads, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

NOTE

Disc capacitor leads em usnally coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacItor and clear the holes of any wax. Reinsert and install.

LOCATION	VALUE	TYPE	ORIENTATION
( ) C1	15 ufd	Tantalum	"+" lead top
( ) C2	.047 ufd	Disc	None
( ) C3	.1 ufd	Mylar:	"

(Continued on Page V-5.

LOCATION		VALUE		TYPE	ORIENTATION
( )	C4	.01	ufd	Disc	None
( )	C5	.047	ufd	"	"
( )	C6	.047	ufd	"	"
( )	C7	.0022	ufd	"	"
( )	C8	470	pfd	"	"
( )	C9	220	pfd	"	"
( )	C10	220	pfd	"	"
( )	C11	.01	ufd	"	"
( )	C12	.047	ufd	"	"
( )	C13	.047	ufd	"	"
( )	C14	15	ufd	Tantalum	"+" lead top

( ) Step 3. Install the following resistors in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, solder and trim.

LOCATION		VALUE (ohms)	COLOR CODE
( )	R1	150	brown-green-brown
( )	R2	150	" " "
( )	R3	150	" " "
( )	R4	68 K	blue-gray-orange
( )	R5	560 K	green-blue-yellow
( )	R6	33 K	orange—orange—orange
( )	R7	1 K	brown-black-red
( )	R8	1.5K	brown-green-red
( )	R9	3 K	orange-black—red
( )	Rl0	3 K	" " "
( )	R11	3 K	" " "
( )	R12	3 K	" " "
( )	R13	1.5K	brown-green-red
( )	R14	1.5K	" " "
( )	R15	1.5K	" " "
( )	R16	1 K	brown-black-red
( )	R17	390	orange-white-brown
( )	R18	1 K	brown-black-red
( )	R19	10	brown-black-black
( )	R20	1 K	brown-black-red
( )	R21	1 K	" " "
( )	R22	3 K	orange-black-red
( )	R23	1 K	brown-black-red
( )	R24	1 K	" " "
( )	R25	1.5K	brown-green—red
( )	R26	680	blue-gray-brown
( )	R27	33 K	orange—orange-orange
( )	R28	1.5K	brown-green—red
( )	R29	1.5K	" " "

(Continued on Page V-6.)

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R30	1.5K	brown—green—red
( )	R31	1.5K	" " "
( )	R32	68 K	blue-gray-orange
( )	R33	1.5K	brown—green-red
( )	R34	2.2K	red-red-red

( ) Step 4. Install Zener diode D1 (1N5221B) in its location to the left of R17. Position Dl with its dark band (cathode) at the bottom.

( ) Step 5. Install Q1, Q2 and Q9 (2N4274) and Q3 through Q8 (2N3640) in their respective locations at the top center of the board. The emitter lead (closest to flat side of case) is oriented toward the right of the board and the base is oriented toward the top. Insert leads until transistor is approximately 3/16" above surface of circuit board, solder and trim.

( ) Step 6. Install resistor networks RX1 and RX3 (2.2K ohms) and RX2 and RX4 (33K ohms) in their respective locations just above the keyboard pads. Install each network so that the dot on its package is positioned next to the foil square on the circuit board. Recheck values before soldering.

CAUTION

THESE RESISTOR NETWORKS ARE DELICATE.
HANDLE WITH CARE.

( ) Step 7. Install light emitting diodes LED1, 2 and 3 (MV5752) in their respective locations in the lower left corner of the circuit board. Insert leads through fiber spacer, position each diode with its cathode lead (longer lead and/or the lead next to flat edge of LED package) at the bottom, insert leads into mounting holes in circuit board, pull down so that spacer and LED are snug to board, solder and trim. (If fiber spacers are not supplied with your kit, install LED's so they are approximately 3/16" above surface of circuit board.)

( ) Step 8. Install 20-pin header in location J1 (upper left corner of board). Position header so pin 1 is in the lower left corner. (An arrow on the header points to pin 1.) Solder.

( ) Step 9. Using an ohmmeter, measure between GND and +5V pads in upper left corner of the board. You should measure some resistance. Zero resistance indicates a short. If re—qu.ired, find and correct the problem before proceeding to Step 10.

( ) Step 10. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin I of each IC.

	IC NO.	TYPE
( )	U1	74LS175
( )	U2	74LS175
( )	U3	555
( )	U4	74LS00
( )	U5	7493
( )	U6	7493
( )	U7	74LS132
( )	U8	74LS74
( )	U9	74LS74
( )	U10	74LS00
( )	U11	74LS74
( )	U12	8334,9334 or 83L34
( )	U13	74LS10
( )	U14	74LS00
( )	U15	74LS74
( )	U16	74LS00
( )	U17	7442
( )	U18	8574, 74S287, or 82S129
( )	U19*	4051A*
( )	U20*	2101 or 9101*
( )	U21	7442
( )	U22*	4051A*
( )	U23	74LS04
( )	U24	7406
( )	U25	74LS30
( )	U26	74LS74
( )	U27	74LS10

*MOS device. Refer to CAUTION on Page V-4.

( ) Step 11. Connect 20-conductor ribbon cable between J1 on keyboard to J3 on Sol—PC so that cable goes left from J3.

( ) Step 12. Check keyboard operation.

( ) Set S1 switches on Sol-PC as follows:

No. 1 through 4: OFF

No. 5: ON

No. 6: OFF

( ) Connect TV monitor to Sol-PC.

( ) With personality module installed, apply power to Sol-PC.

( ) Using a CLEAN finger, touch key pad #62 (MODE SELECT).

( ) You should get a carriage return and line feed and see a greater than" sign (>) on the screen above the cursor.

NOTE

You may have to touch pad #62 several times to obtain the specified display.

( ) If you are unable to obtain the specified display, locate and correct the problem before proceeding.

( ) if the keyboard is operating correctly, turn monitor and Sol-PC power off, disconnect 20—conductor ribbon cable at Jl on the keyboard and go on to Step 13.

( ) Step 13. Place keyboard assembly carefully over key pads on PC board. Be sure the three LED's fit in the holes in the sheet metal. Carefully align holes in PC board, 18 in all, with threaded mounting holes on bottom of keyboard assembly. Insert Torx screws from solder (back) side of board and, using a thin-blade screwdriver, drive into keyboard assembly mounbing holes. Drive screws evenly and tighten just enough to hold keyboard assembly in place.

CAUTION: DO NOT OVERTIGHTEN THESE SCREWS

( ) Step 14. Reconnect 20-conductor ribbon cable to Jl on key-board.

( ) Step 15. Test keyboard for proper operation.

( ) Apply power to monitor and Sol-PC.

( ) Strike MOdE SELECT key.

( ) Strike UPPER CASE key. Indicator light should come on.

( ) Strike UPPER CASE key again. Indicator light should go off.

( ) Strike LOCAL key. Indicator light should come on.

( ) Strike LOCAL key again. Indicator light should go off.

(Step 15 continued.)

( ) Strike SHIFT LOCK key. Indicator light should come on.

( ) Strike either SHIFT key. Indicator light should go off.

( ) Verity operation of all alphanumeric keys. (As you strike each key you should observe the corresponding character on the monitor.)

( ) Should the keyboard fail any of the preceding checks, locate and correct the problem before proceeding.

( ) If the keyboard passes all of the preceding tests, congratulations on a job well done.

At this point you have successfully assembled the Sol keyboard and tested it for proper operation. It is now ready for use with the Sol—PC Single Board Terminal Computer™

Having completed the Sol keyboard, power supply, Sol-PC and personality module, you are now ready to assemble the Sol cabinet—chassis. Cabinet—chassis assembly instructions are provided in Section VI.

SECTION VI

Sol CABINET-CHASSIS

Sol TERMINAL COMPUTER™

VI CABINET-CHASSIS ASSEMBLY

6.1 Introduction VI-1

6.2 Parts and Components VI-1

6.3 Assembly Tips VI-1

6.3.1 General VI-1
6.3.2 Electrical VI-1
6.3.3 Mechanical VI-5

6.4 Required Tools, Equipment and Materials . . VI-6

6.5 Orientation VI-6

6.5.1 Sol Backplane Board, Sol-BPB VI-6
6.5.2 Sol Cabinet-Chassis VI-6

6.6 Assembly-Test VI-7

6.6.1 Backplane Board (Sol-BPB) Assembly . VI-7

6.6.2 Wooden-Masonitr Parts VI-8

6.6.3 Sol Assembly VI-10

6.1 INTRODUCTION

This section covers assembly of the Sol—10 and Sol—20 chassis and cabinet. The instructions contained herein assume that you have already assembled the power supply and Sol-PC Single Board terminal ComputerTM... including the personality module and the Sol keyboard (Sol-KBD).

6.2 PARTS AND COMPONENTS

Check all parts and components against the appropriate "Parts List(s)", Table 6-1 and 6-2. If you have any difficulty in identifying any parts by sight, refer to Figures 6-1 and 6—2 on Pages VI-4 and VI-4.

6.3 ASSEMBLY TIPS

6.3.1 General

1. Scan Section VI in its entirety before you start to assemble your Sol cabinet—chassis.

2. IT IS IMPORTANT that you follow the step-by-step instructions in the order given when assembling the Sol cabinet—chassis if your assembly is to be done correctly and with minimum effort.

3. Assembly steps and component installations are preceded by a set of parentheses. Chock off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

4. Should you encounter any problem during assembly, call on us for help if needed.

6.3.2 Electrical

1. Use a low—wattage soldering iron, 25 watts maximum, for all soldering.

2. Solder neatly and as quickly as possible.

3. Use only 60—40 rosin—core solder. NEVER use acid—core solder or externally applied fluxes.

4. DO NOT press the tip of the soldering iron on pads or traces when installing components and/or attaching leads to a PC board. To do so can cause the pad or trace to "lift" off the board and permanently damage it.

Table 6-1. Sol—10 Cabinet—Chassis Parts List.

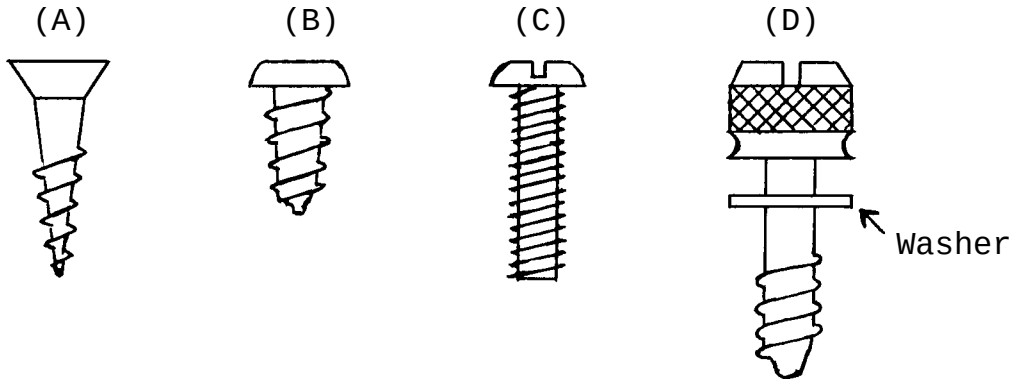
CHASSIS and SUBCHASSIS	HARDWARE
1 Main Chassis	4 4-40 x 3/16 Screw, Machine
1 Expansion Chassis	16 4-40 x 5/16 Screw1 Machine
1 Power Supply Subchassis	8 4-40 Hex Nut
1 Fan Closure Plate	22 #4 Lockwasher, Internal Tooth
BRACKETS	16 6-32 x ½ Screw1 Machine
	8 6-32 Hex Nut
1 Power Supply Subchassis Bracket	16 #6 Lockwasher, Internal Tooth
	11 8—32 x ½ Screw, Machine
2 Keyboard Bracket	2 8-32 x 1 Screw, Machine
3 8—32 Hex Nut	3 #8 Lockwasher, Internal Tooth
CABINET	2 10-24 Thumb Screw
1 Left Side Piece, Walnut	21 #6 x ¼ Screw, Sheet Metal
1 Left Side Piece, Masonite	4 #6 x 5/16 Screw, Sheet Metal
1 Right Side Piece, Walnut	12 5/8 Screw, Wood
1 Right Side Piece, Masonite	2 #4 Solder Lug
1 Keyboard Cover	10 Tinnerman Plastic Inserts, Tapped
1 Top Cover	2 ¼” Spacer, 4—40 Tapped
	4 Self-stick Protective Pads
MISCELLANEOUS	
2 Finger Well Label, Black *	
1 Printed Trim Plate, Paper	
1 Plexiglass Strip	
1 Serial Number Label	
1 Connector Identification Label	

* May be packaged under the plexiglass strip.

Table 6—2. Sol-20 Cabinet-Chassis Parts List.

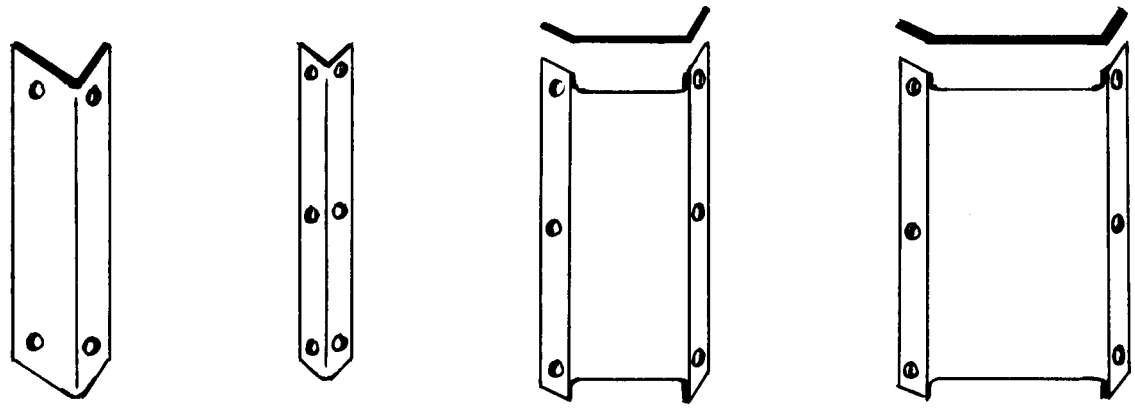
The Sol-20 Cabinet—Chassis Kit includes all Sol—10 parts listed in Table 6—1 plus the following items:

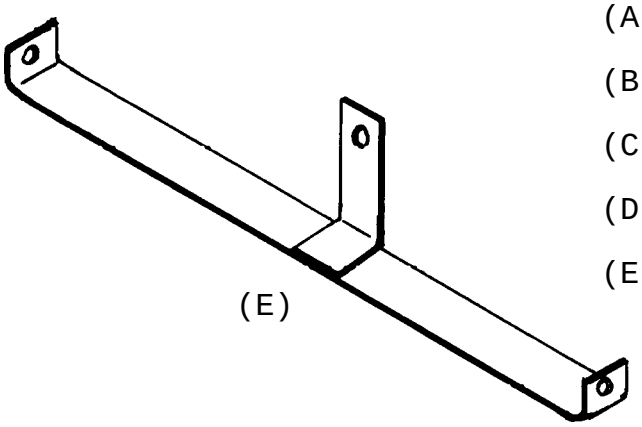
1	Sol—BPB Circuit Board (Backplane Board)
1	3" 5-wire Cable with Molex Connector
1	100-pin Edge Connector, VIKING 3KH50/90V5
5	100—pin Edge Connector, other brand
2	Right Angle Backplane Bracket
1	Gusset Bracket, Left
1	Gusset Bracket, Right
10	Plastic Card Guide
6	4—40 x 5/16 Screw, Machine
6	4-40 x 5/8 Screw, Machine
12	4-40 Hex Nut
12	#4 Lockwasher, Internal Tooth
8	6—32 x ½ Screw, Machine
8	6—32 Hex Nut
9	#6 Lockwasher, Internal Tooth
12	#6 x ¼ Screw, Sheet Metal



(A) Flat Head Wood Screw
(B) Sheet Metal Screw
(C) Binder or Pan Head Screw
(D) Thumb Screw

Figure 6—1. Types of screws used in Sol cabinet—chassis assembly.





(A) Keyboard Bracket
(B) Backplane Bracket, Right Angle
(C) Gusset Bracket, Left
(D) Gusset Bracket, Right
(E) Power Supply Subchassis Bracket

Figure 6—2. Brackets used in Sol cabinet—chassis assembly.

6.3.2 Electrical (continued)

5. (Sol-20 only.) The Backplane PC board (Sol-BPB) has plated-through holes. Solder flow through to the component side of the board can produce solder bridges (shorts). Check for such bridges after you install each component or wire.

6. (Sol-20 only.) The Backplane PC board (Sol-BPB) has an integral solder mask (a lacquer coating) that shields selected areas on the board. This mask minimizes the chances of creating solder bridges during assembly.

6.3.3 Mechanical

1. If you do not have the proper screwdrivers (see Paragraph 6.5), we recommend that you buy them rather than using a knife point, a blade screwdriver on a Phillips screw, and other makeshift means. Proper screwdrivers minimize the chances of stripping threads, disfiguring screw heads and marring decorative surfaces.

2. To assure a correct fit and tight assembly, be sure you use the screws specified in the instructions.

3. Lockwashers are widely used in the Sal cabinet—chassis assembly so that screws will not loosen when subjected to stress or vibration. Then a lockwasher is specified, do not omit it and make sure you install it correctly.

4. Some instructions call for prethreading holes. This is done to make assembly easier by giving you maximum working space for installing relatively hard—to—drive sheet metal screws. If you bypass prethreading instructions you will only make your cabinet—chassis assembly more difficult.

To prethread a hole, insert specified screw in the hole and position it as straight as possible. While holding the screw in this position, drive it into the metal with the proper screwdriver. If started straight the screw will continue to go straight into the metal so that the head and sheet metal surfaces are in full contact.

5. The diameter of the shank (threaded portion) of a screw increases in relation to its number. For example, a 6—32 screw is larger in diameter than a 4—40 screw. Also, a #8 lockwasher is larger than a #4 lockwasher.

6.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the Sol cabinet—chassis. (Unless indicated otherwise, none of the following items are supplied with your kit.)

1. Needle nose pliers
2. Diagonal cutters
3. Screwdriver, thin ¼" blade
4. Screwdriver, #2 Phillips
5. Controlled heat soldering iron, 25 watt
6. 60-40 rosin-core solder (supplied)
7. Silicon grit abrasive paper, 220 & 400 grit
8. Boiled linseed oil
9. Turpentine or mineral spirits
10. Masking tape
11. Transparent tape
12. Rubber mallet or small hammer

6.5 ORIENTATION

6.5.1 Sol Backplane Board, Sol—BPB (Sol—20 Only)

The PC board identification (Sol-BPB) and revision level will be located in the upper left-hand corner of the board when the edge connector (gold contacts) is positioned at the bottom of the board. In this posiCion, the component (front) side of the board is facing up. Subsequent position references related to the Sol-BPB assume this orientation.

6.5.2 Sol Cabinet—chassis

Unless specified otherwise, all position references (e.g., left, right, front, back, bottom and top) in the cabinet—chassis assembly instructions assume the Sol cabinet is viewed from the front (keyboard) when it is sitting in its normal position (key-board up).

6.6 ASSEMBLY-TEST

NOTE

Instructions that apply only to the Sol-20 are preceded by an asterisk. Skip these instructions if you are assembling a Sol—10.

*6.6.1 Backplane Board (Sol-BPB) Assembly

Refer to assembly drawing, page X-11.

*( ) Step 1. Visually inspect Sol-BPB PC board for obvious flaws such as solder bridges (shorts) between traces, broken traces and similar defects.

If visual inspection reveals any defects, return the board to Processor Technology for replacement. If the board passes inspection, go on to Step 2.

*( ) Step 2. Install VIKING 3KH50/9VC5 100-pin edge connector on top edge of PC board. (This edge has silver (not gold) con tacts.)

NOTE

This connector is supplied as a trouble-shooting aid. It is not critical to normal operation of the Sol—20.

Position connector on PC board so that its #1 trace is aligned with the #1 trace on the board, and push connector fully onto board. Bend the connector pins slightly so that both rows of pins are in light contact with the traces on the board. DO NOT CLOSE CONNECTOR PINS SO MUCH THAT YOU WILL DAMAGE THE TRACES WHEN PLACING THE CONNECTOR OVER THE EDGE OF THE BOARD. While holding the connector and board together, place board solder side down on a book, or other flat surface that is higher than your work surface, so the connector extends fully over the edge. That is, the connector should not rest on the book. Reposition connector if needed to align the pins and traces. On the component (front) side of board, solder a pair of traces. On the component (front) side of board, solder a pair of pins at each end of the connector to their respective traces on the

(Step 2 continued on Page VI-8.)

board. Then solder the remaining 46 pins on the component side to traces.

The connector must be perpendicular to the edge of the board. If it is not, bend the pins you just soldered to obtain the required alignment. Then solder the other 50 pins to the traces.

*( ) Step 3. Install the other five 100-pin edge connectors. Position connector on front side of board and insert pins. On solder (back) side of board, solder pins at opposite corners of the connector to hold it in place. Then solder remaining 98 pins. (Refer to Paragraph 6.6.1 on Page VI-6 for definition of front side of board.)

*( ) Step 4. Connect 3" 5—wire cable to circuit board to uppermost pads in top right corner: Insert wires from solder (back) side of board and solder on component (front) side side of board. If a wire is too large for the mounting hole, snip off as many individual strands as needed to obtain a fit. Connect cable leads as follows:

CABLE LEAD	PAD
White	Ground (fifth hole from right)
White	Ground (fourth hole from right)
Blue	+8 V dc (third hole from right)
Red-White	+16 V dc (second hole from right)
Yellow-White	-16 V dc (first hole from right)

NOTE

Pad orientations given above are as viewed from component (front) side of circuit board.

*( ) Step 5. Fill all exposed (not covered with lacquer) fee-through holes on right-hand side of board with solder.

The backplane board is now assembled. Set it to one side for later installation in the cabinet—chassis.

6.6.2 Wooden-masonite Parts

Refer to assembly drawinys, pages X8 and X9.

( ) Step 6. Finish walnut side panels.

The sides of the Sol cabinet are solid black walnut which have been sanded to a smooth surface. If there should be any blemishes, remove them with 220 grit abrasive paper. SAND WITH THE GRAIN.. .NEVER ACROSS TIlE GRAIN.

We recommend an oil finish be applied to the walnut since such a finish lies “in” the wood, not on “top” of it. Also, no wax is necessary with an oil finish.

You may obtain a good finish by using a half-and-half mixture of boiled linseed oil and turpentine. Apply mixture with rag, soaking all surfaces. (End grain may require more oil than face grain.) Let stand for one—half hour, recoating any dry spots, and wipe dry with a clean cloth. Repeat as often as needed to obtain a lustrous finish. (It may take several days.)

You may also use a commercially available penetrating oil such as Watco Danish Oil or Tung Oil. Follow directions on the container if you use such an oil. For a more durable finish when using a penetrating oil:

1. Sand between applications with 220 grit silicon carbide abrasive paper. (Wipe clean after 15 minutes to avoid build-up.)

2. Repeat the following day using 400 grit paper between applications.

3. Repeat as often as desired, using a still finer grit paper between applications. DO NOT sand after final application, but wipe the surfaces clean and let dry for one day. Then coat with previously mentioned linseed oil-turpentine mixture and wipe dry.

( ) Step 7. Using a black broad tipped felt pen, darken all edges of the two masonite parts.

( ) Step 8. Mate the left walnut and masonite side pieces. (Refer to assembly drawing on page X-8.)

NOTE

When the walnut and masonite side pieces are correctly mated, the countersink side of the six countersunk (funnel—shaped enlargement) holes in the masonite will be next to the main chassis.

Insert five Tinnerman plastic inserts in the holes indicated on Drawing X-8. Insert these from the side that mates with the walnut. These inserts may be seated by gently tapping them with a hammer until fully seated.

( ) Step 9. Insert remaining five Tinnerman inserts in right masonite side piece as you did the left side piece. (Refer to Drawing on page X-9.

( ) Step 10. Attach left masonite side piece to left walnut side piece with six 5/8" flat head wood screws. Drive these screws through the countersunk holes in the masonite into the walnut. (Refer to Drawing No. X-8.)

NOTE

Lead holes have been predrilled in the walnut to make driving these screws easier.

( ) Step 11. Attach right masonite side piece to right walnut side piece as you did the left side pieces. (Refer to Drawing No X-9.)

( ) Step 12. Set both side piece assemblies to one side.

6.6.3 Sol Assembly

Refer to Drawing No. X-10 in Section X. Figure 6-3 and 6-4 show complete Sol assemblies without covers.

( ) Step 13. Mount keyboard support bracket (heavy gauge right angle brackets) to each side of the main chassis as shown in Drawing No. X-10 . These are mounted with the narrower side of the bracket at the top.

Attach each bracket to main chassis with two 6-32 x ½ binder or pan head screws and #6 lockwashers. Place lockwasher on screw, insert screw from outer surface of main chassis side wall and drive into the threaded bracket mounting holes.

( ) Step 14. Attach power supply subchassis bracket (short leg “T” shaped bracket) to top front of power supply subchassis as shown in Drawing No. X-10. (Note that leg of “T” is closer to side wall of subchassis. This leg is for mounting a “power on” indicator light—not supplied.) Insert #6 x ¼ sheet metal screw from right side of side wall and drive into bracket.

( ) Step 15. To gain access to the rear area of the power supply subchassis side wall, remove the #6 x ¼ sheet metal screw that attaches the fan closure plate to the subchassis. You should not have to disconnect the transformer (black wires) or AC receptacle ground (green wire) leads since they have sufficient slack to permit moving the closure plate out of the way. (Set screw to one side for use in re—installing the fan closure plate.)

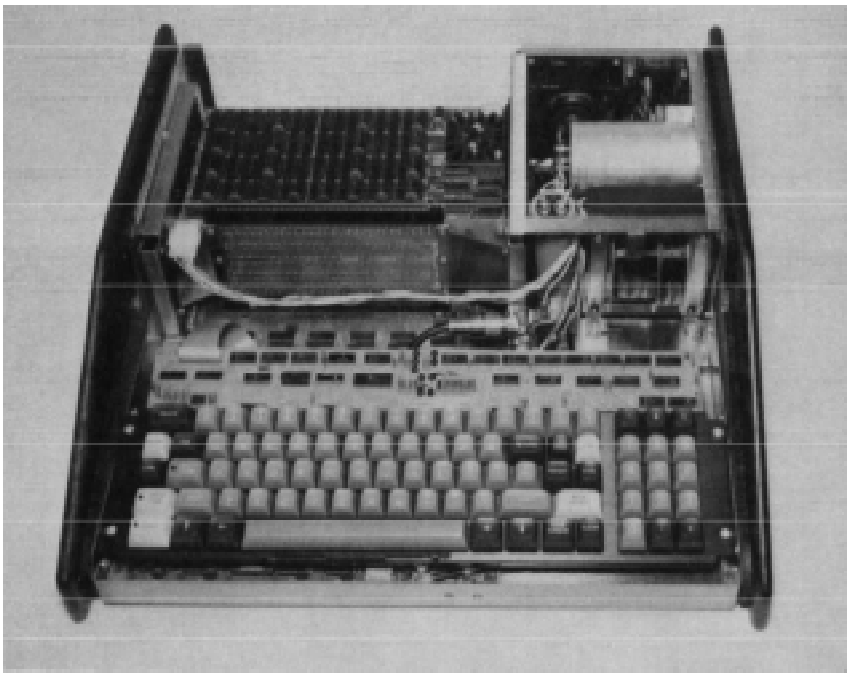


Figure 6-3. Sol-20 with covers removed. Front (or keyboard) is in foreground, power supply is in right rear corner, expansion chassis (with 8KRA Memory installed) is to left of power supply. The vertical board just behind white connector on left is the backplane board.

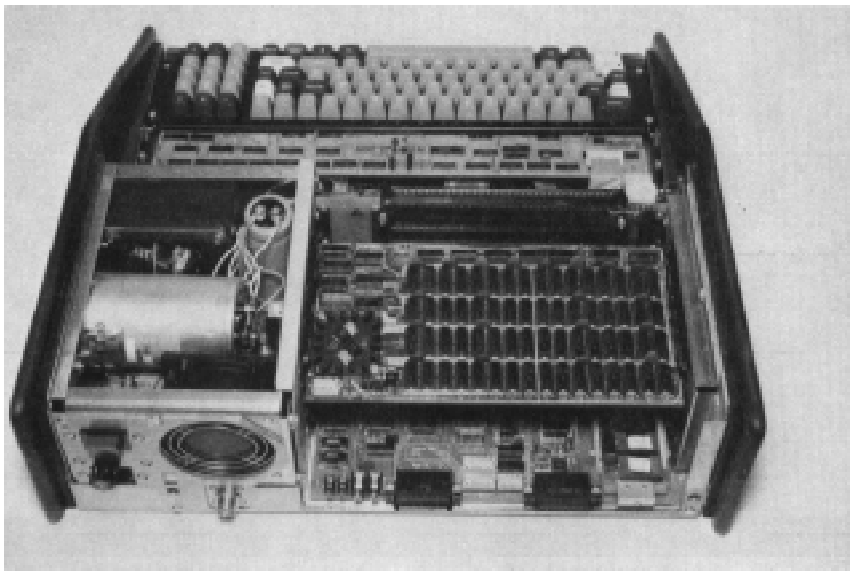


Figure 6—4. Sol-20 with covers removed. Rear side of assembly is in foreground and Sd-PC is just visible at lower right rear of assembly. 8KRA Memory is installed in expansion chassis above Sol-PC.

( ) Step 16. Install power supply subchassis in main chassis as shown in Drawing No. X-10.

Place subchassis over the rear right corner of main chassis and lower it almost vertically into position. Attach sub—chassis to main chassis using eight #6 x ¼ sheet metal screws. Five screws are driven through the bottom of the main chassis into the subchassis. The other three are driven through the right side of the main chassis into the subchassis.

( ) Step 17. Place right side walnut-masonite assembly in proper position against right side of main chassis and outline the finger well on the chassis. Remove backing from one black finger well label and affix it to the right side of main chassis. Position label to cover the finger well outline you made. Be sure label extends beyond all edges of the outline.

( ) Step 18. Using five 8-32 x ½ binder or pan head screws1 attach right side walnut—masonite assembly to main chassis and power supply subchassis as shown in Drawing No. x-lO. Insert screws from inside surface of chassis and drive into the plastic inserts you installed in Step 9. Note that the two front screws are driven through the main chassis, the two lower rear screws are driven through both the power supply subchassis, and the upper rear screw is driven through the power supply subchassis.

( ) Step 19. Assemble expansion chassis (“U” shaped chassis).

*( ) Prethread 12 mounting holes (six on each side) on expansion chassis side walls for backplane brackets with #6 x ¼ sheet metal screws. Three of these holes on each side are located near the front edge of the main chassis. The remaining three holes on each side are about 1½ to 2 inches behind the front three. Leave screws installed.

( ) Install female coaxial connector on the tab that extends out from the lower right front of the expansion chassis. Insert connector through tab so threaded end faces left as shown in Drawing No. X-10. Insert three 4-40 x 5/16 binder or pan head screws from left side of tab through the two front and lower rear mounting holes. Place #4 lockwahser on each and secure with 4—40 hex nuts. Insert another 4-40 x 5/16 binder or pan head screw through upper rear mounting hole and install 4—40 hex nut. (Leave this nut loose.)

*( ) Install 10 plastic card guides (five on each side) on inside surface of both side walls of the expansion chassis.

These are installed over thc ventillation grilles with the gripper fingers pointing towards the backplane board. install, simply insert posts on guide into appropriate mounting holes and push in until they snap into place.

( ) Step 20. Install expansion chassis on main chassis as shown in Drawing No. X-10.

Position expansion chassis with coaxial connector at the front (near FWB3 on power supply subchassis) over left rear area of main chassis and lower into place. Attach expansion chassis to main chassis using eight #6 x ¼ sheet metal screws. Four screws are driven through the bottom of the main chassis into the expansion chassis, three are driven through the left side of the main chassis into the expansion chassis, and one is driven through the lower left corner of the back side of the main chassis into the expansion chassis.

( ) Step 21. Attach left end of power supply subchassis bracket to expansion chassis as shown in Drawing No. X-10. Drive one 6 x ¼ sheet metal screw through expansion chassis into bracket.

( ) Step 22. Route coaxial cable from connector on fan closure plate along left side of power supply subchassis to connector on expansion chassis.

( ) Step 23. Using the #6 x ¼ sheet metal screw you removed in Step 15. re—attach fan closure plate to power supply subchassis. (Make sure side lip on plate is on right side of expansion chassis side wall.

( ) Step 24. Attach fan closure plate to expansion chassis with two #6 x ¼ sheet metal screws. Drive screws through expansion chassis into fan closure plate.

NOTE

If lip on fan closure plate and expansion chassis are not in contact, insert one or two ½" flat washers as needed between the two surfaces. Place washers so screws pass through them.

( ) Step 25. Connect free end of coaxial cable from connector on fan closure plate to connector on expansion chassis. Solder inner conductor to pin of connector. Remove hex nut on upper rear connector mounting screw, place lockwasher lug (coaxial shield) on screw and secure with nut.

Step 26. Install male coaxial connector on free end of co-axial cable that is connected to Sol-PC (the composite video output cable). Install connector as follows (refer to Figure 6—5):

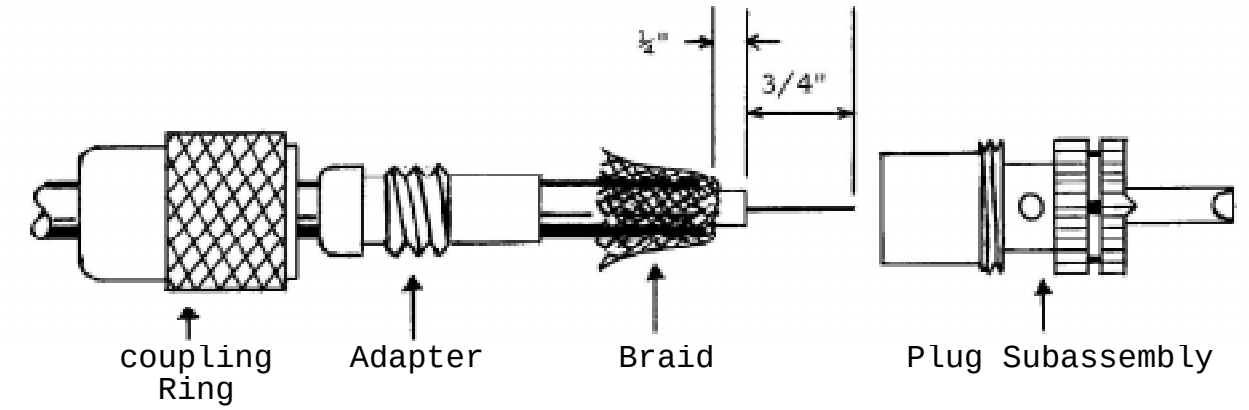


Figure 6—5. Sol—PC coaxial cable connector assembly.

( ) Slide coupling ring and adapter on cable in that order and cut end of cable even.

( ) Remove one inch of outer insulation.

( ) Fan braid slightly and fold back over outer insulation as shown.

( ) Slide adapter fully up under braid and press braid down over adapter body.

( ) Trim braid so that it does not interfer with adapter threads.

( ) Remove 3/4" of inner conductor insulation and tin exposed conductor.

( ) Slide cable fully into plug subassembly and screw subassembly on adapter.

( ) Solder braid to plug subassembly shell through solder holes. (Use enough heat to create a good bond between braid and shell.)

( ) Solder center conductor to plug contact by filling contact with solder. Cut off excess conductor.

( ) Slide coupling ring over plug subassembly and screw it onto plug.

( ) Step 27. Install Sol-PC in expansion chassis.

Position Soi-PC on bottom of expansion chassis with Ji, J2 and J6 through J9 at the rear. Align threaded standoff fs on bottom of Sol-PC with the oblong holes in the bottom of the main chassis.

Attach Sob-PC to chassis with eight 4-40 x 5/16 binder or pan head screws and #4 lockwashers. Place washer on screw and drive screw loosely into standoff from bottom of main chassis. Leave all eight screws loose.

( ) Step 28. Connect Sal-PC composite video output cable to expansion chassis coaxial connector.

( ) Step 29. Affix black finger well label to left side of main chassis in same manner as you did the right side. (See Step 17.) MAKE SURE LABEL DOES NOT OBSTRUCT ANY OF THE COOLING VENTS.

( ) Step 30. Using three 8—32 x ½ and two 8-32 x 1 binder or pan head screws, attach left side walnut—masonite assembly to main chassis as shown in Drawing No. 101000. Insert screws from inside surface of chassis and drive into the plastic inserts you installed in Step 8. Note that the two front screws (8—32 x ½) are driven through the main chassis, the uppermost screw (8-32 x ½) is driven through the expansion chassis, and the two lower rear screws (8—32 x 1) are driven through both the expansion chassis and main chassis.

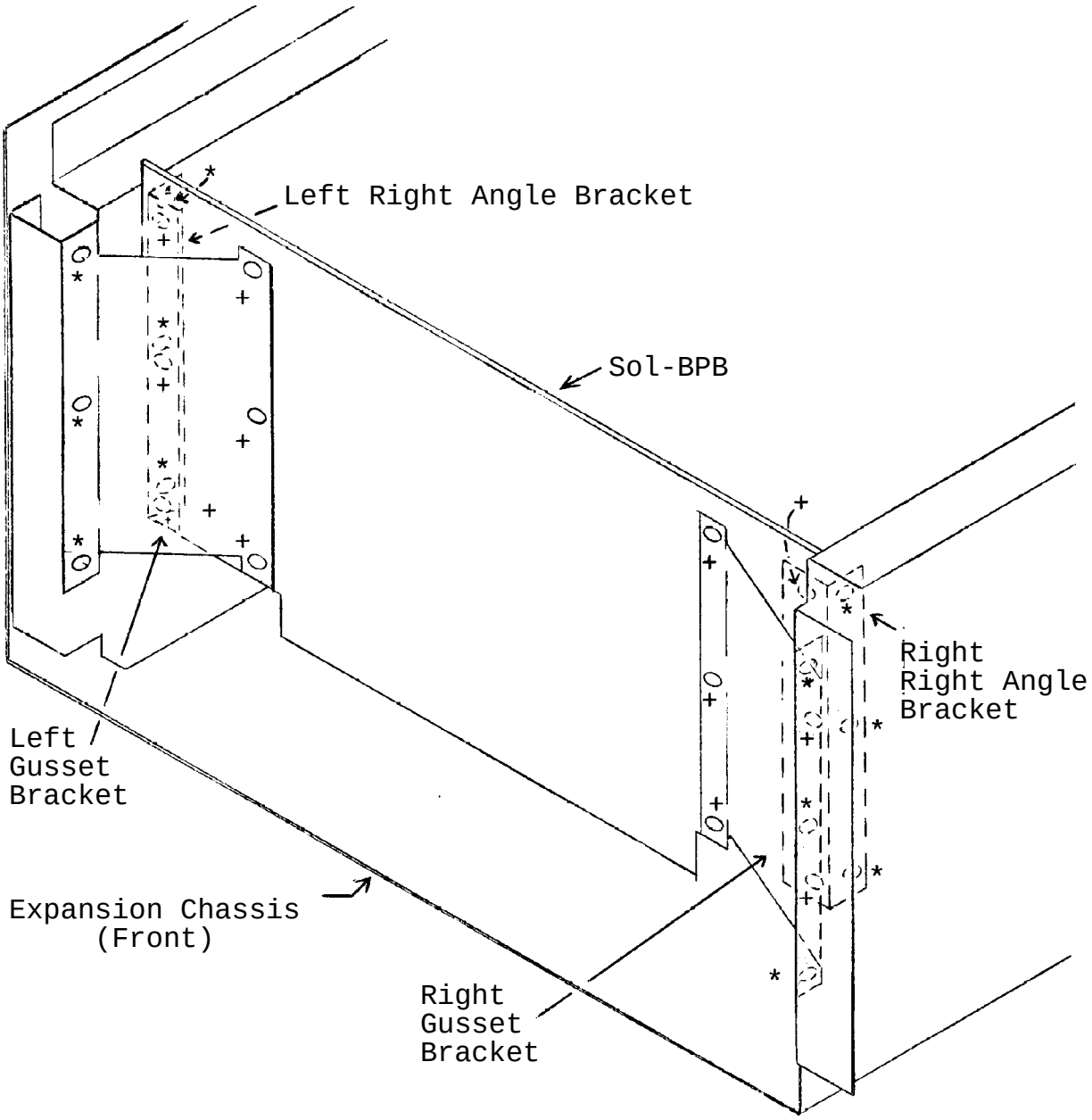
*( ) Step 31. Install left and right backplane right angle brackets (light gauge brackets) on expansion chassis side walls. Refer to Figure 6-6 on Page VI-16.) These two brackets are installed just to the front of the card guides and should be positioned as shown in Figure 6-6. Attach each bracket to the chassis with three #6 x ¼ sheet metal screws. USE THE SCREWS YOU USED IN STEP 19 TO PRETHREAD THE HOLES.

*( ) Step 32. Install backplane circuit board (Sol-BPB). The photograph in Figure 6-7 on Page VI—17 shows the backplane board installed.

*( ) Position Sol-BPB with 100-pin male edge connector down and the five female edge connectors facing the card guides. The board should rest against the front face of the right angle brackets as shown in Figure 6-6. Adjust position of Sol-PC as needed so that you can plug the Sol-BPB edge connector into Jll on the Sal-PC.

*( ) Align holes on left and right ends of Sol-BPB with those in right angle brackets.

(Step 32 continued on Page VI-17)



*
#6 x ¼ sheet metal screw
\+
4-40 x 5/8 binder or pan head screw,
#4 lockwasher and 4-40 hex nut

Figure 6-6. Backplane board (Sol-BPB) installation.

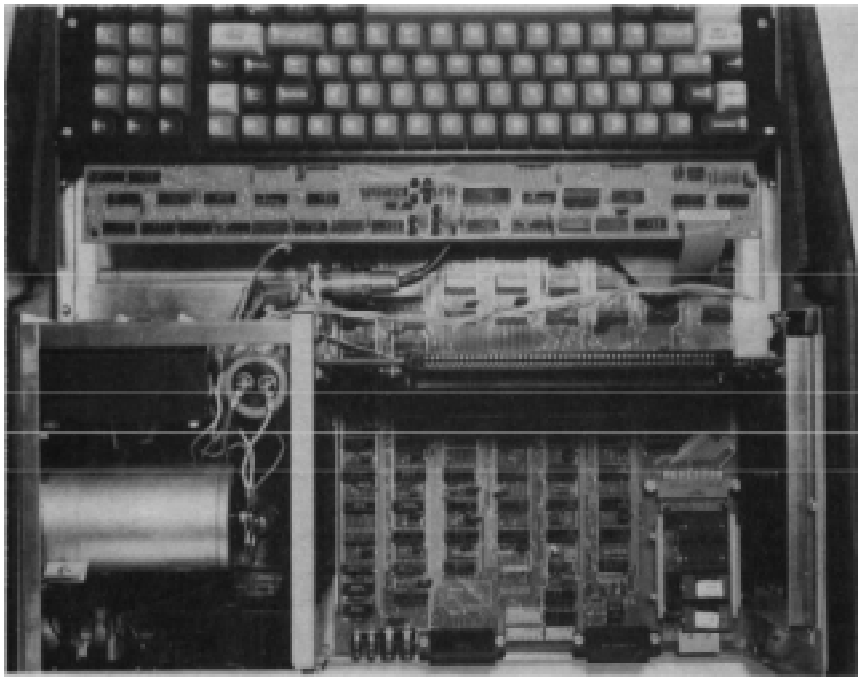


Figure 6—7. Backplane board (Sol—BPB) installation. Rear of Sol is at bottom and Sol-BPB is to right of power supply subchassis in line with C8 and transformer.

(Step 32 continued)

*( ) Attach Sol-BPB to brackets with three 4-40 x 5/16 binder or pan head screws, #4 lockwashers and 4—40 hex nuts on each side. Insert screws from the back side of bracket through Sol—BPB, place lockwasher on each screw and secure each with nut.

*( ) Step 33. Install left and right gusset brackets as shown in Figure 6-6 on Page VI—16.

*( ) Fit narrower gusset bracket on left side so that its flanges are flat against the expansion chassis side wall and the backplane board. (You may have to bend the flange slightly to obtain a proper Lit.)

*( ) Attach bracket to expansion chassis side wall with the three #6 x ¼ sheet metal screws you used in Step 19 to prethread the holes.

See WAPNING on Page VI-l8.

(Step 33 continued on Page VI-18.)

(Step 33 continued.)

WARNING

IT IS QUITE EASY TO SCRATCH OR CUT YOUR HAND ON THE SOLDER SIDE OF THE BACKPLANE BOARD WHEN DRIVING THESE SCREWS. PLACE A SUITABLE PROTECTIVE BARRIER, SUCH AS CARDBOARD, AGAINST SOLDER SIDE OF BACK-PLANE BOARD DURING INSTALLATION TO PRE-VENT SUCH INJURY.

*( ) Attach bracket to backplane board with three 4-40 x 5/8 binder or pan head screws, #4 lockwashers and 4—40 hex nuts. Insert screws from front side of bracket through Sol—BPB, place lockwasher on each screw and secure each with nut.

*( ) Install wider gusset bracket on right side in the same manner as you did the left bracket. THE PRECEDING WARN-ING ALSO APPLIES TO INSTALLING THIS BRACKET.

*( ) Step 34. Connect Sol-20 DC power cable from power supply subchassis to the Sol—BPB power cable you installed in Step 4.

( ) Step 35. Check that Sol-PC is in optimum position and tighten the eight screws holding the Sol-PC to the ex-pansion-main chassis assembly. (See Step 27.)

( ) Step 36. Connect Sol-PC power cable (4-wire) to J1O on Sol-PC. CAUTION: Make sure cable connector mates exactly with J10; that is, pin 1 to pin 1, pin 2 to pin 2, etc. Any other mating relationship will damage the IC’s on the Sol—PC. (Refer to Step 15 in Section III.)

( ) Step 37. Position keyboard (Sol—KBD) near its mounting brackets and connect 20-conductor ribbon cable supplied with Sol keyboard kit between J1 on keyboard and J3 on Sol-PC. With the cable connected properly, the cable will run away from the keys from J1 on the keyboard, and towards the keys from J3 on Sol—PC.

( ) Step 38. Attach keyboard to keyboard brackets with two 6-32 x ½ binder or pan head screws and #6 lockwashers on each side. Place washer on each screw and drive screws loosely into threaded holes in brackets.

( ) Step 39. If your kit does not include the 15-key numeric pad, install thc plastic insert supplied with your Sal keyboard kit to the keyboard cover. Attach it on the right end and to the bottom of the cover with masking tape.

( ) Step 40. Remove protective cover from one side of Plexiglass strip and attach “Sal Terminal Computer” trim plate to Plexiglass with small pieces of transparent tape. Place trim plate with printed side against Plexiglass.

( ) Step 41. Remove protective cover from other side of Plexiglass and slide it into the channel above the keyboard cutout.

NOTE

A hole is provided in the sheet metal behind the trim plate. This may be used for a “power on” indicator light if desired.

( ) Step 42. Install keyboard cover. Hook front of cover under front edge of main chassis and lower it over the keybaord. (A slight adjustment of the keyboard position may be needed to obtain a proper fit.)

Position keyboard within cutout in cover if needed and tighten keyboard mounting screws.

( ) Step 43. Install top cover.

( ) Be sure power cord is not plugged into 110 V ac outlet and disconnect cord from fan closure plate receptacle.

( ) Remove fuse holder cap and fuse.

CAUTION

NEVER REMOVE OR INSTALL FUSE WITH POWER ON.

( ) Hook top cover over back edge of keyboard cover and lower it down into place over the rear of the main chassis. Install the two thumb screws (one at the lower left corner and the other to the right of the fan closure plate coaxial connector) to attach cover to rear of main chassis.

( ) Step 44. Re-install fuse and plug power cord into receptacle. BE SURE POWER CORD IS NOT PLUGGED INTO 110 V ac OUTLET.

See CAUTION on Page VI-20.

(Step 44 continued.)

CAUTION

NEVER REMOVE OR INSTALL FUSE WITH POWER ON.

( ) Step 45. Remove backing from connector identification label and affix it to rear of top cover. Position label just above Sol—PC connector opening in cover so that "J9" is aligned with left mast (as viewed from rear of Sol) subminiature phone jack and "J1" is aligned with right most 25-pin female connector.

( ) Step 46. Remove backing from serial number label and affix it to rear of top cover. Position label to right (as viewed from rear of Sol) of fan opening in cover.

( ) Step 47. Affix self—stick protective pads to bottom of Sal as shown in Figure 6—8.

You have now completed assembly of your Sol Terminal ComputerTM . It is ready for use as a stand—alone computer or CRT terminal. Congratulations on a job well done.

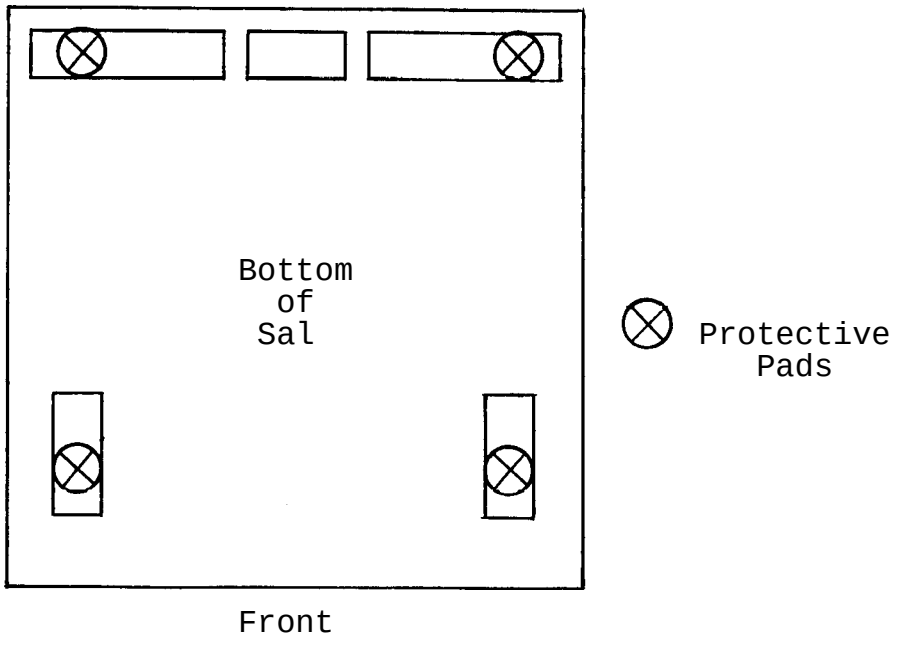


Figure 6-8. Protective foot pad installation.

7.1 INTRODUCTION

Information in this section will help you to become familiar with the operation of your Sol Terminal Computer™. Following brief explanations of the operating controls and the two basic operating modes, you will put your Sol through some simple operations. This should sufficiently acquaint you with the keyboard and control switches so that you will feel at ease with your Sol. In addition, you will have performed functional tests of all Sol sections except the parallel data interface.

Detailed descriptions of the control switches are also provided to allow you to gain greater proficiency in their use. For the same reason, individual keyboard key descriptions are also given. They are intended to be used along with the BASIC/5 and SOLOS Users' Manuals (or if applicable the CONSOL description in Section IX of this manual).

The balance of this section supplies instructions for 1) connecting typical peripheral devices to the serial and parallel data interfaces (J1 and J2), 2) using audio cassette recorders, and 3) changing the fuse.

7.2 THE OPERATING CONTROLS

Sol operating controls are identified and their functions briefly defined in Table 7-1 on Page VII-2. Unless noted otherwise, the location of each control is shown on the Sol-PC assembly drawing in Section X, Page X-3.

7.3 BASIC OPERATING MODES

7.3.1 Command Mode

In this mode Sol operates as a stand alone computer under control of the program (software) contained in the personality module and additional software that is stored in the Sol, stored either in a read only memory (ROM) that is plugged into the computer or the Sol random access memory (RAM). (For a description of the CONSOL and SOLOS Personality Modules, refer to Section IX in this manual and the SOLOS Users' Manual respectively.)

With the SOLOS Personality Module installed, the computer is in the command mode when power is applied to the Sol. Command mode is a sort of "home base" from which excursions may be made into other programs. An analysis of three levels of programs will make the concept of command mode more understandable.

At the lowest level of software are the instructions which the 8080 CPU (central processing unit), the brains of the computer,

Table 7-1. Sol Operating Controls and Their Functions.

CONTROL	FUNCTION
ON-OFF Switch (See Figure 7-1)	Connects and disconnects primary power to Sol.
RST (Restart) Switch, S1-1	Permits manual restart of Sol without turning power off. (Useful for test purposes.)
BLANK Switch, S1-3	Determines if control characters are displayed or not.
POLARITY Switch, S1-4	Selects normal (white characters on black background) or reverse video display.
BLINK-SOLID Switches, S1-5 & 6	Selects blinking, nonblinking or no cursor.
SSW0 – 7 S2-1 through 8	Permits direct data entry to processor.
BAUD RATE Switches, S3-1 through 8	Sets operating speed of serial data interface (SDI).
PS & PI Switches S4-1 & 5	Selects no parity, even parity or odd parity for SDI.
WLS-1 & 2 Switches, S4-2 & 3	Selects number of data bits in transmitted word for SDI.
SBS Switch, S4-4	Determines number of stop bits in transmitted word for SDI.
F/!H Switch, S4-6	Selects half or full duplex operation for SDI.
Keyboard (See Figure 7-4)	Data entry, mode selection, command input and cursor control.

can understand and run. All programs must ultimately be reduced to this basic level to be operated on by the computer. In the case of the 8080 microprocessor, the program is in an "object code" or "machine language", since the "machine" or 8080 CPU understands it. The SOLOS program contained in the personality module is stored in this machine language form, and the computer can therefore run directly from this program. Since the SOLOS program is contained in permanent ROM which is plugged directly into the computer, the SOLOS program is always available, and is automatically selected whenever the power switch of the Sol is turned on. There is also provision for returning at all times to the command mode of SOLOS. From the command mode other programs may be brought in for various operations or stored on cassette tape. The contents of the computer's memory may be displayed or changed. The command mode also performs "housekeeping" functions such as setting the rate at which data is read from tape, or the rate at which characters are displayed on the video monitor.

The command mode allows the introduction of the second level of software. This level includes higher-level language programs such as BASIC/5 or FOCAL in which complex application programs may be more easily written. These are called higher level languages because they permit the user to write programs in a form much closer to human languages such as English. However, programs written in these languages must be translated into the more basic machine language before they can be run. Besides higher level languages, this second level of software includes programs such as the TREK 80 and GAMEPAC video games and the ALS-8 program (a software package used for developing programs), all of which are offered by Processor Technology Corporation. Through the facilities of the command mode, these second level programs are transferred (loaded) into memory from cassette tape or other storage media, and then "executed" (used). These programs may also exist in ROM or EPROM (erasable programmable ROM) memory which is plugged into the computer to make them instantly available like the SOLOS program. All first and second level programs are stored in the computer as binary object code.

Let us illustrate the concept of the second level of programs with an example, BASIC/5. Using the "XEQ" command available in the SOLOS command mode, we load the BASIC/5 program into the computer's memory from cassette tape. With this command BASIC/5 is ready for use as soon as the tape has stopped moving. The control of the computer is now taken over by the BASIC/5 program now in memory, and SOLOS is no longer in command. All the features of BASIC/5 language are now available to us, with a new set of commands and rules. Since the CPU of the computer only understands the machine language of the first level of software, the BASIC/5 program must translate the commands and data we enter to this lower level. BASIC/5 does this as we go. While we are using BASIC/5, we still have access to some of the commands and features of SOLOS, although they may have a modified form while we are in BASIC/5. We will load and use BASIC/5 later in this section.

The third level of software consists of programs written using the higher order languages of the second level programs. A program written in BASIC/5 is on this third level. This program only makes sense to the computer while the computer has BASIC/5 in memory and control has been transferred to the BASIC/5 program. Third level programs written in any high level language are often called "applications programs" since they are usually written in order to fit a specific application need.

The ALS-8 Program Development System is another second level program. A program to be developed within ALS-8 would then be a third-level application program. The ALS-8 also includes an Assembler which takes a program written on the third level in "assembly" language, and translates it to object code which the computer can run. The object code version then resides in memory and can be run in another operation. For a further discussion, of types of software see the article "Your Personal Genie" in Appendix VIII of this manual.

7.3.2 Terminal Mode

Sol operates as a CRT terminal in this mode, capable of sending keyboard data to an output port and displaying data received at the serial input port on an external video monitor via the Sol video display circuitry. When Sol is "hard-wired" to another computer or connected to a modem, the terminal mode is used for data entry, data retrieval, inquiry/response and monitoring and control applications.

Capabilities in the terminal mode depend on the personality module used. Both CONSOL and SOLOS Personality Modules permit operation as a CRT terminal. CONSOL 1) initializes Sol in the terminal mode whenever you turn the power on or initiate a system reset, 2) sends keyboard data to the serial data interface (SDI) only, and 3) provides simple stand-alone computer capabilities. SOLOS, on the other hand, 1) enters the terminal mode when given the "TERM" (terminal) command, 2) sends keyboard data to any output port available with the "SET 0" (set out) command, and 3) duplicates CONSOL functions while providing additional capabilities.

7.4 GETTING ACQUAINTED WITH Sol

One of the best ways to get acquainted with your Sol is to use it. After connecting a cassette recorder and video monitor to your Sol, you will operate the system in the terminal mode to become familiar with the keyboard and the functions of the video display switches. You will then switch to the command mode and perform some of the basic computer operations.

7.4.1 Monitor and Cassette Recorder Connections

The basic Sol system consists of the Sol, a video monitor for display (e.g., the Processor Technology PT-872 TV-Video Monitor by Panasonic) and a cassette recorder for external storage (e.g., the Panasonic Model RQ-413S).

To connect these three system components, you will need the following cables:

Audio In & Out Cables -- two cables of shielded wire fitted with miniature phone plugs at both ends.

Motor 1 Cable -- one cable pair, such as speaker wire, fitted with subminiature phone plugs at both ends. (An identical cable for Motor 2 is needed if you use two recorders.)

Video Cable -- one RG59/U coaxial cable fitted with a PL259 UHF male connector on one end and a monitor-compatible connector on the other.

Connect the basic Sol system as follows (refer to Figure 7-1 on Page VII-6):

( ) Step 1. Remove top and keyboard covers from Sol.

( ) Step 2. Plug one end of Audio In Cable into Audio IN jack (J7) on Sol rear panel, and plug other end into MONITOR or EARPHONE jack on recorder.

( ) Step 3. Plug one end of Audio Out Cable into Audio OUT jack (J6) on Sol rear panel, and plug other end into AUXILIARY or MICROPHONE jack on recorder. (The AUXILIARY input is preferred and recommended over the MICROPHONE input.)

NOTE

If your recorder has only a microphone jack, remove the I-to-J jumper installed in Step 69 in Section III and install a jumper between I and H.

( ) Step 4. Plug one end of Motor I Cable into Motor I jack (J8) on Sol rear panel, and plug other end into REMOTE jack on recorder.

( ) Step 5. Connect PL259 UHF connector on Video Cable to video output connector on Sol rear panel, and connect other end to video monitor input connector.

( ) Step 6. Make sure monitor, recorder and Sol power switches are in their OFF position. Then connect AC power cord to AC receptacle on Sol rear panel and connect Sol, monitor and recorder to appropriate power source.

7.4.2 Terminal Mode Operation

The following procedure assumes your Sol is equipped with a SOLOS personality module.

( ) Step 7. Set Sol control switches as follows (see Figure 7-2 on Page VII-7):
RST Switch (S1-1): OFF
S1-2 (spare): OFF
BLANK Switch (S1-3): OFF (display control characters)
POLARITY Switch (S1-4): OFF (reverse video display)
BLINK Switch (S1-5): OFF (solid cursor)
SOLID Switch (S1-6): ON (solid cursor)
(Step 7 continued on Page VII-7.)

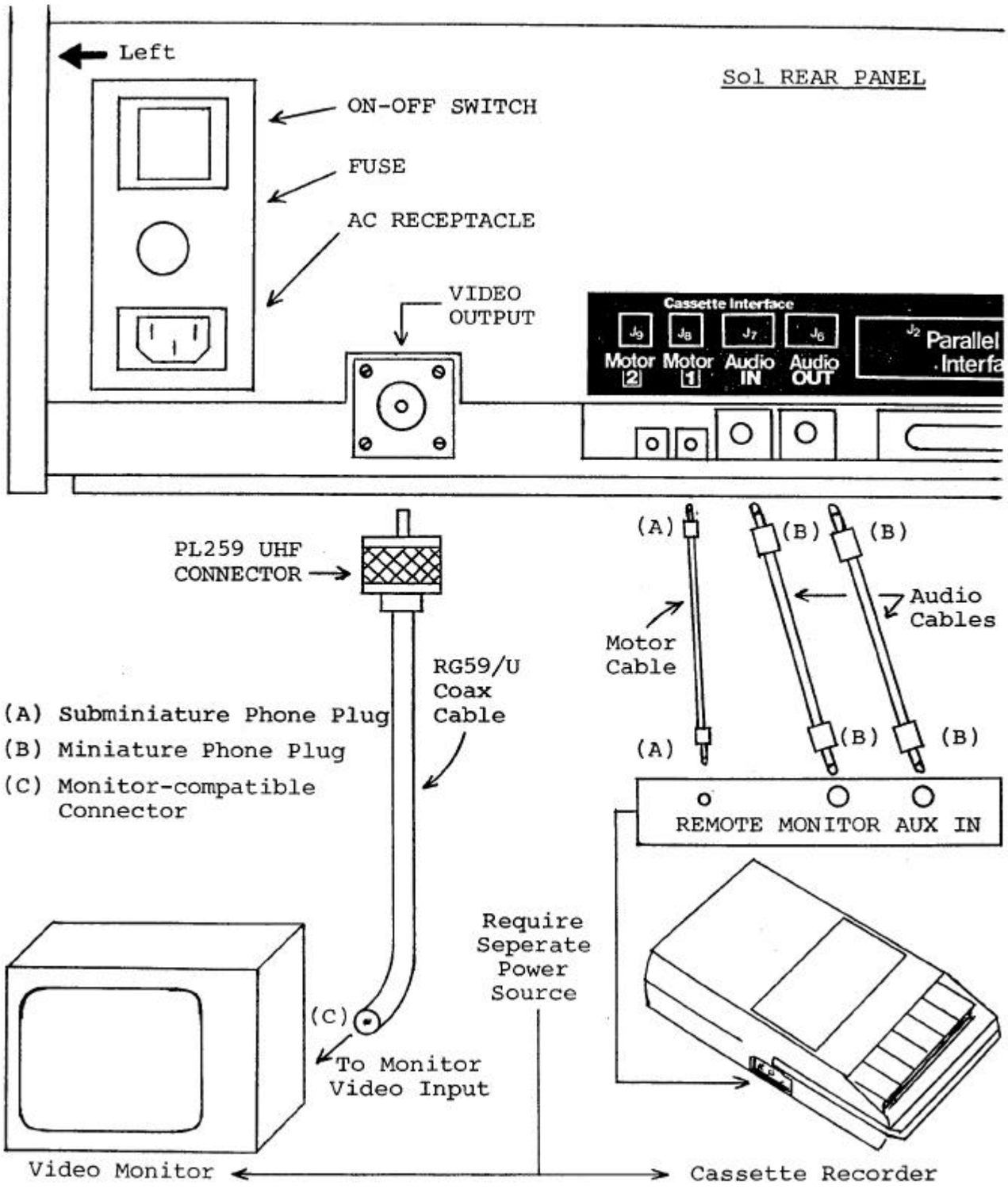


Figure 7-1. Connecting the basic Sol system

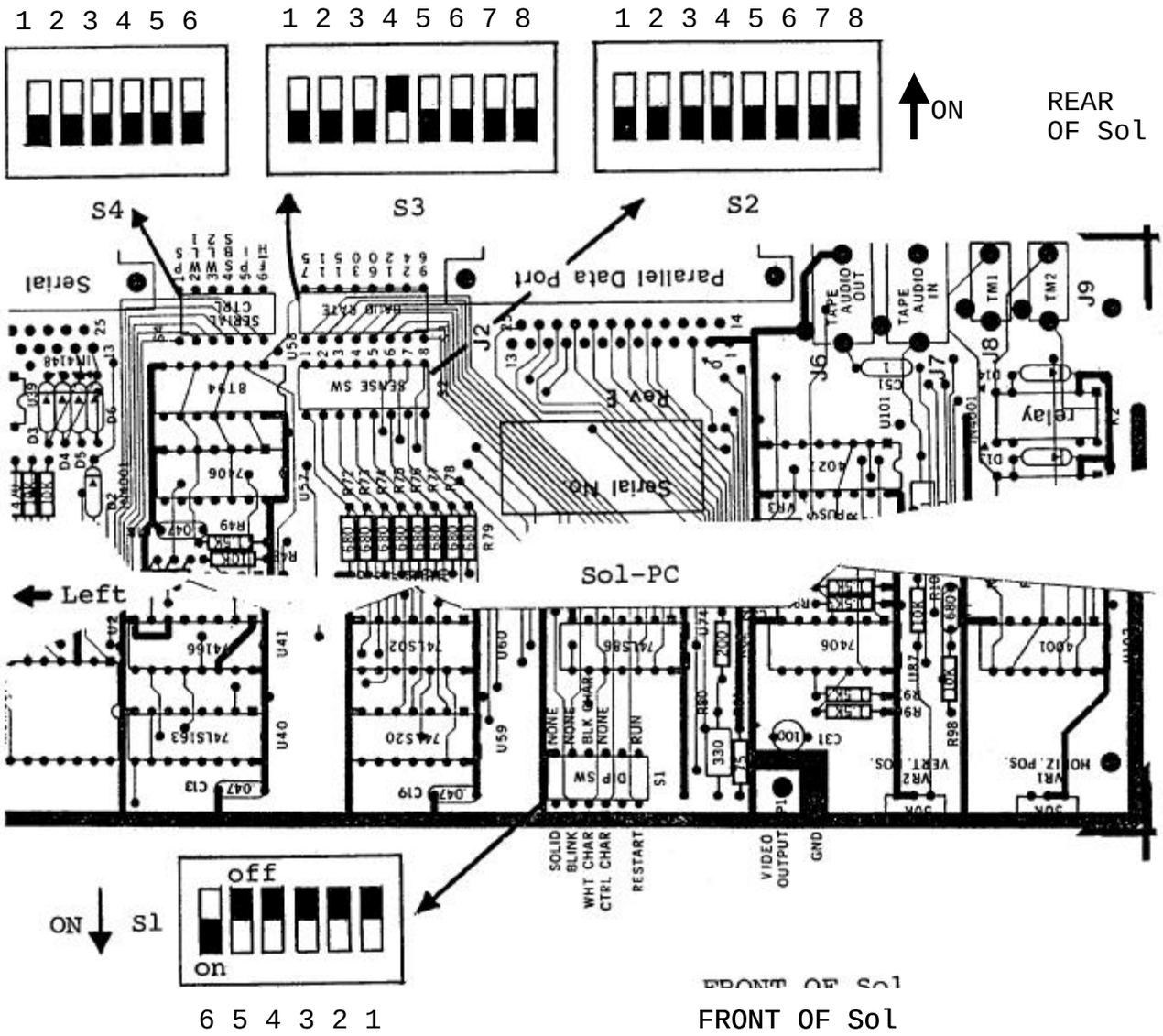


Figure 7-2. Sol control switch settings for terminal mode.

(Step 7 continued.)

SSW Switches (S2-1 - 8): OFF

BAUD RATE Switches (S3-1 - 8): S3-4 ON, all others OFF (300 Baud)

SDI Switches (S4-1 - 6): OFF (selects full duplex operation, 8 data bits, 2 stop bits and no parity)

( ) Step 8. Turn Sol and monitor on.

( ) Step 9. If the monitor display raster is out of sync (black horizontal bar moves slowly down screen, numerous black lines cut across raster, or both), adjust monitor vertical and horizontal hold controls for a stable raster.

( ) Step 10. You should see a prompt character followed by the cursor (>■) in the upper left corner of the screen. If you don't, adjust VRI and VR2 (see Figure 7-3) to move the prompt character and cursor onto the screen. (With CONSOL, only the cursor will appear on the screen.)

NOTE

Use VR1 (horizontal position) and VR2 (vertical position) to center the display page (16 lines, 64 characters/line) on the screen.

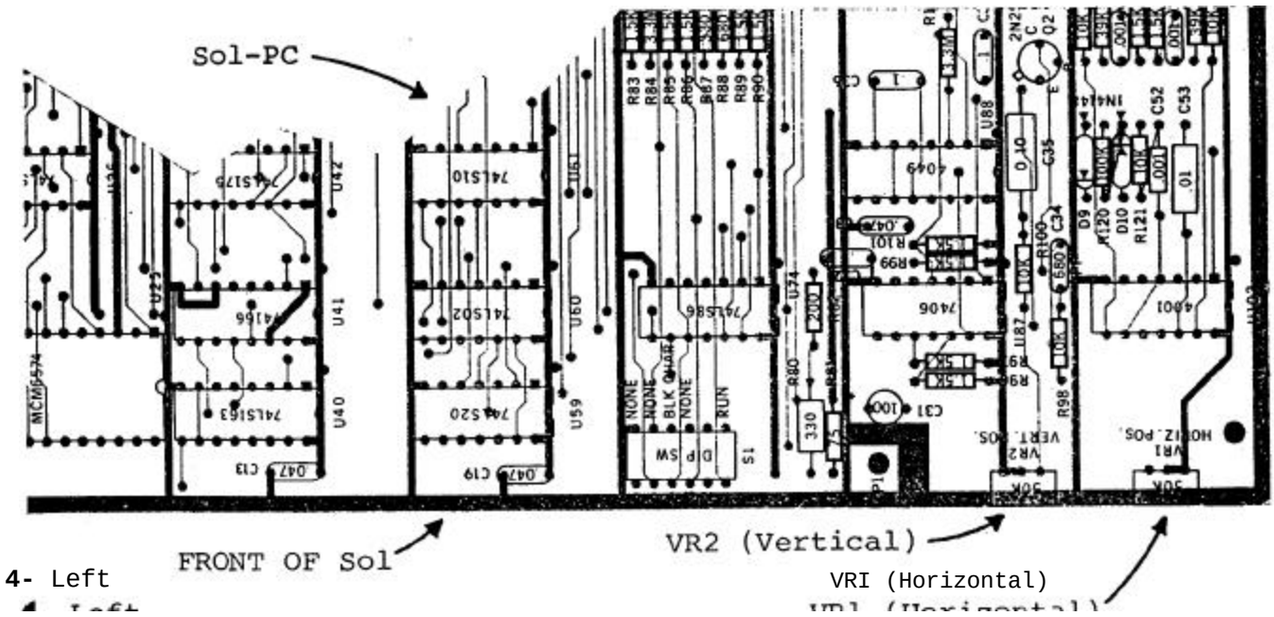


Figure 7-3. Location of positioning adjustments, VRI and VR2.

( ) Step II. Enter terminal mode by 1) pressing UPPER CASE key to turn the indicator light on (Alphabetic characters are now entered as upper case, regardless of SHIFT key status, but dual character keys do respond to SHIFT key.), 2) typing TERM and 3) pressing RETURN key. (If your Sol is equipped with CONSOL, it entered terminal mode when you turned the Sol on.) "TERM" will appear on the screen as you type, and the cursor will disappear when you press the. RETURN key.

NOTE: All commands must be given in upper case characters in order to be recognized, and the RETURN key must be pressed after a command so that SOLOS can execute the command (MODE SELECT excepted).

( ) Step 12. Set for local operation by pressing LOCAL key to turn indicator light on. Set for lower case operation by pressing UPPER CASE again (indicator light out).

( ) Step 13. Press each of the alphanumeric, punctuation and symbol keys. As each is pressed, the lower case character in the UNSHIFTED column of Table 7-4 should appear on the screen. Read Section 7.7 on page VII-17 to become familiar with Table 7-4.

NOTE: If the MODE SELECT key is pressed, SOLOS will return to the command mode and display a prompt character followed by the cursor. In this case return to terminal mode by typing "TERM" in upper case letters, followed by a carriage return.

( ) Step 14. Press SHIFT LOCK key to return keyboard to shifted operation (indicator light will go out) and repeat Step 13. Each corresponding upper case character should appear from the SHIFTED column of Table 7-4.

( ) Step 15. Use the control sequences given in Table 7-4 on Page VII-18 to generate the indicated control characters. Control characters are generated by pressing the CTRL (control) key and, while holding it depressed, pressing the desired key given in the first column of the table. As the table shows in the last two columns, the symbol generated by a control sequence depends on whether a 6574 or 6575 character generator (U25) is installed in your Sol. Two examples follow:

CONTROL SEQUENCE	6574 SYMBOL	6575 SYMBOL
CTRL and I	→	H_T
CTRL and 5 or %	☒	E_Q

( ) Step 16. Change video display polarity by setting POLARITY Switch (SI-4) to ON and observe the effect on the display. It should change from black characters on a white background to white characters on a black background.

( ) Step 17. Switch from non-blinking cursor to a blinking cursor by setting SOLID Switch (SI-6) to OFF and BLINK Switch (SI-5) to ON in that order. You should see a rectangular solid cursor that blinks on and off approximately two times per second. Never put SI-5 and SI-6 ON at the same time.

( ) Step 18. Blank control characters by setting BLANK Switch (SI-3) to ON. Any control characters generated (refer to Step should not appear on the screen.

Up to this point, keyboard data has been processed by the CPU, transmitted out through the serial channel output, looped back

to the serial channel input and then displayed on the video monitor. You have consequently just "tested" the CPU, serial channel and display section functions in your Sol.

7.4.3 Command Mode Operation

The following operations assume your Sol is equipped with a SOLOS personality module.

Using the Cassette Recorder. The following procedure for loading a program from cassette tape into Sol memory provides a good example of how to use an audio cassette recorder with Sol. In this example you will use the BASIC/5 cassette supplied with your Sol.

( ) Step 19. Set POLARITY (S1-4) and BLANK (S1-3) Switches as desired.

( ) Step 20. Replace top and keyboard covers.

( ) Step 21. Load BASIC/5 cassette in recorder. If required, fully rewind tape. (This can be done by disconnecting the REMOTE plug from the recorder and using the REWIND control on the recorder.) After rewinding, reconnect REMOTE plug.

( ) Step 22. Set the following recorder controls and indicator, if so equipped, as indicated:

Transport: press STOP control

Volume: midrange

Tone: top of range (maximum treble)

Tape Counter: 0

( ) Step 23. Press PLAY control on recorder. The tape should not move. If it does, there is a malfunction in the remote control circuitry or cabling. (With the Sol off, there should be no continuity between the REMOTE plug contacts.)

NOTE

The tape head must be clean to reliably read a tape or write on tape.

( ) Step 24. If needed, press MODE SELECT key on Sol to enter command mode. (Remember SOLOS initializes in the command mode while CONSOL initializes in the terminal mode whenever Sol is turned on.) You should see a prompt character followed by the cursor (**>■**) on the left of the screen.

( ) Step 25. Type the XEQ command as follows:

XEQ BASIC

( ) Step 26. Press the RETURN key on Sol. The cursor should disappear and the tape should advance. The display should not change otherwise. NOTE: With certain cassette recorders or cassettes there may be a misreading of the tape when the splice joining the leader to the tape passes the tape head. In this case an ERROR message will appear and the tape will stop. To resume tape "loading", retype the XEQ BASIC command. If further difficulty is encountered, try different cassette recorder volume settings until a reliable setting is found.

( ) Step 27. If the tape has loaded successfully, in approximately two minutes BASIC/5 will display five lines of text ending with:

SOL BASIC 5

READY

( ) Step 28. BASIC/5 is now ready for use. Refer to your BASIC/5 User's Manual. Become familiar with both BASIC/5 and the Sol keyboard. Try some exercises in BASIC/5.

Dump Operation. The dump operation displays memory data in hexadecimal on the video monitor. It can also be used with the appropriate SET command to output memory data to a hard-copy device (e.g., a printer). As an example, dump the first part of the SOLOS personality module (C000 through C0E0) as follows:

( ) Step 29. Set UPPER CASE key so that the indicator is on. If you are still in BASIC/5, type the BASIC/5 command "BYE" at the beginning of a command line to re-enter SOLOS command mode. BASIC/5 remains in memory and may be returned to by typing a command line: "EXEC 0".

( ) Step 30. Type the DUMP command as follows:

DUMP C000 C0E0

( ) Step 31. Press RETURN key. Lines of 16 bytes of hexadecimal data will scroll (move) rapidly up the screen until the last address (C0E0) is displayed. At this point the display will stop scrolling.

Enter Operation. The enter operation is used to enter hexadecimal data from the keyboard into available Sol memory. As an example, enter 16 bytes of data, starting at address C900 and ending at address C90F, as follows:

( ) Step 32. Type the ENTER command as follows:

ENTER C900

( ) Step 33. Press RETURN key. The monitor should display a colon (:) prompt character at the start of the next line.

( ) Step 34. Type the following data:

II 22 33 44 55 66 77 88 99 00 AA BB CC DD EE FF/

NOTE

The slash (/) terminates the enter function.

( ) Step 35. If you made a mistake in typing the above line of data, refer to Paragraph 7.8.3 on Page VII-25. If you made no mistakes, press RETURN key.

The data entered in Step 34 now resides in locations C900 through C90F in the Sol memory.

( ) Step 36. To verify that the data did indeed enter Sol memory, simply give your Sol this DUMP command:

DUMP C900 C90F

Then press RETURN key. The line of data you entered in Step 35 should be displayed on the monitor screen, preceded by the starting address.

( ) Step 37. Using your SOLOS User's Manual, experiment with the other commands until you feel at home with your Sol.

The preceding command mode operations used the CPU, personality module, audio cassette interface (ACI) and the Sol RAM. You have consequently just tested the functions of these sections.

7.5 OPERATING CONTROLS IN DEPTH

Unless indicated otherwise, the location of the controls described in this paragraph are shown on the Sol-PC assembly drawing in Section X, Page X-3.

7.5.1 ON-OFF Switch (See Figure 7-1 on page VII-6.)

Push this switch in to turn your Sol on. In the ON position the switch remains locked in its "in" position. To turn your Sol off, push the switch again. This releases the locking mechanism, and the switch will return to its OFF ("out") position.

7.5.2 Restart (RST) Switch, S1-1

This switch permits you to restart your Sol without turning the power off. You should normally leave it in its OFF, or run, position. Set it to ON and then OFF to initialize the Sol circuitry and reset the CPU program counter to zero. (A manual restart with this switch performs the same function as turning the power on or pressing a keyboard generated restart: UPPER CASE key with REPEAT key.)

7.5.3 Control Character Blanking (BLANK) Switch, S1-3

Set this switch to its ON position if you do not want control characters (see Table 7-4 on Page VII-18) to be displayed on the screen. In the OFF position, control characters are displayed.

7.5.4 Video Display (POLARITY) Switch, S1-4

If you want a normal video display (white characters on a black background), set this switch to its ON position. In the OFF position, black characters will be displayed on a white background (reverse video display).

7.5.5 Cursor Selection (BLINK, SOLID) Switches, S1-5 & 6

CAUTION

DO NOT SET S1-5 AND S1-6 TO THEIR ON POSITIONS AT THE SAME TIME. TO DO SO MAY DAMAGE YOUR Sol.

If you want the cursor to blink, set S1-6 to OFF and S1-5 to ON. The cursor will blink on and off about two times per second.

Set S1-5 to OFF and S1-6 to ON if you want a non-blinking (solid) cursor.

With both S1-5 and S1-6 in their OFF positions, there will be no cursor display.

7.5.6 Sense (SSW0 - 7) Switches, S2-1 through S2-8

These eight switches are normally left in the OFF position. They are used to manually enter data into the CPU. (They serve the same function as the front panel sense switches on the Altair 8800 and IMSAI 8080.)

S2-1 is the least significant data bit (D100) and S2-8 is the most significant data bit (DIO7). To pull a DIO bit low (when the program tests SSW0 - 7), set the switch associated with the bit to ON. An open (OFF) switch pulls the associated DIO bit high when the program tests SSW0 - 7.

NOTE

The configuration of SSW0 - 7 is tested by the CPU only when it executes an input port FF instruction. Otherwise, the Sense Switches have no bearing on Sol operation.

7.5.7 Baud Rate Switches, S3-1 through S3-8

The setting of the Baud Rate Switches determines the operating speed of the Serial Data Interface (SDI). Assuming you have not installed any of the K, L and M jumper options, you can select any one of eight Baud rates. Table 7-2 on page VII-15 defines Baud rate as a function of S3-1 through S3-8.

CAUTION

DO NOT SET MORE THAN ONE S3 SWITCH TO THE ON POSITION AT THE SAME TIME. TO DO SO CAN DAMAGE YOUR Sol.

7.5.8 Parity (PS, PI) Switches, S4-1 & 5

With these two switches you can select no parity, parity, even parity or odd parity for data handled through the SDI (J1).

Set S4-5 (PI) to its ON position if you want a parity bit. When OFF, there will be no parity bit. (A stop bit immediately follows the data if no parity bit is selected.)

S4-1 (PS) selects even or odd parity if S4-5 is ON. It otherwise has no affect. For even parity, set S4-1 to ON. Set S4-1 OFF for odd parity.

7.5.9 Data Word Length (WLS-I & 2) Switches, S4-2 & 3

Use these two, switches to select the number of bits, excluding parity, in the transmitted word for the SDI. You have a choice of 5, 6, 7 or 8 bits. Table 7-3 defines word length as a function of S4-2 and S4-3.

7.5.10 Stop Bit Selection (SBS) Switch, S4-4

Set this switch to ON if you want one stop bit transmitted out of the SDI. In the OFF position, two stop bits are transmitted unless you have selected a five bit word length. In that case 1.5 stop bits are transmitted.

Table 7-2. Baud Rate Selection With Switch S3.

BAUD RATE	SWITCH S3 CONFIGURATION*
75	S3-1 ON, all others OFF
110**	S3-2 ON, all others OFF
150	S3-3 ON, all others OFF
300	S3-4 ON, all others OFF
600	S3-5 ON, all others OFF
1200	S3-6 ON, all others OFF
2400	S3-7 ON, all others OFF
4800***	S3-8 ON, all others OFF

*Set no more than one switch to ON at the same time.

**Rate required by standard 8-level TTY's (Teletype Machine).

***Assumes K-to-M jumper on Sol-PC is not installed. With K-M jumper in and L-M trace on back side of Sol-PC cut, SDI operates at 9600 Baud when S3-8 is ON and all others OFF.

NOTE FOR REV D Sol-PC BOARDS: With S3-7 ON and all others OFF, Baud rate is either 2400 (K-to-M jumper not installed) or 4800 (K-M jumper in and L-M trace on back side of Sol-PC cut). With S3-8 ON and all others OFF, Baud rate is 9600.

Table 7-3. Word Length Selection With S4-2 & 3.

WORD LENGTH (Number of Bits)	SWITCH SETTINGS	
	S4-2	S4-3
5	ON	ON
6	ON	OFF
7	OFF	ON
8	OFF	OFF

7.5.11 Full/Half Duplex (F/H) Switch, S4-6

Set this switch to ON if you want half duplex operation in the terminal mode. In half duplex operation, data transmitted out the SDI (J1) is "looped back" and received by the SDI for subsequent

display on the monitor. Use this type of operation when your Sol works with an external computer that does not "echo" data back to the Sol.

For full duplex: operation in the terminal mode, set S4-6 to OFF. Only received data is displayed in full duplex operation. Use full duplex when Sol's transmitted data need not be displayed. (Note that transmitted data from the Sol, if echoed back, is displayed as received data.)

NOTE

If no Baud rate is selected, data will not be transmitted out of the SDI.

7.5.12 Keyboard

The keyboard is an output device that produces ASCII (American Standard Code for Information Interchange) encoded data. It is hardwired to an input port on the Sol and is used for data entry. ASCII data is interpreted by the Sol as data and/or commands as determined by the current system monitor program. The monitor program may be in the personality module, ALS-8, Sol RAM memory or some memory.

7.6 THE KEYBOARD, GENERAL DESCRIPTION

The Sol Terminal Computer has ASCII 96-character keyboard. Its key arrangment conforms with the QWERTY (standard typewriter) format. As shown in the photo on page X-26, there are also 12 control keys (including five basic cursor controls) and seven special function keys. A 15-key arithmetic pad, available as an option on the Sol-10, is provided as standard equipment on the Sol-20.

7.6.1 Operating Features

The Sol keyboard features N-key rollover. That is, several keys can be pressed at the same time without loss of characters or commands. Key entries, however, are in the order of actual key closures. (The keyboard circuitry includes a scanning circuit that prevents simultaneous key operation.)

7.6.2 Keyboard Indicators

Three keys (SHIFT LOCK, UPPER CASE and LOCAL) have indicator lights to indicate keyboard/terminal status. When any of these keys is pressed to turn an indicator light on, the light remains on after the key is released to show that the status persists. Pressing the key again turns the light out to indicate the change in status.

7.7 INDIVIDUAL KEY DESCRIPTIONS

The exact function of most keys on the Sol keyboard is determined by the software used (e.g., the personality module). Others have predefined functions that are common to the CONSOL and SOLOS Personality Modules. (Note that any key that generates a code can be redefined by a program to perform a specific funstion.) The code generated by each key on the keyboard and the corresponding character, or symbol, produced by the Sol's character generator (U25) are given in Table 7-4 on Pages VII-18 through VII-21.

Table 7-4 has two main headings: 1) KEY which identifies the keys on the Sol keyboard and 2) HEXADECIMAL CODE/CHARACTER GENERATION which specifies for each key the hexadecimal code generated by the keyboard and the symbol produced by the Sol's character generator. The second heading is divided into three major categories: UNSHIFTED, SHIFTED and CONTROL. UNSHIFTED defines the results when operating the keys unshifted (lower case), SHIFTED provides the same information when they are operated shifted (upper case), and CONTROL defines the results of control sequences (refer to Paragraph 7.7.7 on Page VII-22). Within each of these three categories you will find the hexadecimal code generated and the symbol displayed in response to that code by either of the two possible character generators that can be supplied with your Sol, the 6574 and 6575. Some keys move the cursor without displaying a new character.

Looking at the "W" entry on Page VII-18 and reading across the table, we see that:

1. Pressing "W" unshifted would generate the code 77 and either character generator (6574 or 6575) produces a lower case "W" (w). Do not actually press the keys at this point.

2. Pressing "W" shifted would generate the code 57 and either character generator would produce an upper case "W" (W).

3. Pressing CTRL (control) and "W", whether shifted or unshifted, generates the code 17 which causes the 6574 to produce the graphic symbol “-|”) for the ASCII "end of transmission block" control character and the 6575 to produce a two-character mnemonic (E_B) for that same control character.

In the following paragraphs, each key function is described in terms of its role in the terminal mode only and assumes the control character display option is enabled and the LOCAL indicator light is on. Many key functions differ from these descriptions in SOLOS command modes BASIC/5, ALS-8, etc. As an aid to learning each key location, we suggest that you keep the keyboard photo, X-26, in view as you study these functions.

7.7.1 Alphanumeric-Punctuation-Symbol Keys

These keys enter the applicable character into the Sol.

Table 7-4. Sol Keyboard Assignments.

KEY #	HEXADECIMAL CODE/CHARACTER GENERATION								
	UNSHIFTED			SHIFTED			CONTROL		
	Hex. Code	Symbol Displayed*		Hex. Code	Symbol Displayed*		Hex. Code	Symbol Displayed*	
		6574	6575		6574	6575		6574	6575
STANDARD KEYS									
ESCAPE	1B	None	None	1B	None	$^{E}_{C}$	1B	None	None
1 | !	31	1	1	21	!	!	01	⌜	$^{S}_{H}$
2 | "	32	2	2	22	"	"	02	⊥	$^{S}_{X}$
3 | #	33	3	3	23	#	#	03	⌟	$^{E}_{X}$
4 | $	34	4	4	24	$	$	04	⍼	$^{E}_{T}$
5 | %	35	5	5	25	%	%	05	⊠	$^{E}_{Q}$
6 | &	36	6	6	26	&	&	06	⍱	$^{A}_{K}$
7 | '	37	7	7	27	'	'	07	⍦	$^{B}_{L}$
8 | (	38	8	8	28	(	(	08	⍬	$^{B}_{S}$
9 |)	39	9	9	29	)	)	09	→	$^{H}_{T}$
Ø |	30	Ø	Ø	20	None	None	00	None	None
– | =	2D	–	–	3D	=	=	0D	Return	Return
^ | ~	5E	^	^	7E	~	~	1E	◱	$^{R}_{S}$
[| {	5B	[	[	7B	{	{	1B	None	None
\ | ¦	5C	\	\	7C	¦		1C	◰	$^{F}_{S}$
] | }	5D	]	]	7D	}	}	1D	◱	$^{G}_{S}$
BREAK	None	None	None	None	None	None	None	None	None
TAB	09	→	$^{H}_{T}$	09	→	$^{H}_{T}$	09	→	$^{H}_{T}$
Q	71	q	q	51	Q	Q	11	⊖	$^{D}_{1}$
W	77	w	w	57	W	W	17	⊣	$^{E}_{B}$
E	65	e	e	45	E	E	15	⊠	$^{E}_{Q}$
R	72	r	r	52	R	R	12	⊖	$^{D}_{2}$
T	74	t	t	54	T	T	14	⊖	$^{D}_{4}$
Y	79	y	y	59	Y	Y	19	⍿	$^{E}_{M}$
U	75	u	u	55	U	U	15	⍲	$^{N}_{K}$
I	69	i	i	49	I	I	09	→	$^{H}_{T}$

Table 7-4. Sol Keyboard Assignments. (Continued)

KEY#	HEXADECIMAL CODE/CHARACTER GENERATION								
	UNSHIFTED			SHIFTED			CONTROL		
	Hex. Code	Symbol Displayed*		Hex. Code	Symbol Displayed*		Hex. Code	Symbol Displayed*	
		6574	6575		6574	6575		6574	6575
STANDARD KEYS (Continued)									
O	6F	o	o	4F	O	O	0F	⊙	S_I
P	70	p	p	50	P	P	10	⊟	D_L
@ | `	40	@	@	60	`	`	00	None	None
RETURN	0D	←	C_R	0D	←	C_R	0D	Return	Return
LINE FEED	0A	Line Feed	Line Feed	0A	Line Feed	Line Feed	0A	Line Feed	Line Feed
CTRL	None	None	None	None	None	None	None	None	None
SHIFT LOCK	None	None	None	None	None	None	None	None	None
A	61	a	a	41	A	A	01	⌐	S_H
S	73	s	s	53	S	S	13	⊖	D_3
D	64	d	d	44	D	D	04	⋁	E_T
F	66	f	f	46	F	F	06	⋀	A_K
G	67	g	g	47	G	G	07	⊞	B_L
H	68	h	h	48	H	H	08	↶	B_S
J	6A	j	j	4A	J	J	0A	Line Feed	Line Feed
K	6B	k	k	4B	K	K	0B	↓	V_T
L	6C	l	l	4C	L	L	0C	⇓	F_F
; | +	3B	;	;	2B	+	+	0B	↓	V_T
: | *	3A	:	:	2A	*	*	0A	Line Feed	Line Feed
DEL | _	7F	None	None	5F	Delete	Delete	1F	⊟	U_S
REPEAT	None	None	None	None	None	None	None	None	None
CTRL	None	None	None	None	None	None	None	None	None
UPPER CASE	None	None	None	None	None	None	None	None	None
SHIFT	None	None	None	None	None	None	None	None	None
Z	7A	z	z	5A	Z	Z	1A	$	S_B
X	78	x	x	58	X	X	18	X	C_N
C	63	c	c	43	C	C	03	⌋	E_X

*See notes at end of this table. Page VII-21.

Table 7-4. Sol Keyboard Assignments. (Continued)

KEY#	HEXADECIMAL CODE/CHARACTER GENERATION								
	UNSHIFTED			SHIFTED			CONTROL		
	Hex. Code	Symbol Displayed*		Hex. Code	Symbol Displayed*		Hex. Code	Symbol Displayed*	
		6574	6575		6574	6575		6574	6575
STANDARD KEYS (Continued)									
V	76	v	v	56	V	V	16	⎍	S_Y
B	62	b	b	42	B	B	02	⊥	S_X
N	6E	n	n	4E	N	N	0E	⊗	S_O
M	60	m	m	40	M	M	0D	Return	Return
, <	2C	,	,	3C	<	<	0C	↓	F_F
. >	2E	.	.	3E	>	>	0E	⊗	S_O
/ ?	2F	/	/	3F	?	?	0F	⊙	S_I
SHIFT	None	None	None	None	None	None	None	None	None
LOCAL	None	None	None	None	None	None	None	None	None
Space Bar	20	None	None	20	None	None	20	None	None
ARITHMETIC PAD KEYS									
−	2D	−	−	2D	−	−	2D	−	−
*	2A	*	*	2A	*	*	2A	*	*
÷	2F	/	/	2F	/	/	2F	/	/
7	37	7	7	37	7	7	37	7	7
8	38	8	8	38	8	8	38	8	8
9	39	9	9	39	9	9	39	9	9
4	34	4	4	34	4	4	34	4	4
5	35	5	5	35	5	5	35	5	5
6	36	6	6	36	6	6	36	6	6
1	31	1	1	31	1	1	31	1	1
2	32	2	2	32	2	2	32	2	2
3	33	3	3	33	3	3	33	3	3
Ø	30	Ø	Ø	30	Ø	Ø	30	Ø	Ø
.	2E	.	.	2E	.	.	2E	.	.
+	2B	+	+	2B	+	+	2B	+	+

KEY#	HEXADECIMAL CODE/CHARACTER GENERATION								
	UNSHIFTED			SHIFTED			CONTROL		
	HEX. Code	Symbol Displayed*		HEX. Code	Symbol Displayed*		HEX. Code	Symbol Displayed*	
		6574	6575		6574	6575		6574	6575
SPECIAL KEYS									
LOAD	8C	None	F_F	8C	None	F_F	8C	None	F_F
MODE SELECT	80	None	None	80	None	None	80	None	None
↑	97	None	None	97	None	None	97	None	None
←	81	None	None	81	None	None	81	None	None
→	93	None	None	93	None	None	93	None	None
↓	9A	None	None	9A	None	None	9A	None	None
HOME CURSOR	8E	None	None	8E	None	None	8E	None	None
CLEAR	8B	None	None	8B	None	None	8B	None	None

#Vertical line between characters indicates dual character key.
*Character generated is displayable and transmittable. “None” means no code is generated or no symbol is displayed. Return is defined in Section 7.7.11, and line feed in Section 7.7.12, on page VII-24.

7.7.2 Space Bar

Pressing the Space Bar, shifted or unshifted, generates the ASCII space code (20) and moves the cursor one space to the right.

7.7.3 Arithmetic Pad Keys

Except for the division symbol key (), these keys enter the applicable character into the Sol. The division symbol key enters a forward slash (/) character. SHIFT does not affect these keys.

The arithmetic pad is useful for entering large amounts of numerical data. Each key in the pad duplicates its corresponding numeric, period (decimal point), dash (minus), plus (addition), asterisk (multiplication) and forward slash (division) key in the "typewriter" group of keys. That is, pressing one of the pad keys does the same thing as pressing its corresponding key in the "type-writer" group.

7.7.4 ESCAPE Key

Pressing ESCAPE, shifted or unshifted, generates the ASCII escape character (1B). The character is displayed.

7.7.5 BREAK Key

Pressing BREAK, shifted or unshifted, forces the SDI output line to a space level for as long as the key is depressed. No character is displayed. (Some communications systems use this feature.)

7.7.6 TAB Key

Pressing TAB, shifted or unshifted, generates the ASCII horizontal tab character (09). The character is displayed.

7.7.7 Control (CTRL) Key

CTRL, shifted or unshifted, is used with alphanumeric, punctuation and symbol keys to initiate functions or generate the characters defined in Table 7-4. Table 7-5 defines the ASCII control characters. The characters in Table 7-5 are not always displayed on the video monitor.

A control sequence (e.g., CTRL plus J, which produces ASCII line feed) requires that CTRL be pressed first and held down while the other key or keys are pressed in sequence.

7.7.8 SHIFT Key and SHIFT LOCK Key/Indicator

The SHIFT key generates no code and is thus not displayed. It is interpreted as a direct internal operation, and when pressed specifically shifts the keyboard from lower case to upper case and from the lower to upper character on dual character keys as on a typewriter. The keyboard remains in upper case as long as SHIFT is held down.

Pressing SHIFT LOCK to turn the indicator light on electronically locks the SHIFT key in the upper case position. Again, no code is generated and no character is displayed. Pressing SHIFT returns the keyboard to lower case and causes the SHIFT LOCK indicator light to go out.

7.7.9 UPPER CASE Key/Indicator

Pressing this key, shifted or unshifted, to turn the indicator light on activates the upper case keyboard function so that all alphabetic characters entered from the keyboard, regardless of SHIFT key status, are transmitted as upper case characters. (Dual character keys, however, do respond to the SHIFT key.) With the indicator light on, the Sol keyboard essentially simulates a teletype (TTY) keyboard.

Pressing UPPER CASE to turn the indicator light off returns the keyboard to normal SHIFT key operation.

Table 7-5. Control Character Symbols and Definitions.

HEXADECIMAL CODE	SYMBOL GENERATED BY		DEFINITION
	6574 Generator	6575 Generator	
06		AK	Acknowledge
07		BL	Bell
08		BS	Backspace
18		CN	Cancel
0D		CR	Carriage Return
11		D1	Device Control 1
12		D2	Device Control 2
13		D3	Device Control 3
14		D4	Device Control 4
7F			Delete
10		DL	Data Link Escape
17		EB	End of Transmission Block
1B		EC	Escape
19		EM	End of Medium
05		EQ	Enquiry
04		ET	End of Transmission
03		EX	End of Text
0C		FF	Form Feed
1C		FS	File Separator
1D		GS	Group Separator
09		HT	Horizontal Tab
0A		LF	Line Feed
15		NK	Negative Acknowledge
00		NU	Null
1E		RS	Record Separator
1A		SB	Substitute
01		SH	Start of Heading
0F		SI	Shift In
0E		SO	Shift Out
02		SX	Start of Text
16		SY	Synchronous Idle
1F		US	Unit Separator
0B		VT	Vertical Tab

7.7.10 LOCAL Key/Indicator

The LOCAL key internally connects the SDI output to the SDI input and disables serial transmission. No character is displayed. Pressing LOCAL, shifted or unshifted, to turn the indicator light on sets Sol for local operation. Keyboard entries are not transmitted, but they are "looped back" to the SDI input for display. That is, Sol is not on "line". Pressing LOCAL to turn the light off ends local operation. This corresponds to the local/line operation of a TTY.

7.7.11 RETURN Key

Pressing RETURN, shifted or unshifted, generates the ASCII carriage return character (0D), which is not displayed, and moves the cursor to the start of the line on which it resided prior to RETURN being depressed. (This is the same action as a TTY carriage return.) RETURN also erases all data in the line to the right of the cursor.

7.7.12 LINE FEED Key

Pressing LINE FEED, shifted or unshifted, generates the ASCII line feed character (0A), which is not displayed, and moves the cursor vertically downward one line. (This is the same action as a TTY line feed.) Line feed action does not erase any data in the line to the right of the cursor.

7.7.13 LOAD Key

The LOAD key character is displayed, but the key is non-functional with CONSOL and SOLOS. The code generated by this key is 8C, and it may be used by a program to meet a specific need.

7.7.14 REPEAT Key

The REPEAT key generates no character and is consequently not displayed. Pressing REPEAT, shifted or unshifted, and another key at the same time causes the other key to repeat at an approximate rate of 15 times per second as long as both keys are held down. Pressing REPEAT at the same time as UPPER CASE performs a restart. See Section 7.5.2 on page VII-13.

7.7.15 MODE SELECT Key

Pressing this key, shifted or unshifted, generates the code 80 and causes Sol to enter the command mode.

7.7.16 CLEAR Key

Pressing CLEAR, shifted or unshifted, erases the entire screen and moves the cursor to its "home" position (upper left corner of the screen).

7.7.17 Cursor Control (HOME CURSOR and Arrows) Keys

Five keys control basic cursor movement. They are HOME CURSOR and the four keys with arrows. None are affected by SHIFT status, and none are displayed or transmitted.

Pressing HOME CURSOR moves the cursor to its home position--the first character position in the upper left corner of the screen.

To move the cursor up, down, left or right, press the applicable "arrow" key. Each time you press a key the cursor moves one unit in the direction you wish--one space horizontally or one line vertically. These keys may be used with REPEAT. The cursor will not move across any margin of the screen with these four keys.

7.8 BASIC OPERATIONS

7.8.1 Switching From Terminal To Command Mode

To switch from terminal to command mode, simply press the MODE SELECT key. Sol enters the command mode, issues a prompt character (**>**) and waits for a command input.

7.8.2 Switching From Command To Terminal Mode

To switch from command to terminal mode, press UPPER CASE, TERM and RETURN in that order. Sol enters the terminal mode and all keyboard data will be sent to the SDI output and ail data received (including "looped back" data) will appear on the screen.

7.8.3 Entering Commands In The Command Mode

The various commands for CONSOL and SOLOS are described in Section IX of this manual and the SOLOS Users' Manual respectively.

You can place more than one command on the screen. For each command, use the arrowed cursor control keys to position the cursor at the start of a new line and begin the new command line with a prompt character (**>**).

A command is executed when you press the RETURN key, and all characters on the line to the left of the cursor are interpreted as the command. This means that if more than one command line is on the screen, you can execute any one of them as follows: position the cursor with the arrowed cursor control keys to the right of the desired command and press RETURN.

Should you make a mistake when entering a command, there are two ways to correct it:

(Paragraph 7.8.3 continued on Page VII-26.)

1. If you see the error immediately (the error is to the immediate left of the cursor), press the DEL key (unshifted) to erase the mistake. Then make the correction.

2. If the error is more than one character position to the left of the cursor, use the arrowed cursor control keys to position the cursor over the mistake. Then make the correction

7.8.4 Keyboard Restart

To perform a keyboard restart, press the UPPER CASE and REPEAT keys at the same time. This key combination performs the same function as a power on initialization or setting the RST switch to ON. Use the keyboard restart to return to SOLOS/CONSOL from 1) a program which does not recognize the MODE SELECT key or 2) a program that is stuck in an endless loop.

7.9 Sol-PERIPHERAL INTERFACING

7.9.1 Audio Cassette Recorders

Your Sol is capable of controlling one or two recorders. The interconnect requirements for one recorder were previously covered in Paragraph 7.4.1 in this section.

Since the Sol has only one audio input and one audio output jack, however, the interconnect requirements for two recorders are somewhat different than for one.

You will need two "Y" adapters, one to feed the single Sol audio output to the AUXILIARY input of two recorders and the other to feed the MONITOR output of two recorders to the single Sol audio input. (If you intend to use the Audio In and Out cables described in Paragraph 7.4.1 in this section, miniature phone jack-to-two miniature phone plug adapters are required.) Since the recorder outputs are most likely unbalanced, we also suggest that you incorporate 1000 ohm resistors in the MONITOR adapter as shown in Figure 7-5 on Page VII-29. Figure 7-5 also illustrates, in schematic form, how to connect two recorders to your Sol.

When using two recorders you may read or write to both under program control as well as read one tape while writing on the other. If you intend to read one tape while writing on the other, however, you may have to disconnect the MONITOR plug from the write unit, with the need for disconnect being determined by the recorder design. The MONITOR disconnect must be made if the recorder has a

"monitor" output in the record mode. (Panasonic RQ-413S and RQ-309DS do, for example.)

NOTE 1

Recorders on which the "monitor" jack is labeled MONITOR usually provide a monitor output in the record mode. If the jack is labeled EAR or EARPHONE, the recorder usually does not provide a monitor output in the record mode.

NOTE 2

To determine if your recorder provides a monitor output in the record mode, install a blank tape, plug earphone into "monitor jack and microphone into MICROPHONE jack, set recorder controls to record, and speak into microphone while listening with the earphone. If you hear yourself through the earphone, your recorder does provide a monitor output in the record mode.

Write Operations. Other than placing the recorder(s) in the record mode, loading the cassette(s) and making sure that the head(s) is on tape (not leader), no manual operations are needed to write on tape.

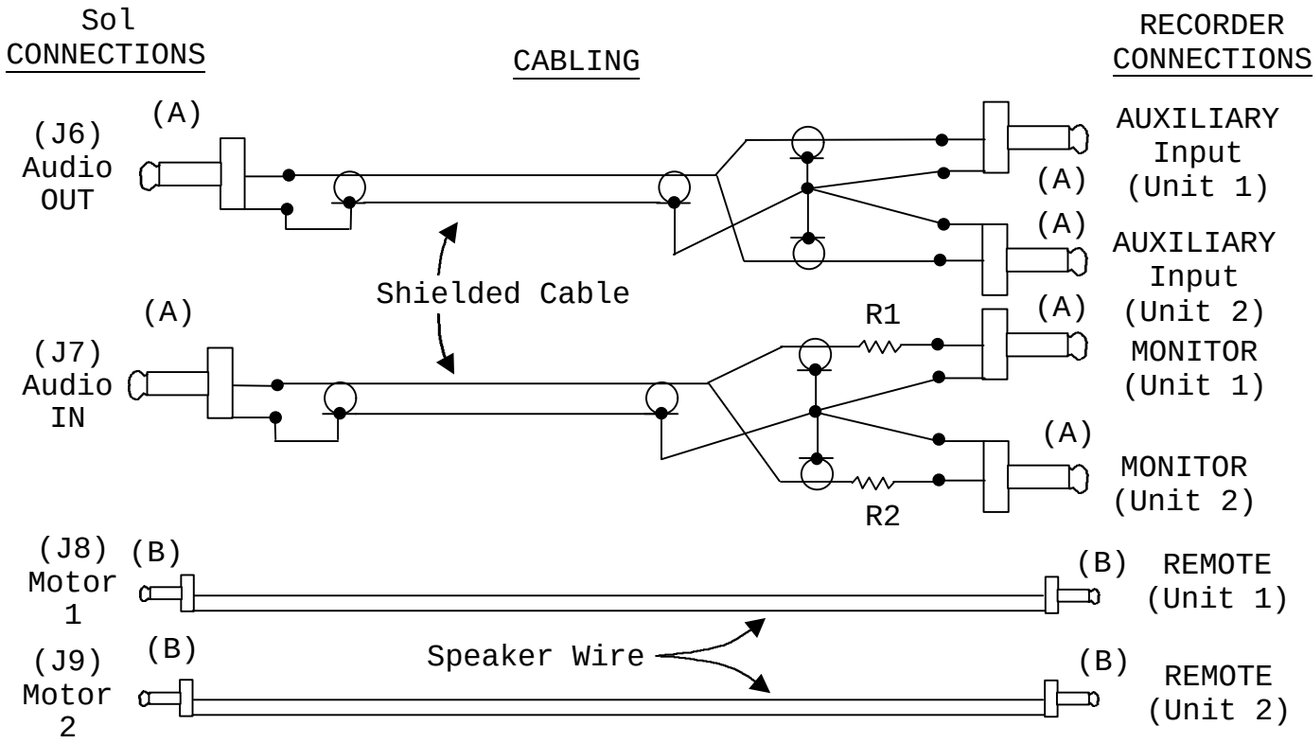
In the case of two recorders, however. Unit 1 and 2 must be specified in the SAVE command in order to select the desired recorder. A default selects Unit 1. Refer to your SOLOS Users' Manual for instructions on how to use tape commands.

Read Operations. In order to read a specific file on tape, you must start the tape at least two seconds ahead of that file. This delay allows the Sol audio cassette interface circuitry and the recorder playback electronics to stabilize after power is turned on. Since all file searches are in the forward direction, the simplest approach is to fully rewind the cassette(s) before a read operation unless you know that the file of interest is advanced at least two seconds. (See Paragraph 7.4.3, Step 21 for instructions on how to rewind the tape.)

For a read operation, proceed as follows:

1. Load cassette(s) as just described.

2. If only one recorder is used, set its volume control at midrange. With two recorders, set both volume controls at their high end.



(A) Miniature Phone Plug
(B) Subminiature Phone Plug
R1 = R2 = 1000 ohms, 1/4 watt

Figure 7-5. Connecting Sol to two cassette recorders

3. Set recorder(s) tone control(s) at the top of the range (maximum treble).

4. Set PLAY control(s) for playback mode.

5. Give Sol the GET or "GET, then Execute" command as appropriate. (Refer to your SOLOS Users' Manual for instructions on how to use tape commands.)

7.9.2 Serial Data Interface (SDI)

The Sol Serial Data Interface (J1) is capable of driving an RS-232 device, such as a modem, or a current loop device, such as the ASR33 TTY.

S3 (Baud Rate) and S4 (Parity, Word Length, Stop Bits and Full/Half Duplex) are used to select the various serial interface options as described in Paragraphs 7.5.7 through 7.5.11 in this section.

Set S3 switches to select the Baud rate required by the modem or current loop device. (Standard 8-level TTY's operate at 110 Baud, S3-2 ON and all other S3 switches OFF.) For standard 8-level TTY's and most modems, set all S4 switches OFF. (This selects eight data bits, two stop bits, no parity bit and full duplex operation for the SDI.

Figures 7-6 and 7-7 show examples of current loop and modem interconnections to the Sol SDI connector (Jl). The ASR33 TTY is used to illustrate a current loop interconnect, and the Bell 103 modem is used to illustrate a modem interconnect.

When operating in the terminal mode and full duplex. Sol keyboard data is transmitted out on Pin 2 of Jl and date received on Pin 3 of Jl is displayed on the video monitor. In the command mode, SOLOS set in and out commands can be used to channel output data and input data through the SDI. (Refer to your SOLOS Users' Manual for instructions on how to use the set commands.)

In either mode, the LOCAL key directly controls the SDI. With the LOCAL indicator light on, received data is ignored and keyboard data is not transmitted. It is, however, looped back for display on the video monitor. With the LOCAL light off, received data is displayed and keyboard data is transmitted but not displayed unless it is echoed back.

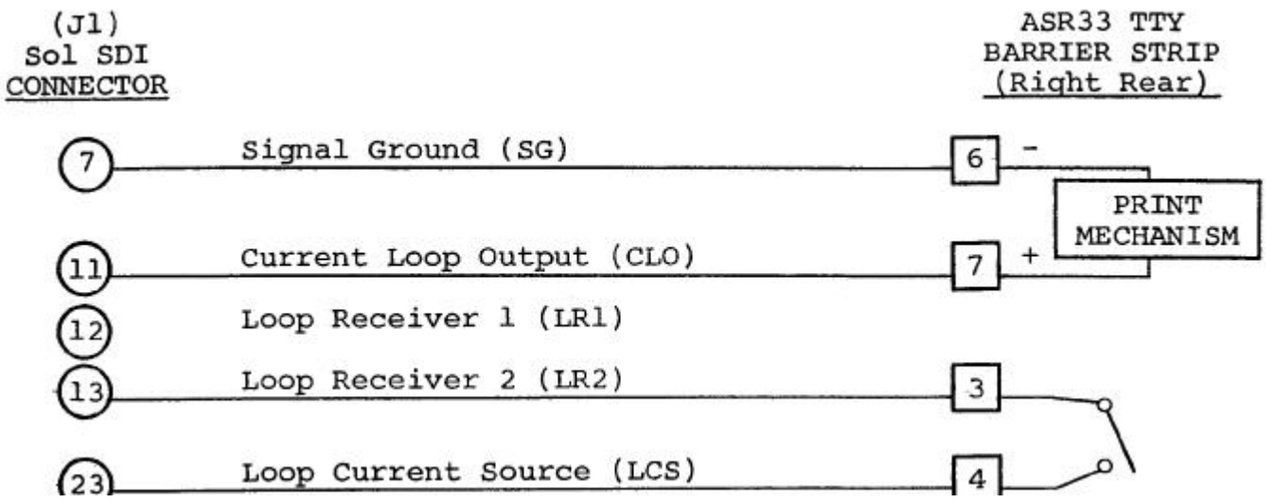
7.9.3 Parallel Data Interface (PDI)

The Sol Parallel Data Interface (J2) is used to drive parallel devices such as paper tape readers/punches and line printers. It provides eight output data lines, eight input data lines, four handshaking signals and three control signals. The latter allow up to four devices to share the PDI connector. (See Appendix VII for J2 pinouts.)

The port address for parallel input and output data is FD (hexadecimal), and the control port address for the PDI is FA (hexadecimal). PXDR is available at bit 2 of port FA. When this bit is set to 0, the external device is ready to receive a byte of data. PDR is available at bit I of port FA, with 0 indicating the external device is ready to send a byte of data. Parallel Unit Select (PUS) is controlled by bit 4 of port FA. The input and output enable lines are available for tri-stating an external two-way data bus.

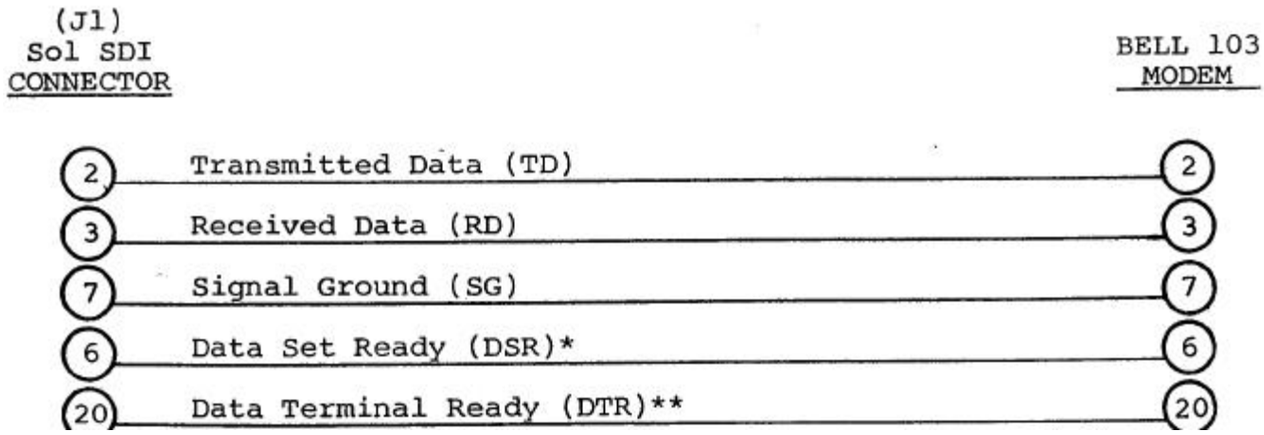
Use of the three control signals is optional and is unnecessary when only one device is connected to the PDI connector.

(Paragraph 7.9.3 continued on Page 31.)



CAUTION: PINS 1 AND 2 ON TTY BARRIER STRIP CARRY 120 V ac LINE VOLTAGE.

Figure 7-6. Connecting Sol SDI to current loop device such as TTY.



*Available at bit 1 of port F8. Terminal mode software (SOLOS et al) does not use this signal and transmits data whether or not the modem is ready.

**Sol is wired so that DTR indicates a ready condition whenever power is on.

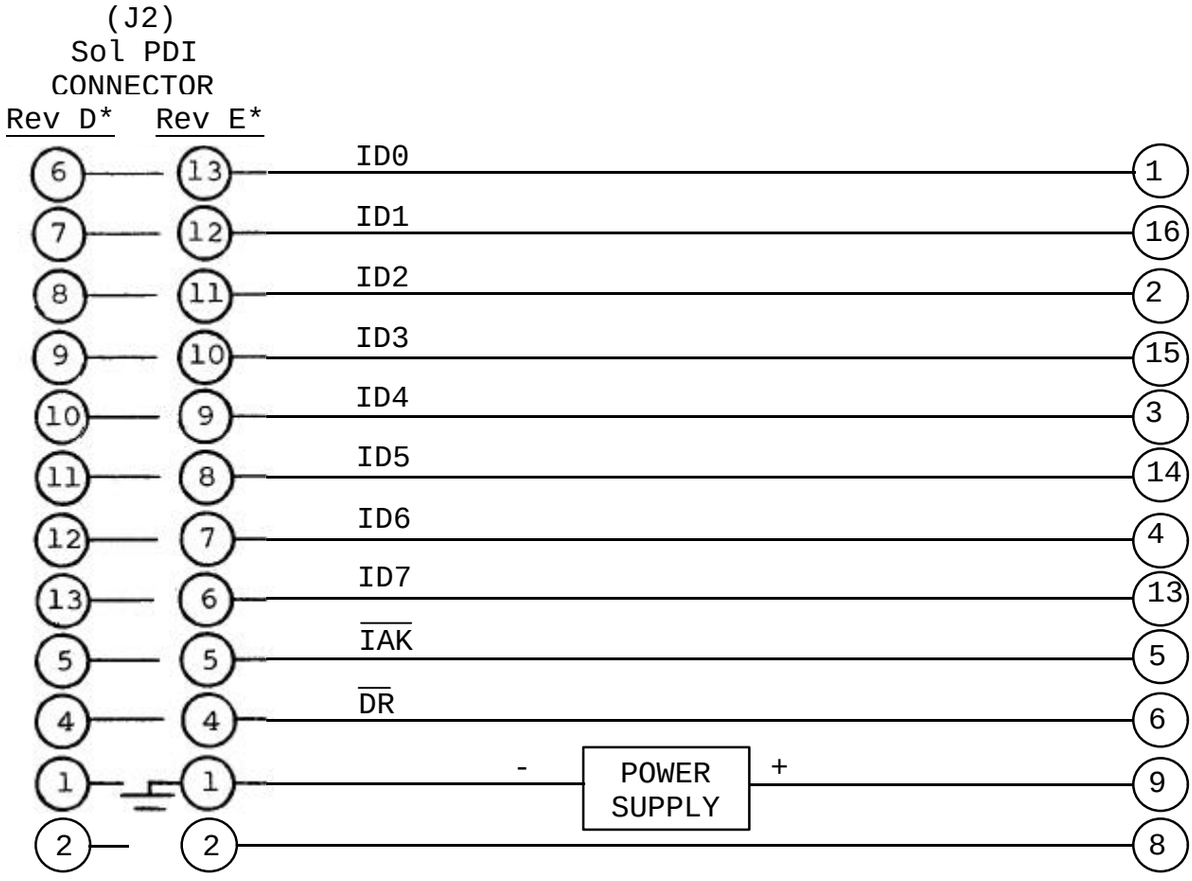
Figure 7-7. Connecting Sol SDI to communications modem.

In Figure 7-8, the Oliver OP80 Manual Paper Tape Reader is used to illustrate a typical PDI interconnect.

7.10 CHANGING THE FUSE

Sol is protected with a 3.0 amp Slo-Blo fuse housed on the rear panel (see Figure 7-1 on Page VII-6). To remove the fuse, turn Sol off, disconnect power cord, turn fuse post cap one quarter turn counterclockwise, pull straight out and remove fuse from cap.

To install a fuse, insert fuse in cap, push in and turn one-quarter turn clockwise.



NOTE: +5 V dc is not available at J2. The use of an external +5 V dc power supply with its ground connected to Pin 1 of J2 (Sol chassis ground) is recommended.

*Sol-PC Board

Figure 7-8. Connecting Sol PDI to parallel device.

VIII THEORY OF OPERATION

8.1 INTRODUCTION VIII-1

8.2 OVERVIEW VIII-1

8.3 BLOCK DIAGRAM ANALYSIS, Sol-PC VIII-3
8.3.1 Functional Elements And Their Relationships VIII-3
8.3.2 Typical System Operation VIII-5
Keyboard Data Entry and Display VIII-5
SDI/UART Transfer and Display VIII-6

8.4 POWER SUPPLY CIRCUIT DESCRIPTION VIII-6

8.5 Sol-PC CIRCUIT DESCRIPTIONS VIII-8
8.5.1 CPU and Bus VIII-8
8.5.2 Memory and Decoder VIII-14
8.5.3 Input/Output VIII-18
8.5.4 Display Section VIII-22
8.5.5 Audio Tape I/O VIII-33

8.6 KEYBOARD VIII-38
8.6.1 Block Diagram Analysis VIII-38
8.6.2 Circuit Description VIII-39

TABLES AND ILLUSTRATIONS

TABLE	TITLE	PAGE
8-1	Port Decoder (U35 & U36) Outputs and Their Functions	VIII-17

FIGURE	TITLE	PAGE
8-1	Clock Generator Timing	VIII-11
8-2	Example of uppercase character (I) display	VIII-24
8-3	Example of lowercase character (p) display	VIII-24
8-4	Video Display timing	VIII-27
8-5	6574 Character Generator ROM pattern	VIII-30
8-6	6575 Character Generator ROM pattern	VIII-31

8.1 INTRODUCTION

This section concerns itself with the hardware aspects of the Sol Terminal Computer$^{T.M.}$. It specifically deals with the operation of the power supply and the logic associated with the Sol-PC and keyboard. Descriptions of software and the operation of the circuitry contained in the multitude of integrated circuits (IC's) used in the Sol fall outside the scope of this section. In some cases, references to other publications or sections in this manual are provided when it is felt that additional information will contribute to a better understanding of how Sol operates. Should the reader wish to delve further into the operation of a specific IC, we suggest that he study the appropriate data sheet for that IC.

The section begins with an overview of the Sol design. A block diagram analysis then provides the reader with an understanding of the relationship between the functional elements of the Sol-PC. This analysis sets the stage for detailed descriptions of the circuitry that makes up these elements. The section concludes with a block diagram analysis and circuit description of the keyboard.

8.2 OVERVIEW

The Sol Terminal Computer$^{T.M.}$ as the name implies, is both a terminal and computer. It is designed around the S-100 bus structure used in other 8080 microprocessor-based computers and incorporates all of the circuitry needed to perform either function. In essence, Sol combines a central processor unit (CPU) with several S-100 peripheral modules--memory, keyboard input interface (including the keyboard), video display output interface plus audio cassette tape, parallel, and serial input/output (I/O) interfaces. Sol-20 also includes a five-slot backplane board for adding other memory and I/O modules that are compatible with the S-100 bus.

An 8080 microprocessor (the CPU) is the "brain" of the Sol. It controls the functions performed by the other system components, obtains (fetches) instructions stored in memory (the program), accepts (inputs) data, manipulates (processes) data according to the instructions and communicates (outputs) the results to the outside world through an output port. (For information on 8080 operation, refer to the "Intel® 8080 Microcomputer Systems User's Manual.")

As shown in the Sol Simplified Block Diagram on Page X-24 in Section X, data and control signals travel between the CPU and the rest of the Sol over three buses: 1) a 16-line Address Bus, 2) an eight-line Bidirectional Data Bus, and 3) a 28-line Control Bus which is interfaced to the CPU with support logic circuitry. (Note that the use of a bidirectional data bus permits eight lines to do the work of 16, eight input and eight output.) These three buses account for the bulk of the S-100 Bus which connects the Sol to expansion memory and I/O modules.

In the Sol-20, the S-100 Bus structure takes the form of a five-slot backplane board. It consists of a printed circuit board with 100 lines (50 on each side) and five edge connectors on which like-numbered pins are connected from one connector to another. Functionally, the Sol version of the S-100 Bus is comprised of:

1. Sixteen output address lines from the CPU which are input to all external memory and I/O circuitry. (Direct memory access (DMA) devices must generate addresses on these lines for DMA transfers.)

2. Eight data input/output lines that transfer data between external memory and I/O devices and the CPU or DMA devices. (These eight lines are paralleled with eight other bus lines.)

3. Eight status output lines from the CPU support logic: Memory and I/O devices use status signals to obtain information concerning the nature of the CPU cycle. (DMA devices must generate these signals for DMA transfers.)

4. Nine processor command and control lines: Six of these are output signals from the CPU support logic; three of them are input signals to the CPU support logic from memory and I/O devices. (In a DMA transfer, the DMA device assumes control of these lines.)

5. Five disable lines: Four of these are supplied by a DMA device to disable the tri-state drivers on the CPU outputs during DMA transfers. The fifth is a derivative of the DBIN output from the CPU, and it is used to disable any memory addressed in Page ft. Use of this disable is optional with a jumper.

6. Two input lines to the CPU support logic which are used for requesting a wait period. One is used by memory and I/O devices and the other by external devices.

7. Six power supply lines which supply power to expansion modules.

8. Three clock lines.

9. Four special purpose signal lines.

10. Thirty-one unused lines.

Definitions for each S-100 Bus line, as used in the Sol, are provided on Pages AVII-3 through AVII-6 in Appendix VII.

In addition to the S-100 Bus structure, Sol also uses an eight-line keyboard input port, an eight-line parallel input port,

an eight-line parallel output port, an eight-line sense switch logic input port, and a unidirectional eight-line internal data bus.

The use of a unidirectional (input) data bus accommodates Sol's internal low-drive memory and I/O devices that do not meet the heavy drive requirement of the bidirectional data bus. The low-drive requirement of the internal bus also allows using the tri-state capabilities of the UART's (Universal Asynchronous Receiver/Transmitter) in the serial and audio cassette I/O circuits without additional drivers.

All CPU data and address lines are buffered through tri-state drivers to support a larger array of memory and I/O devices than would otherwise be possible with the 8080 output drive capability. Data input to the CPU is selected by a four-input multiplexer from the Keyboard Port, Parallel Port, Bidirectional Data Bus and Internal Data Bus. The Internal Data Bus is the source of all data input to the CPU from Sol's internal memory, the serial interface and the cassette interface. The Bidirectional Data Bus is the source of all data fed to memory and I/O, both internal and external. It is also the source of data input to the CPU from eight internal sense switches as well as from external memory and I/O.

8.3 BLOCK DIAGRAM ANALYSIS, Sol-PC

8.3.1 Functional Elements And Their Relationships

As can be seen in the Sol block diagram on Page X-24 in Section X, timing signals for Sol are derived from a crystal controlled oscillator that produces a "dot clock" frequency of 14.31818 MHz. (This frequency, four times that of the NTSC color burst, provides compatibility with color graphics devices.) The dot clock is applied directly to the Video Display Generator circuit and divided in the Clock Generator to provide ϕ1, ϕ2 and CLOCK. CLOCK synchronizes all control inputs to the 8O8O; ϕ1 and ϕ2 are the nonoverlapping, two phase clocks required by the 8O8O.

Memory internal to the Sol is divided between 2K of ROM (Read Only Memory), 1K of System RAM (Random Access Read/Write Memory) and 1K of Display RAM. The ROM permanently stores the instructions that direct the CPU's activities. (To enhance Sol's versatility, this particular memory is on a plug-in "personality module". Thus, Sol can be easily optimized for a particular application by plugging in a personality module that contains a software control program designed for the task. The CONSOL and SOLOS programs, which are described in Section IX, are examples of such personality modules.) Display RAM stores data for display on a video monitor, and the System RAM provides temporary storage for programs and data. All memories are addressed on the Address Bus (ADR0-15) and, except for the Display RAM, input data to the CPU on the Internal Data Bus (INT0-7). Data entry into both RAM's is done on the Bidirectional Data Bus (DIO0-7).

As can be seen, Sol's internal memory consists of four contiguous 1024-byte pages. There are two pages (C0 and C4, hexadecimal or hex) of ROM, with Page C0 at hex addresses C000 through C3FF and Page C4 at hex addresses C400 through C7FF. System RAM (Page C8) is at hex addresses C800 through CBFF, and Display RAM (Page CC) is at hex addresses CC00 through CFFF.

The six high order bits of the address are decoded in the Address Page and I/O Port Decoder to supply the required four memory page selection signals. The I/O Port Decoder portion of this circuit decodes the eight high order address bits to provide outputs that control Data Input Multiplexer switching, Data Bus Driver enablement and I/O port selection.

The video display section consists of the Video Display Generator and Display RAM. The RAM is a two-port memory, with the CPU having the higher priority. Screen refresh circuitry in the Video Display Generator controls the second port to call up data as needed for conversion by a character generator ROM into video output signals. Other circuitry generates horizontal and vertical sync and blanking signals as well as cursor and video polarity options.

A 1200 Hz signal, extracted from dot clock by a divider in the Video Display Generator, drives the Baud Rate Generator. This generator supplies the receive and transmit clocks for the serial data interface (SDI/UART) and provides ail frequencies required for Baud rates between 75 and 9600. It also supplies clock signals to the Cassette Data Interface (GDI).

A UART controls data flow through the Serial Data Interface (SDI/UART) and provides for compatibility between the Sol and a data communications system, be it RS-232 standard or a 20 ma current loop device. In the transmit mode, parallel data on the Bidirectional Data Bus is converted into serial form for transmission. Received serial data is converted in the receive mode into parallel form for entry into the CPU on the Internal Data Bus. SDI/UART status is also reported to the CPU on the Internal Data Bus. The SDI/UART channel is enabled by the port strobe from the Address Page and I/O Port Decoder.

Circuitry within the GDI derives timing signals from clocks supplied by the Baud Rate Generator. The Cassette Data UART functions to 1) convert parallel data on the Bidirectional Data Bus into serial audio signals for recording on cassette tape, and 2) convert serial audio signals from a cassette recorder into parallel data for entry into the CPU from the Internal Data Bus. Note that Cassette Data UART status is also reported to the CPU on the Internal Data Bus. Again, a UART performs the necessary parallel-to-serial and serial-to-parallel conversions. Other GDI circuitry performs the needed digital-to-audio and audio-to-digital conversions and provides the signals that allow motor control for two recorders. As with the SDI/UART, the Cassette Data UART is enabled by a port strobe from the Address Page and I/O Port Decoder.

Output data from the CPU that is channeled through the Parallel Port (PP) is latched from the Bidirectional Data Bus by the parallel strobe from the Address Page and I/O Port Decoder. This data is made available at P2, the PP connector. Parallel input data (PID0-7) on P2, however, is fed directly to the Data Input Multiplexer for entry into the CPU.

As can be seen, keyboard data (KBD0-7) from J3 is also fed directly to the Data Input Multiplexer. The keyboard data ready flag, though, is input to the CPU on the internal data bus.

The remaining internal source of data input to the CPU is the Sense Switch Logic, with the data being input on the Bidirectional Data Bus. This is an eight-switch Dual Inline Package (DIP) array that lets the CPU read an eight-bit word when it issues the sense switch strobe via the Address Page and I/O Port Decoder. The sense switch data source is available to interact with the user's software.

CPU Support Logic accepts six control outputs from the CPU, status information from the CPU's data bus and control signals from the Control Bus. It controls traffic on the data buses by generating signals to 1) select the type of internal or external device (memory or I/O) that will have bus access and 2) assure that the device properly transfers data with the CPU.

8.3.2 Typical System Operation

Basic Sol system operation is as follows: The CPU fetches an instruction and in accordance with that instruction issues an activity command on the Control Bus, outputs a binary code on the Address Bus to identify the memory location or I/O device that is to be involved in the activity, sends or receives data on the data bus with the selected memory location or I/O device, and upon completion of the activity issues the next activity command.

Let's now look at some typical operating sequences.

Keyboard Data Entry and Display. Assume the "A" and SHIFT keys on the keyboard are pressed. The keyboard circuitry converts the key closures into the 7-bit ASCII (American Standard Code for Information Interchange) code for an "A" {1000001) and sends a keyboard-data-ready status signal to the CPU on the Internal Data Bus. The monitor program in ROM repetitively "looks" for the status signal. When it finds this signal the program enters its keyboard routine and enables the transfer by switching the Data Input Multiplexer to the keyboard bus via the Address Page and I/O Port Decoder.

Following program instructions, the CPU addresses the Display RAM on the Address Bus to determine where the next character is to appear on the screen. It then stores the ASCII code for the "A" at the appropriate location in the Display RAM and adds one to the cursor position in readiness for the next character. (Addressing is

done over the Address Bus; cursor position and the "A" enter the Display RAM on the Bidirectional Data Bus.) The CPU is now finished with the transfer, and will issue the next activity command.

When the refresh control circuitry calls up (addresses) the "A" from the Display RAM, the character generator ROM decodes the ASCII-coded "A" that is input from the Display RAM and generates the "A" dot pattern (see Figure 8-5 and 6) in parallel form. The ROM output is serialized into a video signal and combined with a composite sync signal to provide an Electronic Industries Association (EIA) composite video signal for display on an external video monitor.

SDI/UART Transfer and Display. A data transfer through the SDI/UART is similar to a keyboard entry, but data can be transferred in either direction.

Assume the SDI/UART wants to transfer an "A" from a modem to the CPU for display on a video monitor. The ASCII code for the "A", received in serial form from the modem on the serial data input of the SDI connector (Jl), is fed to the SDI/UART. In the receiver section of the UART the serial data is converted into parallel form and placed in the UART's output register. The UART also sends a "received data ready" status signal to the CPU on the Internal Data Bus. When the program in ROM checks and finds the status signal, the program enters the SDI routine, and enables the transfer by switching the Data input Multiplexer to the Internal Data Bus. The "A" enters the CPU on the Internal Data Bus and is sent to the Display RAM on the Bidirectional Data Bus. Operations involved in displaying the "A" are identical to a keyboard entry.

Now assume the CPU wants to send an "A" to the SDI/UART for transmission. The CPU, under program control, sends the SDI/UART status input port strobe via the Address Page and I/O Port Decoder to the UART. In turn, the UART responds with its status on the Internal Data Bus. Assuming the UART is ready to transmit, the CPU places the ASCII code for the "A" on the Bidirectional Data Bus and sends the SDI/UART data output port strobe which loads the Bidirectional Data Bus content into the UART's transmitter section. The "A" is serialized by the UART and sent out the transmitted data pin of Jl.

8.4 POWER SUPPLY CIRCUIT DESCRIPTION

Refer to the Sol-REG and Sol-10 or Sol-20 Power Supply Schematics in Section X, Pages X-12, 13 and 14.

The Sol power supply consists of the Sol-REG regulator and either the Sol-10 or Sol-20 power supply components. An 8 V dc unregulated supply in the Sol-20 is the only difference between the two. We will, therefore, describe the complete Sol-10 supply followed by the unregulated 8 V dc supply in the Sol-20.

Fused primary power is applied through S5 to T1 (T2 in the Sol-20). FWB1, a full-wave bridge rectifier, is connected across the 8-volt secondary (green leads). The rectified output is filtered by C8 and applied to the collector of Q1. Q1, a pass transistor, is driven by Q2, with the two connected as a Darlington pair. The output of Q1 is connected to R1 which serves as an overload current sensor.

An overload current (approximately 4 amps) increases the voltage drop across R1. The difference is amplified in one-half of U2 (an operational amplifier) and the output on pin 7 turns Q3 on. Q3 in turn "steals" current from Q1-Q2 and diverts current from the output on pin 1 of U2. This in effect turns the supply off to reduce the current and voltage. Note that the circuit is not a constant current regulator since the current is "folded back" by R6 and R8. The current is reduced to about 1 amp as the output voltage falls to zero.

Divider network R11 and R12, which is returned to -12 volts, senses changes in the output voltage. If the output voltage is 5 volts, the input on pin 2 of U2 is at zero volts. U2 provides a positive output on pin 1 if pin 3 is more positive than pin 2 and a negative output for the opposite condition.

When the output voltage falls below 5 volts, pin 2 of U2 goes more negative than pin 3. This means pin 1 of U2 goes positive to supply more current to the base of Q1. The resulting increase in current to the load causes the output voltage to rise until it stabilizes at 5 volts. Should the output voltage rise above 5 volts, the circuit operates in a reverse manner to lower the voltage.

Protection against a serious over-voltage condition (more than 6 volts) is provided by SCR1, D1, R2, R13, R14 and C8. Zener diode, (D1), with a 5.1 zener voltage, is connected in series with R13 and R2. When the output voltage exceeds about 6 volts, the resulting voltage drop across R2 triggers SCR1 to short the foldback current to ground. Since the overload current circuit is also working, the current through SCR1 is about 1 amp. Once the current is removed, this circuit restores itself to its normal condition; that is, SCR1 turns off. R13, R14 and C8 serve to slightly desensitize the circuit so that it will not respond to small transient voltage spikes.

Bridge rectifier FWB2, connected across the other T1 secondary, supplies +12 and -12 V dc. The positive output of FWB2 is filtered by C5 and regulated by IC regulator U1. The negative output is filtered by C4 and regulated by U3. Shunt diodes D3 and D4 protect U1 and U3 against discharge of C6 and C7 when power is turned off. (Note that should the -12 volt supply short to ground, the +5 volt supply turns off by the action of U2.

Unregulated -16 and +16 V dc, at 1 amp, from the filtered outputs of FWB2 are made available on terminals X6 and X5. These are not used in the Sol-10, but they are supplied to the backplane board in the Sol-20 to drive S-100 Bus modules.

In the case of the Sol-20, the power transformer (T2) has an additional 8-volt secondary winding and a third bridge rectifier (FWB3) to supply +8 V dc at 8 amps. The output of FWB3 is filtered by C9 and controlled by bleeder resistor R13. Again, this voltage is supplied to the backplane board in the Sol-20.

Sol-20 also includes a cooling fan powered by the AC line voltage.

8.5 Sol-PC CIRCUIT DESCRIPTIONS

8.5.1 CPU and Bus

Refer to the CPU and Bus Schematic in Section X, Page X-15.

A crystal, two inverter sections in U92 and four D flip-flops (U90) and associated logic make up the Clock Generator.

The two U92 sections function as a free-running oscillator that runs at the crystal frequency of 14.31818 MHz. R133 and R134 drive these two sections of U92 into their linear regions, and C61 and 64 provide the required feedback loop through the crystal. U77, a permanently enabled tri-state non-inverting buffer/amplifier, furnishes a high drive capability.

This fundamental clock frequency is fed directly to the Video Display Generator and to the clock inputs of U90. U90 is a four-stage register connected as a ring counter that is reset to zero when power is applied to the Sol. This reset is accomplished with D8, R104 and C39.

The bits contained in the ring counter shift one to the right with every positive-going clock transition, but the output of the last stage is inverted or "flipped" before being fed back to the input In a simple four-stage "flip-tail" ring counter, the contents would progress from left to right as follows: 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000--on the first through eighth clocks respectively. The hypothetical counter would go through eight states, dividing the clock by eight.

The Sol counter, however, is a modified flip-tail ring counter that can be configured to divide by one of three divisors--5, 6 or 7. This is made possible by using a two-input NAND gate (U91) in the feedback path and three jumper options (no jumper, D-to-C and D-to-E) to alter the feedback path. Let's see how it works.

Sol is normally configured with the D-to-E jumper installed to meet the clock requirements of the 8080A CPU. With this jumper installed, the outputs of the third and fourth U90 stages are applied to pins 9 and 10 of U91. Assuming U90 is reset to zero, pin 8 of U91 is high, and on the first clock pulse the counter contents change to 1000. (Refer to 2.045 MHz Clocks portion of Figure 8-1 on Page VIII-11.) Pin 8 of U91 cannot change until the fourth state (1111), at which time it goes to zero. On the fifth clock pulse the counter changes to 0111. Again, pin 8 of U91 cannot change from zero until one of its inputs changes. As shown in Figure 8-1, the third U90 stage (C) changes on the seventh clock. The counter now stands at 0001, and on the eighth clock the counter flips to 1000 and the count cycle repeats. The pattern is thus 1000, 1100, 1110, 1111, 0111, 0011, 0001. U90 consequently goes through seven states. We have a 3.5-stage counter that divides DOT CLOCK by seven to supply a 2.045 MHz output.

With no jumper installed, pin 10 of U91 is pulled high by R105, and U91 operates as a simple inverter for feeding back the output of the third U90 stage. In effect we have a three-stage counter that operates in a similar manner to that described in the preceding paragraph. It gees through six states (100, 110, 111, 011, 001, 000) to divide DOT CLOCK by six which produces a 2.386 MHz output. The timing for this option is also shown in Figure 8-1.

Let's now put the D-to-C jumper in. The feedback in this case is the NAND combination of the outputs from the second (B) and third (C) U90 stages. This gives us a 2.5-stage counter that divides DOT CLOCK by five. As can be determined from the 2.863 MHz portion of Figure 8-1, the counter has five states with this option, and the count pattern is: 100, 110, 111, 011, 001.

Outputs from U90 are applied to the logic comprised of the remaining three sections in U91. This logic and the A-to-B jumper option permits extracting clock pulses of varying widths and relationships to each other from various points within the counter. We extract two clock signals: ϕ1 on pin 6 of U91 and ϕ2 on pin 11 of U91. (The ability to select the frequency and pulse width for ϕ1 and ϕ2 permits the use of either the 8080A, 8080A-1 or 8080A-2 CPU for U105. The "A" version is the slowest speed unit, the "A-2" has an intermediate speed, and the "A-l" is the fastest.) Let's now see how the pulse width of ϕ1 and ϕ2 are determined.

ϕ1 on pin 6 of NAND gate U91 is low only when its two inputs are high, and this happens only when there is a 1 in the second and fourth stages of U90. This occurs during the time between the fourth and sixth fundamental clocks for 2.04 MHz operation--the fourth and fifth clocks for 2.38 MHz and 2.86 MHz. Keeping in mind that the fundamental clock period is 70 nsec, it is readily seen that the low frequency pulse train on pin 6 of U91 has a pulse width of 140 nsec and the two higher frequency pulse trains have a pulse width of 70 nsec. (Refer to Figure 8-1 on Page VIII-11.)

The A-to-B jumper is installed when the 8080A or 8080A-1 CPU is used in the Sol. Note that the output (ϕ2) on pin 11 of NAND gate U91 is low only when the output on pin 3 of NOR gate U91 is high. (This section in U91 is actually a two-input NAND gate which is functionally the same as a two-input NOR gate.) Pin 3 of U91, with the A-to-B jumper in, is high when either the second (B) or third (C) U90 stage is at zero. As shown in Figure 8-1, this occurs between the sixth and tenth DOT CLOCKS, or 280 nsec (4 x 70 nsec), for 2.04 MHz operation. For 2.863 MHz, it occurs between the fifth and eighth DOT CLOCKS for 210 nsec. The section of NAND gate U91 with its output on pin 11 inverts the output on pin 3 of U91 and introduces a slight delay to insure there is no overlap between ϕ1 and ϕ2.

With the A-to-B jumper out, pin II of U91 is low only when the second stage (B) of U90 is at zero. At 2.386 MHz, this occurs between the fifth and eighth DOT CLOCKS for 210 nsec. This configuration is used for the 8080A-2 CPU.

In summary, we have two non-overlapping pulse trains which represent the 01 and 02 clocks required by the 8080 CPU, and the pulse widths of these two clocks vary with frequency as follows:

FREQUENCY	ϕ1 PULSE WIDTH	ϕ2 PULSE WIDTH	CPU
2.045 MHz	140 nsec	280 nsec	8080A
2.386 MHz	70 nsec	210 nsec	8080A-2
2.863 MHz	70 nsec	210 nsec	8080A-1

ϕ1 and ϕ2 are applied to S-100 Bus pins 25 and 24 respectively through inverters (U92) and bus drivers (U77). They are also capacitively coupled to pins 2 and 4 respectively of driver U104, the phase clock conditioner.

An additional clock, called CLOCK, is taken from pin 8 of NAND gate U91. It occurs 70 nsec after ϕ2. It is used on the Sol-PC and is also made available on S-100 Bus pin 49 as a general 2.04, 2.38 or 2.86 MHz clock signal.

Three J-K flip-flops (U63 and 64) are used to synchronize the READY, RESET and HOLD inputs to the CPU. All three are connected as D-type flip-flops so that their outputs follow their inputs on the low-to-high transition of the clock. The READY flip-flop input on pins 2 and 3 of one section in U63 is either PRDY or XRDY from the S-100 Bus; these are normally pulled high by R34 and R12 respectively. S-100 Bus signal !PRESET, which is normally pulled high by R55, inputs the RESET flip-flop, the other section of U63. The HOLD flip-flop (U64) input is !P_HOLD, normally pulled high by R56, from the S-100 Bus. Pull up resistors R51, R50 and R53 insure that the high states of these three flip-flops are adequate for the CPU.

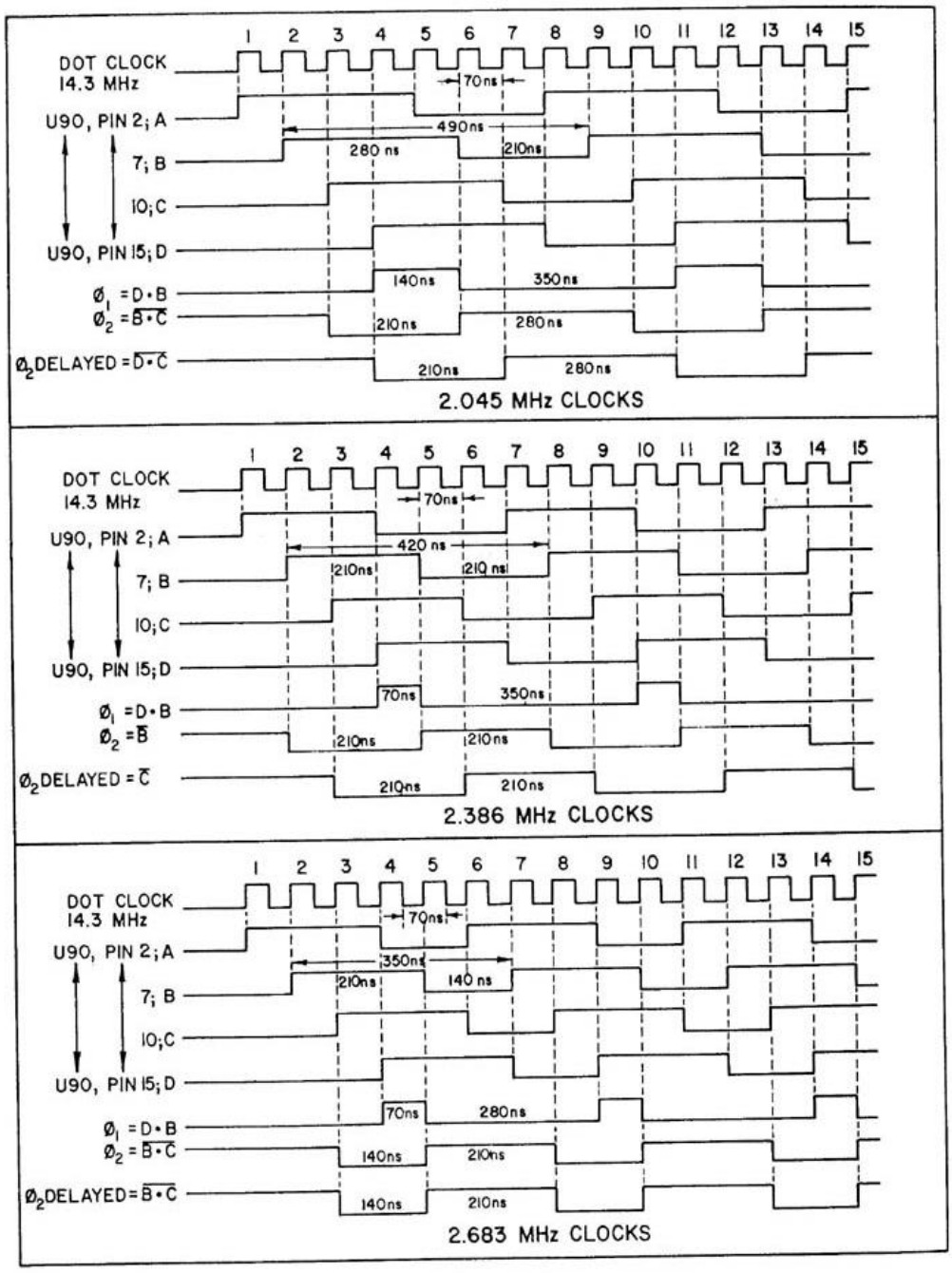


Figure 8-1. CLOCK GENERATOR TIMING

Diode D7, Cl5 and R18 make up the POC (power on clear) circuit. When power is applied, Cl5 starts to charge slowly until it reaches the threshold on pin 6 of U46, a Schmitt trigger. (By this time the logic and 5 volt supply have stabilized.) When the threshold is reached, pin 1 of U46 suddenly goes low. The resulting output on pin 8 of inverter U92 is initially low and then rapidly goes high. This signal is passed through a section of U77, a permanently enabled noninverting tri-state driver, as !POC to S-100 Bus pin 99. It is also inverted in a section of U45 to become POC.

The output on pin 8 of U92 is also connected to pin 15 of U63. Thus, pin 9 (RESET) of U63 is high to start the CPU in the reset condition when the Sol is initially turned on.

When !POC goes high, the RESET flip-flop section of U63 is free to clock. Assuming !PRESET is not active, it will change state on the first CLOCK transition. The resulting high on pins 10 and 5 of U63 cause pin 7 (READY) of U63 to go low to place the CPU in the not ready or wait state. This state is subsequently removed on the CLOCK transition following the transition which removed the low from pin 5 of U63. This helps prevent the CPU from starting in a crash condition.

The HOLD flip-flop (U64), however, is not affected by the POC circuit, and was clocked to a low on pin 7 well before the RESET and READY signals became active.

Operation of the POC circuit can also be initiated, without turning the power off, by a keyboard restart signal on pin 13 of J3 or by closing S1-1 if the N-P jumper is in. In either case, C15 is discharged through R58 and then allowed to recharge after !KBD_RESTART is removed or S1-1 is opened.

!POC also resets all stages of D flip-flop U76 (the phantom start-up circuit) to zero. On initial start-up, the CPU performs four fetch machine cycles (refer to Intel® 8080 Microcomputer Systems User's Manual) in accordance with program instructions. For each fetch, the CPU outputs a DBIN on pin 17. U76, connected as a four-stage shift register, is clocked by the inverted DBIN signal on pin 3 of NOR gate U46. Thus, !PHANTOM, on S-100 Bus pin 67, is active low (assuming the F-to-G jumper is in) for the first four fetches or machine cycles. After the fourth DBIN, !PHANTOM goes high. !PHANTOM is used to 1) disable any memory addressed in Page 0 that has Processor Technology’s exclusive “Phantom Disable” feature and 2) cause the Sol program memory (ROM), which normally responds to Page C0 (hex) to respond to Page 00 (hex). The second function is discussed in Paragraph 8.5.2.

The inverted DBIN on pin 3 of U46 is also applied to pin 12 of NOR gate U46 and inverted to appear as PDBIN on S-100 Bus pin 78. This section of U46 also allows !DIG1 (bus pin 57) to override DBIN. (!DIG1 is used when an external DMA device replaces the CPU in terms of writing into and reading from memory.) The other CPU control signals (SYNC, INTE, HLDA, WR and WAIT) are also fed to the S-100 Bus pins as indicated. These, as well as DBIN or !DIG1, are placed on the bus through tri-state drivers which are enabled by C/C DSB on S-100 Bus pin 19. Note that this signal is normally pulled high by R20.

The data lines of the CPU (D0-7) are bidirectional and are used for several functions. One of these is to output status at the start of each cycle which is marked by the SYNC output of the CPU. Status on D0-7 is latched in U93 and U106 (each of which contains four D flip-flops) when pin 8 of inverter U45 goes high. Status information, as identified on the schematic, is then buffered through tri-state drivers U94 and U107 to the S-100 Bus. The status latch strobe on pin 8 of U45 is extracted in the middle of the SYNC pulse by gating PSYNC and !ϕ2 in NAND gate U44. !STAT_DSB on S-100 Bus pin 18 is used to disable the U94 and U107 buffers when a DMA device or another processor assumes control of the S-100 Bus.

A second function of D0-7 is to output data from the CPU to the Bidirectional Data Bus. Data out of the CPU is placed on this bus through tri-state drivers (U80 and U81). Note that these drivers are normally enabled unless this bus is in the input mode or an external device has control of the bus. In the latter case, !DO_DSB on S-100 Bus pin 23 would be pulled low to make pin 8 of NOR gate U48 high. In the input mode pin 8 of U48 is high because !OUT_DSB is low. This signal is generated by decoding !PAGE_CC, MEM_SEL, !PORT_IN_FC, PORT_IN_FD, INT_SEL to produce MPX_ADR_A and MPX_ADR_B on pins 3 and 11 respectively of two NOR gates in U48. MPX_ADR_A and MPX_ADR_B are decoded with !DBIN on pin 5 of NAND gate U47.

The D0-7 bus lines are also used to input data to the CPU. Data input to the CPU is multiplexed from four data buses with four 4-to-l line multiplexers (U65, 66, 70 and 79). These four buses are the: 1) Keyboard Data Bus, KDB0-7, 2) Parallel Input Data Bus, PID0-7, 3) Internal Data Bus, INT0-7, and 4) Bidirectional Data Bus, DIO0-7.

These data multiplexers are tri-state devices, with their outputs pulled up by R107 through R114 to a level that satisfies the input requirements of the CPU. Their outputs are active only when both their El and E2 (pins 1 and 15) are low. As can be seen, this occurs only when !DBIN on pin 3 of NOR gate U46 is low; that is, when the DBIN output of the CPU is active to indicate its data bus is in the input mode.

Input selection to the multiplexers is done with the A and B inputs to U65, 66, 78 and 79. These two inputs are driven by MPX_ ADR_A on pin 3 of NOR gate U48 and MPX_ADR_B on pin II of NOR gate U48. There are four possible states for the combination of MPX_ADR_A and _B, and their relation to input selection is as follows:

1. If both are active (high), the multiplexers select the Bidirectional Data Bus.

2. When the keyboard is called up by the CPU, only !PORT_IN_FC is active (low) to make MPX_ADR_A low. This selects the Keyboard Data Bus.

3. When the parallel port is called up by the CPU, only !PORT_IN_FD is active (low) to make MPX_ADR_B low. This selects the Parallel Input Data Bus.

4. When the CPU selects any I/O port that uses the Internal Data Bus, only !INT_SEL (pin 2 of U47 and U61) is active. Thus, both MPX_ADR_A and _B are low to select the Internal Data Bus.

Two other conditions, defined by !PAGE_CC on pin 2 and MEM_SEL on pin 1 of NAND gate U44, are possible. When any of the four memory pages in the Sol are accessed, MEM_SEL goes high and an inversion in U44 (!PAGE_CC is normally high) appears as a low MPX_ADR_A and _B to select the Internal Data Bus. Should Page CC (the Display RAM) be addressed, !PAGE_CC also goes active (low) to override MEM_SEL. MPX_ ADR_A and _B are consequently high to select the Bidirectional Data Bus. These two conditions are required since the ROM and System RAM use the Internal Data Bus and the Display RAM uses the Bidirectional Data Bus.

The address outputs of the CPU (A0-15) are placed on the Address Bus via tri-state drivers (U67, 68 and 81). These drivers are normally enabled since pin 3 of inverter U49 is pulled high by R36. !ADD_DSB on S-100 Bus pin 22 is used to disable the address drivers when a DMA device or another CPU takes over the bus.

A 5.1 volt zener diode, D11, and a divider network composed of R130, 131 and 132 derive -5 V dc from the -12 V dc supply for use by the CPU. Diode D12 and the same divider supply -12 V dc to pin 3 of U104, the phase clock conditioner.

8.5.2 Memory and Decoder

Refer to the Memory and Decoder Schematic in Section X, Page X-16.

The System RAM consists of eight 1K by 1 bit static memory chips, U3 through U10, and it is assigned addresses C800-CBFF (hex). When the CPU wants to write data into memory, it addresses the System RAM on ADR0-15. ADR0-4 select the row inside the RAM chips, ADR5-9 select the column, and ADR10-15 select the page (in this case Page C8, hex). Page selection enables the eight RAM chips on pin 13. For a read operation, MWRITE on S-1OO Bus pin 68 is low, and the resulting high on pin 3 (WE) of the RAM chips keeps them in the read mode. Thus, data on the Bidirectional Data Bus is read into the PRAM'S on their D1 (pin 11) inputs. MWRITE is high, however, during the time the CPU wants to write data into memory. In this case, pin 3 of the RAM's is low to enable them to accept data from the Bidirectional Data Bus.

The ROM is also addressed on ADR0-15 as is the System RAM. Since there can be two pages, however, two enable lines (one for Page C0, hex, and the other for C4, hex) are provided. The C0 and C4 enables are connected to pins A6 and A5 respectively of J5, the Personality Module connector. Unlike the RAM, the ROM can only read data into the CPU, so the previously discussed MWRITE signal is not needed. Data out of the ROM is output on the Internal Data Bus on pins A3, A4 and B5-10 of J5.

ADR10-15 are input to the Address Page and Port Decoder (U34, 35, 36 and their associated logic). U34 (Address Page), U35 (Output Port) and U36 (Input Port) are 3-to-8 line decoders which have three enable inputs (G1, G2A and G2B). G1 must be high and both G2A and B must be low in order to obtain an active output.

Let's look at the Address Page Decoder, U34, first. It must be able to decode four pages: C0 and C4 (ROM), C8 (System RAM) and CC (Display RAM). (Note that these are the hexadecimal digits of the six high order address bits, ADR10-15).

The high order four bits (ADR12-15) must be 1100 (C, hex) in all cases by virtue of the U22 exclusive OR logic. If they are not, the G1 enable on U34 is low to disable that decoder. Bits ADR10 and 11 (The A and B inputs to U34) are the high order bits of the second hexadecimal digit which must be 00 (0, hex), 01 (4, hex), 10 (8, hex) or 11 (12, hex) if U34 is to have an active output. For C0, pin 11 of U34 is active (low); for C4, pin 10 is active; for C8 pin 9 is active; and for CC pin 7 is active. These outputs are applied to the appropriate memories and also provide the MEM_SEL signal on pin 6 of one section in U23. (This section is actually a 4-input NAND gate which is functionally the same as a 4-input NOR gate.)

Note that the U22 logic input with ADR14 and 15 is also connected to !PHANTOM. When this signal is active (low), the output on pins 3 and 11 will be low to disable U34 when ADR12-15 represent a C. If Page 0 is addressed, however, pins 3 and 11 of U22 are high, and this, coupled with lows on ADR10-13, are decoded by U34 as an active output on pin 11. The ROM will consequently respond to addresses in Page 0 and C0 (hex) as long as !PHANTOM is active.

The other two enables on U34 (G2A and G2B) are connected to SINP and SOUT. These two status signals indicate an input or output operation during the CPU cycle. U34 is therefore disabled during these operations.

SINP and SOUT are also fed to pins 5 and 6 of NOR gate U53 which detects an input or output operation. Its output is inverted by U54 and applied to pin 9 of another U53 NOR gate. The other input (pin 8) to U53 is MEM_SEL. So during a memory reference, input operation or output operation, pin 10 of U53 is active to enable the PRDY driver, U71. The low on pin 10 of U53 is also clocked by ϕ2 as a high to pin 7 of U70, a J-!K flip-flop that is connected as a D flip-flop. Note that the !(PSYNC & !ϕ2) signal on pin 5 of U70 forces U70 to set during the middle of PSYNC (refer to CPU and Bus discussion). U70 cannot clock until pin 5 is released, and this occurs simultaneously with the low-to-high transition of ϕ2. PRDY is thus low immediately after pin 10 of U53 goes low and remains in that state from the middle of PSYNC to the first positive-going ϕ2 after PSYNC. This is the time the CPU tests the status of the ready lines (PRDY and XRDY). If either is low, the CPU enters a WAIT state. U53, 70 and 71 thus guarantees that the CPU enters one WAIT state during cycles in which an input, output or memory reference is made.

U35 and 36, the Output and Input Port Decoders respectively, decode the higher order eight address bits (ADR8-15).

All Sol ports have a hexadecimal F (1111) in their high order four bits (ADR12-15 are 1's). The second hexadecimal digit is also never less than eight. This means that ADR11 is always 1 for a port address. These five address bits are thus NAND gated in U23 to provide one of the enables on U35 and 36. Note that the ADR14-15 combination is derived from the output on pins 3 and 11 of the U22 exclusive OR logic. This is permissible since no I/O operations are performed during the first four start-up cycles of the CPU.

The A, B, and C inputs to U35 and 36 (ADR8, 9 and 10 respectively) specify the second hexadecimal digit in the port address and are decoded to supply the indicated outputs. These outputs and their functions are defined in Table 8-1. U36 is enabled to decode when PDBIN and SINP are active; that is, during an input operation. U35 is enabled when SOUT and !PWR are active; that is, during an output operation.

INT_SEL on pin 8 of inverter U83 is the remaining signal generated by the Input Port Decoder circuit. This signal is active when either input port F8, F9, FA or FB is decoded by U36.

Both the address page and input/output decoders can be disabled by SINTA (S-100 Bus pin 96) when the AE-to-AC and AB-to-AD jumpers are installed. SINTA is active (high) when the CPU is responding to an interrupt. Should an external device issue addresses during this time, any memory response would interfere with the

Table 8-1. Port Decoder (U35 & U36) Outputs and Their Functions.

PORT DECODER OUTPUT	FUNCTION
!PORT_OUT_FE	Loads starting row address and first display line position information from Bidirectional Data Bus into Video Display scroll circuit.
!PORT_OUT_FD	Clocks data from Bidirectional Data Bus to output data pins of PP connector.
!PORT_OUT_FB	Loads data from Bidirectional Data Bus into Cassette Data UART.
!PORT_OUT_FA	Clocks PP and CDI control bits from Bidirectional Data Bus.
!PORT_OUT_F9	Loads data from Bidirectional Data Bus into SDI UART.
!PORT_OUT_F8	Clocks RTS (request to send) from bit 4 of Bidirectional Data Bus to pin 4 of SDI connector.
!PORT_IN_FF	Permits CPU to read data byte entered from Sense Switches.
!PORT_IN_FE	Places Video Display scroll timer and screen position status on bits 0 and 1 of Bidirectional Data Bus.
!PORT_IN_FD	Switches Data Input Multiplexer to input data pins of PP connector and resets PP at end of a transfer to ready it for another.
!PORT_IN_FC	Switches Data Input Multiplexer to Keyboard Data Bus.
!PORT_IN_FB	Strobes received data in CDI UART to Internal data Bus.
!PORT_IN_FA	Places PP, keyboard and CDI UART status on Internal Data Bus.
!PORT_IN_F9	Strobes received data in SDI UART to Internal Data Bus.
!PORT_IN_F8	Places SDI UART status on Internal Data Bus.

interrupt operation. To prevent this, SINTA is inverted in U58 to 1) disable U34 on pin 6 and 2) force pin 8 of NAND gate U23 high to disable U35 and U36 on pin 5. (This feature is provided to enable future versions of Sol to operate with a vectored interrupt system.)

8.5.3 Input/Output

Refer to the Input/Output Schematic In Section X, Page X-17.

This section in the Sol has five functional circuits: 1) Parallel I/O Logic, 2) Sense Switch Logic, 3) Keyboard Flag Logic, 4) SDI/UART and 5) Baud Rate Generator.

The PP uses U95 and 96 (4-bit D-type registers) and their related logic. Data output to the PP connector (J2) is latched from DIO0-7 by U95 and U96. Data is strobed into these registers on the leading edge of an inverted active !PORT_OUT_FD signal on pin 4 of inverter U54. This strobe is also applied to pin 2 of U73 which functions as a J-K flip-flop that is clocked by !ϕ2. When the !ϕ2 goes from low to high 200 to 300 nsec after !PORT_OUT_FD, pin 7 of U73 goes low to become !POL on pin 17 of J2. (This delay allows U95 and 96 to stabilize.) U73 is reset in the middle of the following PSYNC which means !P0L is active for the balance of the cycle.

The outputs of U95 and 96 are tri-state outputs that are enabled by a low on pin 2. In the absence of POE at pin 15 of J2, pin 2 of U95 and 96 are low by virtue of the output on pin 8 of inverter U55. Note that the input to U55 is normally pulled up through R63. The POE provision permits tri-stating an external bidirectional data bus.

As discussed in Paragraph 8.5.1, parallel input data on J2 is fed directly to the Data Input Multiplexer (see Page X-15). The strobe that indicates the presence of input data, !PDR on pin 4 of J2, is applied to pins 2 and 3 of one section in U72, a J-!K flip-flop which is connected as a D flip-flop. When !PDR goes active (low), pin 7 of U72 will go high on the next low-to-high transition of ϕ2 to toggle the following U72 stage. At this point pins 9 and 10 of the second section in U72 go high and low respectively. Pin 9 supplies PIAK on pin 5 of J2. When high, PIAK signals the external device that Sol has yet to complete acceptance of the data. The state of pin 10 of U72 is transmitted to INT1 of the Internal Data Bus through a U71 tri-state noninverting buffer. U71 is enabled only for the duration of !PORT_IN_FA (auxiliary status). During the time U71 is enabled, the CPU reads the Internal Data Bus. A high INT1 indicates the parallel input data is not ready; a low indicates the data is ready.

The second U72 flip-flop is preset by !PORT_IN_FD or POC. !PORT_IN_FD is active to read data in from the PP; POC occurs only when Sol is restarted or power is turned on. Thus the PP is reset and ready for another transfer at the end of a transfer or when POC is active.

PXDR on pin 16 of J2 is supplied by the external device. It indicates the device is ready to receive data. !PXDR is buffered to INT2 and will effect the transfer of data to the Internal Data Bus during the status input to the CPU. !PXDR is analogous to the previously discussed PIAK signal.

Sense Switches S2-1 through 8 are driven by !PORT_IN_FF when it is low. Thus, the DIO lines connected to closed switches are driven low, and those connected to open switches are pulled high.

U97 (a 4-bit D-type register) and one section of U52 (a J-!K flip-flop connected as a D flip-flop) latch five bits of data on D103-7 when !PORT_OUT_FA goes active. These bits, which supply the indicated outputs, control conditions in both the PP and CDI. With respect to the PP, PIE enables parallel input, and PUS selects the parallel device for the transfer. The data in these two latches remains until either a new word is read out or POC goes active.

Also during !PORT_OUT_FA, the keyboard flag is reported. !KEYBOARD_DATA_READY on pin 3 of J3 is a low going pulse 1 to 10 usec in duration. It is applied to pin 13 of J-!K flip-flop U70. Some time after pin 13 of U70 goes low, but before 500 nsec, U70 is set by ϕ2 and pin 10 goes low. This low is buffered through U71 to INT0 to indicate the keyboard is ready to send data. Reset of U70 occurs with a POC or by !PORT_IN_FC. The latter occurs when data is accepted from the keyboard.

The other half of flip-flop U52, with its output on pin 6, latches one bit of status, D104, when !PORT_OUT_F8 is active. Its output is applied to pin 5 of one operational amplifier section in U56 to become the SRTS (request to send) signal on pin 4 of J1, the SDI connector.

The SDI/UART centers around a UART, U51. The UART transmission conditions (parity, word length and stop bits) are determined by the settings of S4-1 through 5. (Refer to Paragraphs 7.5.8 through 7.5.10 in Section VII for descriptions of the switch settings and their effect on transmission.

Data destined to leave Sol through the SDI/UART enters the UART on its TI1-6 inputs from the Bidirectional Data Bus when TBRL (pin 23) is low; that is, when !PORT_OUT_F9 goes active. Circuitry within the UART serializes the input data, which is in parallel form, and outputs it on pin 25 at a rate determined by the clock on pin 40. The binary states at pin 25 are low for a zero and high for a one. Assuming Sol is not in local operation ("off line"), the output on pin 25 of the UART is applied to pins 2 and 11 of J1 via two gates in U55 and the other half of U56.

Data that enters Sol through the SDI/UART on pins 3, 12 or 13 of J1 is input to the SDI UART on pin 20 by way of U38, an inverting level converter that converts data levels of up to 25 volts to TTL levels. (Note that current loop data on pin 12 or 13 of J1 is first rectified before it is applied to U38.) The UART converts this serial data into parallel form and outputs it on RO1 through RO8 (pins 12 through 5 respectively) to the Internal Data Bus when ROD (pin 4) is low; that is, when !PORT_IN_F9 goes active.

The receive-transmit clock for the SDI UART is supplied by the Baud Rate Generator (U84, U85, U86 and their associated circuitry). U85 is a phase locked loop, U86 is a 7-stage binary counter and U84 is connected as a divide-by-11 counter. The 1200 Hz reference signal applied to pin 14 of U85 is supplied from the Video Display Generator. A phase comparator in U85 compares this signal to the output of a voltage controlled oscillator (VCO) in U85. By feeding an output from U86 (in this case the 1200 Hz output on pin 3) back to the compare input (pin 3) of U85, the circuit acts as a frequency multiplier. The output (pin 4) of U85 remains locked, therefore, to a multiple of its input on pin 14. In this case we have a 128X multiplier to generate 153.6 KHz which is counted down in U86. Since U86 is a 7-stage binary counter, the first stage output (pin 12) is 76.8 KHz (one-half of 153.6 KHz, the clock for U86), the second stage output (pin 11) is 38.4 KHz (one-fourth of 153.6 KHz), the third stage output (pin 9) is 19.2 KHz (one-eighth of 153.6 KHz), and so on to the seventh stage output (pin 3) which is 1.2 KHz (1/128 of 153.6 KHz).

With the exception of outputs on pins 12 and 9, the outputs of U86 are connected to S3, the Baud Rate Switch. The 19.2 KHz output on pin 9 is divided by 11 in U84 to supply 1745 Hz to S3-2. The 38.4 KHz on pin 12 can be connected to S3-8 instead of the 153.6 Hz clock by cutting the L-M connection and installing a jumper between K and M.

Let's now translate the frequencies input to S3 into Baud rates. The Baud rate of a UART is 1/16 of its clock rate. Thus, a 1200 Hz clock equates to a 75 Baud transmission rate, a 1745 Hz clock equates to a 109.1 (110) Baud rate, etc. It is now readily seen that the Baud rate available with S3-8 is 9600 assuming the L-M connection is made (153.6 KHz - 16 = 9600). (The L-M connection is default wired on the Sol-PC; that is, there is a trace between L and M on the circuit board.) If the L-M trace is cut and a jumper is installed between K and M, the Baud rate with S3-8 is 4800 (76.8 KHz - 16 = 4800).

We can thus select any one of eight clock frequencies for the SDI UART with S3, with the highest being determined by the K, L and M jumper arrangement. The selected clock is applied to both the receive and transmit clock inputs (pins 17 and 40 respectively) of the UART. This means, of course, that the UART always receives and transmits at the same Baud Rate.

Returning to the SDI UART, we see that its transmitter output on pin 25 is applied to pin 5 of U55, a two-input NAND gate that is functionally a NOR gate. It is normally enabled on pin 4 by pull-up resistor R44. A low on pin 5 represents a binary 0; a high represents a binary 1. The inverted output on pin 6 of U55 is again inverted (assuming Sol is not operating in Local) by the following U55 NAND gate. One-half of operational amplifier U56, operating open loop, converts TTL levels to RS-232 levels (5 to 15 volts). Pin 3 of U56 is held at +2.5 V dc by the R47 and R48 divider network. When pin 2 is more negative than pin 3, the output on pin 1 of U56, which is fed to pin 2 of J1, is at approximately +10 volts. For the opposite condition, pin 2 of J1 is about -10 volts. Thus, U56 also inverts, and a high or low on pin 2 of J1 represent a binary 1 and 0 respectively.

Two conditions can override transmitted data: a keyboard break (!BRK) or local (!KBD_LOC) command. For a break command, !BRK on pin 4 of J3 and pin 4 of NOR gate U55, is low to hold pin 6 of U55 high for the duration of the !BRK signal. This appears as a "space", or high level, on pin 2 of J1. (A space, or break, condition requires that the space level exist for a period longer than the normal length of a character.) In the case of a !KBD_LOC command from the keyboard, pins 1 and 13 of the other two U55 sections are low. Thus, data cannot be transmitted to pin 3 of NAND gate U55, and pin 11 of NOR gate U55 is held high to enable tri-state driver U37 at pin 15. Data on pin 6 of U55 is consequently looped back by way of U37 and R21 to pin 12 of U38. Data on pin 12 of U38 overrides any data arriving at pin 13 of U38. In local operation, therefore, data from pin 25 of the UART does not appear at pin 2 of J1, but it is looped back to the receiver input (pin 20) of the UART via U37, R21 and U38.

Notice that data on pin 25 of the UART will also be looped back if S4-6 is closed (half duplex operation). But in this case, data from the UART is also fed to pin 2 of J1.

Serial data from the UART that appears at pin 1 of U56 also drives transistor Q1 by way of R45 and R46 to supply the serial current loop output (SCLO) on pin 11 of J1. Q1 supplies 20 ma. (max.) current for a binary 1 and no current for a binary 0.

Pin 23 of J1 (connected through R23 to +12 V dc) is the serial loop current source (SLCS). It can supply up to 20 ma of current to ground and is used when the external current loop device has no current source.

Data received from a current loop device enters Sol on pins 12 and 13 of J1 in the form of no current for a 0 and 20 ma of current for a 1. This input is rectified by bridge rectifier D3-D6 and applied to a light emitting diode (LED) in optical isolator U39. As its name implies, U39 electrically isolates the current loop circuit from the rest of the Sol. (This isolation permits a high offset voltage on pins 12 and 13 of J1.) For a 1, the LED is energized, and

the light is optically coupled to the base of a photo transistor in U39 to cause the transistor to conduct. Conduction translates to a low, or mark, level at the input (pin 13) of U38. Since both the current loop and RS-232 received data (SLR1/SLR2 and SRD respectively) share the input to U38, both should not be used simultaneously.

There are five external control signals in the RS-232 section of the SDI/UART: two are sent to the external device (SRTS and SDTR), and three are received from the device (SCTS, SCD and SDSR).

SRTS on pin 4 of J1 was discussed earlier. SDTR (serial data terminal ready) is simply tied to +12 V dc through R24. This indicates to the external device that Sol is connected to it.

SCTS (serial clear to send), SCD (serial carrier detect) and SDSR (serial data set ready) indicate status of the external device. They enter Sol on pins 5, 8 and 6 of J1 respectively, and all three are active high. Following level conversion and inversion in line receivers U38, data on these lines is gated through noninverting tristate buffers U37 to the Internal Data Bus when !PORT_IN_F8 is active.

!PORT_IN_F8 also enables five bits of UART status to be reported over the Internal Data Bus. These are PE, FE, OE, DR and TBRE on pins 13, 14, 15, 19 and 22 respectively of the UART. They are defined as follows:

PE: Parity Error--received parity does not compare to that programmed. (Bit INT2)

FE: Framing Error--valid stop bit not received when expected. (Bit INT3)

OE: Overrun Error--CPU did not accept data before it was replaced with additional data. (Bit INT4)

DR: Data Ready--data received by UART is available when requested. (Bit INT6)

TBRE: Transmitter Buffer Register Empty--UART is ready to accept another word from the Bidirectional Data Bus. (Bit INT7)

8.5.4 Display Section

An understanding of how characters are formed on the video monitor will help you follow operation of the display section.

The monitor screen can be thought of as a large matrix of small light elements, or dots, that can be turned on and off. In this context the overall video presentation consists of light and dark dots.

In the Sol, the display format is 64 characters maximum per character row, with a maximum of 16 rows per frame (page). Thus, up to 1024 characters can be displayed per page.

A 9x13 (columns by lines) dot area, or character position, is alloted on the monitor screen for each displayed character (see Figures 8-2 and 8-3 on Page VIII-24). Consequently, each character row consisting of sixty-four 9 x 13 dot areas requires 13 horizontal scan lines. To provide spacing between both characters and rows, only 12 dot lines and seven dot columns within the 9 x 13 matrix are used for character display. Only nine of the available 12 dot lines, however, are used for any given character.

Let's take a closer look at how the 9 x 13 dot matrix is used. The first seven dot columns are available for all character displays; the last two are used to provide a space between characters. The first dot line in a character row is always blank to provide a space between character rows. As shown in Figure 8-2, the second through tenth dot lines are available for all upper case (capital) and control characters, all symbol and punctuation marks (except the comma and semicolon), and all lower case characters (except the g, j, p, q and y). As shown in Figure 8-3, dot lines five through 13 are available to display characters that normally extend below the base line--lower case g, j, p, q and y plus the comma and semicolon.

Now that we have a feeling for how characters are formed on the video monitor screen, we will move on to the circuit description.

Refer to Display Section Schematic in Section X, Page X-18.

The 14.31818 MHz DOT_CLOCK, which defines the period of one dot (69.8 nsec) in a character display matrix, controls all timing in the Video Display Generator. DOT_CLOCK is applied to pin 2 of U28, a four-bit binary counter that is preset to count from seven through 15 to divide DOT_CLOCK by nine. Two 1.591 MHz outputs are supplied by U28: LOAD_CLOCK on pin 11 and !CHARACTER_CLOCK on pin 12. Pin 11 is a low-active pulse of one DOT_CLOCK duration. Pin 12 is high for five and low for four DOT_CLOCK periods. Both the LOAD_ and !CHARACTER_CLOCK low-to-high transitions occur synchronously on the same DOT_CLOCK.

!CHARACTER_CLOCK, which defines the period of one character position (628 nsec), is inverted in U49 to become CHARACTER_CLOCK. It performs most of the clocking functions in the Video Display Generator and is made available on pin 4 of J4 for use by external graphic display devices.

CHARACTER_CLOCK is in turn divided in U31 and U33, both of which are presettable four-bit binary counters. Both start at count 3 when pin 8 of NAND gate U47 is low, and together they count 102 CHARACTER_CLOCKS to define horizontal timing at 64 usec (102 x 628 nsec = 64 usec).

CHARACTER ADDRESS*	LINE ADDRESS	SCAN LINE NO.	COLUMN NO. 1 2 3 4 5 6 7 8 9	VIDEO INFORMATION BITS
1001001	1111	1	O O O O O O O O O	000000000 (blank)
↑	0000	2	O # # # # # O O O	011111000
|	0001	3	O O O # O O O O O	000100000
|	0010	4	O O O # O O O O O	000100000
|	0011	5	O O O # O O O O O	000100000
|	0100	6	O O O # O O O O O	000100000
|	0101	7	O O O # O O O O O	000100000
|	0110	8	O O O # O O O O O	000100000
|	0111	9	O O O # O O O O O	000100000
|	1000	10	O # # # # # O O O	011111000
|	1001	11	O O O O O O O O O	000000000 (blank)
↓	1010	12	O O O O O O O O O	000000000 (blank)
1001001	1011	13	O O O O O O O O O	000000000 (blank)

*7-bit ASCII code for I # = illuminated dot

Figure 8-2. Example of uppercase character (I) display.

CHARACTER ADDRESS*	LINE ADDRESS	SCAN LINE NO.	COLUMN NO. 1 2 3 4 5 6 7 8 9	VIDEO INFORMATION BITS
1110000	1111	1	O O O O O O O O O	000000000 (blank)
↑	0000	2	O O O O O O O O O	000000000 (blank)
|	0001	3	O O O O O O O O O	000000000 (blank)
|	0010	4	O O O O O O O O O	000000000 (blank)
|	0011	5	# O # # # O O O O	101110000
|	0100	6	# # O O O # O O O	110001000
|	0101	7	# O O O O # O O O	100001000
|	0110	8	# O O O O # O O O	100001000
|	0111	9	# # O O O # O O O	110001000
|	1000	10	# O # # # O O O O	101110000
|	1001	11	# O O O O O O O O	100000000
↓	1010	12	# O O O O O O O O	100000000
1110000	1011	13	# O O O O O O O O	100000000

*7-bit ASCII code for p # = illuminated dot

Figure 8-3. Example of lowercase character (p) display.

As indicated in Figure 8-4 on Page VIII-27, Subgroup Counter U31 and Group Counter U33 are preset to a count of 3 at the start of each horizontal scan line. U31 counts from 3 through 15 (13 character positions) and enables U33 for one count. U31 then counts 0 through 15 and enables U33 for the second count. The sequence continues through four more groups of 16 character positions, and at this point U33 is at its sixth count (a binary 9). Thus, pins 11 and 14 are high at pins 10 and 11 of U47. U31 continues to count from 0, and on the ninth count (a binary 8) pin 9 of U47 goes high. The resulting low on output pin 8 of U47 loads three into U31 and U33, and the cycle repeats. The U31-U33 cycle) from preset, is then 13, 16, 16, 16, 16, 16 and 9 character position counts for a total of 102.

The QD output on pin 11 of U33 is SCAN_ADV, and the QC output on pin 12 is HDISP. SCAN_ADV is used to generate horizontal synchronization signals, and HDISP defines the start of the display portion of the horizontal scan line.

Four outputs from U31 and the two low order outputs of U33 (pins 13 and 14) are input to the Character Address Multiplexer, U30 and U32, which supplies the low order six address bits to the Display RAM (U14 through U21). The second address source for the Display RAM is the Address Bus, bits ADR0-5. Address source selection is controlled by the output on pin 7 of D flip-flop U75. Pin 7 of U75 goes high when !PAGE_CC (the Display RAM) is active and !(PSYNC & !ϕ2) goes high (which it does in the middle of PSYNC). Pin 7 of U75 remains high for the rest of the memory access cycle.

The preset signal (pin 8 of U47) to U31 and U33 is applied to the Scan Counter (U4O) via inverter U87. U40 counts the horizontal scan lines that make up a row of characters and supplies the line number to U25, the Character Generator ROM. (This ROM is discussed later.) U40 is preset to a count of 15 for the first scan line in the character row. It then counts from 0 through 11. On count 11, SCAN_ENABLE on pin 8 of U47 is inverted in U87 to disable the Scan Counter. A decoder, comprised of NAND gates U59 and U60, decodes the 13th count (count 11) in U40 and SCAN_ENABLE to supply a load pulse to pin 9 of U40. This resets U40 to a count of 15, and the cycle repeats. (Presetting the Scan Counter to a count of 15 permits the Character Generator ROM to provide a blank spacer line between character rows since line 15 in the ROM is always blank.)

The output on pin 8 of NAND gate U59, after inversion in U87, becomes the OVERFLOW_LINE signal. This signal occurs after each character row and appears at pins 7 and 10 of Text Counter U62 to enable it to count. Thus, the Text Counter counts character rows. It resets itself with its carry output (pin 15) through another inverter in U87, with the reset count being determined by the state on pin 10 (VDISP) of J-!K flip-flop U43. If VDISP is low, the Text Counter resets to a count of 0; if VDISP is high, it resets to a count of 12.

Assume VDISP is active (low), which it is during the vertical display portion of the displayable area on the screen. (Refer to Figure 8-4.) U62 is then preset to a count of 0 and will count from 0 through 15 (16 character rows). The resulting carry output on count 15 of the Text Counter causes the U43 VDISP flip-flop to toggle. It also appears as a low on the load input of the Text Counter. The Text Counter is also enabled to reset by virtue of the OVERFLOW_LINE going low after the reset of the Scan Counter. Since VDISP is now high, the Text Counter is reset to a count of 12 and will count 12 through 15 (four character rows). The carry output from the Text Counter then causes the U43 VDISP flip-flop to toggle, and the Text Counter is reset to a count of 0. We can now see that the Text Counter counts 16 character rows when the display is active (VDISP is low) and four character rows when the display is blanked (VDISP is high). The total of 20 character rows represents a full display of 260 scan lines for 60 Hz operation (13 scan lines/row x 20 rows = 260 scan lines per page).

Horizontal and vertical synchronization signals are generated by two one-shot multivibrators consisting of three two-input NOR gates in U102. Horizontal sync is triggered by SCAN_ADVANCE and vertical sync by !VDISP. Both circuits generate fixed-length sync pulses with adjustable starting times. C52 determines the length of the horizontal sync pulse and C53 the length of the vertical sync pulse. The starting times, with respect to triggering, are variable with variable resistors VR1 (HORIZ) and VR2 (VERT) to provide continuous adjustment of the display position on the screen. An exclusive OR gate in U74 combines the two sync pulses into a composite sync (COMP_SYNC) signal. Note that the use of the exclusive OR inverts the horizontal sync pulses when the vertical sync pulse appears. Since vertical sync information is extracted in a monitor by an integrating, or averaging, process, this technique maintains horizontal synchronization during the vertical sync period.

Two types of blanking are available: control character blanking and video blanking. The first blanks control characters and causes cursor information to be displayed in their place. Video blanking forces portions of the video display to a white or black level, depending on whether normal or reverse video is selected with S1-4.

Control character blanking, switch selectable with S1-3, is accomplished with one NAND gate in U60 and one NAND gate in U61. When a control character is present in the Data Latch (U26 and U27), pins 3 and 15 of U26 are high. Assuming the blanking option is selected (S1-3 closed), the output of U60 (!LOAD_CLOCK) is gated with the control character bits by U61 to clear the video parallel-to-serial converter, U41. U41 then loads all zeros instead of the character.

Video blanking is initiated by the PRE_BLANK or COMP_BLANK (pin 14 of Blank Latch U42) inputs to U59, a three-input NOR gate. The third input, the video output on pin 6 of exclusive OR gate U74, is blanked when any of the two blanking inputs is active.

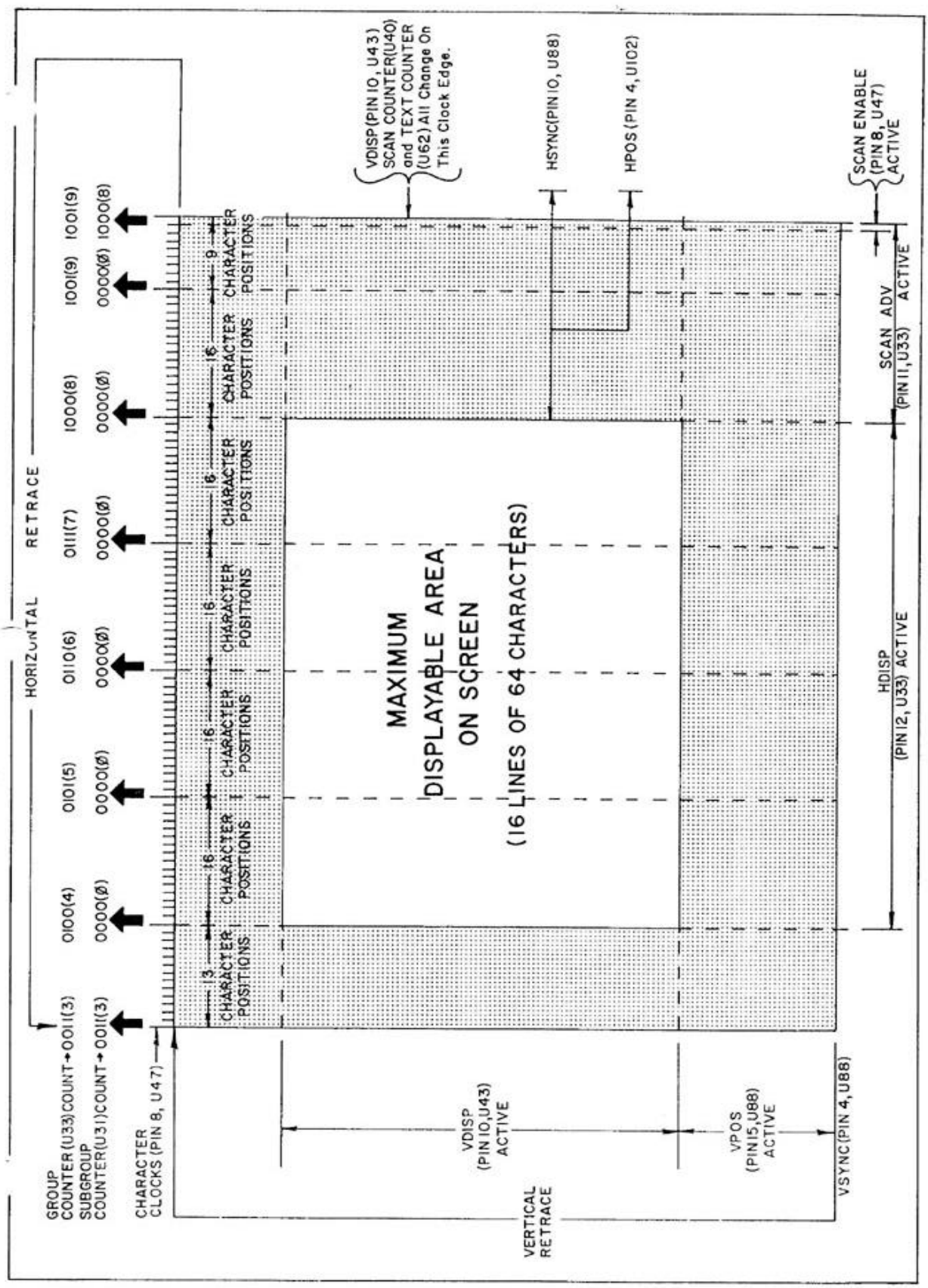


Figure 8-4. VIDEO DISPLAY TIMING

VIII-27

The PRE_BLANK input provides "window shade" blanking which is analogous to pulling a window shade down from the top of the display. PRE_BLANK is generated in one half of J-!K flip-flop U43. U43 is reset by the TC output of First Screen Position Counter, U11, and set by VDISP. The output on pin 7 of U11 is generated by the scrolling circuitry (to be discussed later) and defines the character row for which the "window shade" ends. It may begin with any character row from zero through 14.

The remaining video blanking function concerns the output on pin 14 of D flip-flop U42. This signal, COMP_BLANK, is a composite of HDISP and VDISP.

Since there is a two character time delay between Display RAM addressing and the corresponding video output on pin 6 of exclusive OR gate U74, the horizontal and vertical blanking signals must be delayed an equal amount. U42, connected as a two-stage shift register, functions to shift the blanking into synchronization with the video. Since U42 is clocked by LOAD_CLOCK (which has a period equal to one character time), COMP_BLANK is delayed two character times from the input on pin 4 of U42. COMP_BLANK is active low during nondisplayable portions of the video scan to override any video input data on pins I and 2 of NOR gate U59. The display is thus blanked.

The Display RAM consists of eight 1K x 1 bit RAM (random access memory) chips, U14 through U28. All chips are held permanently enabled by connecting their CE (pin 13) inputs to ground. Memory addressing is provided through two-to-one multiplexers (U30, U32 and U12) which select one of two display address sources: 1) an external address on Address Bus bits ADR0-9 and 2) an internal address supplied by the Subgroup Counter (U31), Group Counter (U33) and the Beginning Address Counter (U1). The function of the address bits associated with each address source is as follows:

1. External address bits ADR0-5 specify the character position (one of 64) in the character row.

2. External address bits ADR6-9 specify the character row position (one of 16) on the display screen.

3. Internal address bits, a total of six outputs from U31 and U33, specify the character position (one of 64) in the character row.

4. Internal address bits, the four outputs from U1, specify the character row position (one of 16) on the display screen.

Normally the internal display address is multiplexed to the Display RAM. When the CPU or a DMA device requests access (!PAGE_CC active), the multiplexers switch to the external address lines, ADR0-9.

Seven-bit ASCII-coded data is written into RAM chips U14 through U20 from bits DIO0-6 of the Bidirectional Data Bus, and the cursor bit (DIO7) is written into RAM chip U21. This writing occurs when the write enable (WE) input to the RAM chips is low. This occurs when the Display RAM is addressed (!PAGE_CC active low) and MWRITE on S-100 Bus pin 68 is high. The enable is supplied on output pin 8 of NAND gate U44. Data is read out of the Display RAM when pin 8 of U44 is high. Data out of the Display RAM is placed on the Bidirectional Data Bus via tri-state drivers U29 and U89 when !PAGE_CC and PDBIN (S-100 Bus pin 78) are active. U29 and U89 are enabled by a low output on pin 11 of another U44 NAND gate.

Data out of the Display RAM is also strobed into Data Latches U26 and U27 by LOAD_CLOCK. Seven outputs from these latches are used to address the Character Generator ROM, U25. Note that the output from RAM chip U19 is inverted in exclusive OR gate U74 before being applied to the C input (pin 13) of U26, and the complement (pin 14) of the QC output of U26 is used in addressing U25. This is done so that the Data latches will output the space code (0100000) to the Character Generator ROM when the latches are reset. These latches are reset each time !PAGE_CC is active by way of U75, a J-!K flip-flop connected as a D flip-flop, and D flip-flop U42 (Q output pin 6). By outputting the space code on reset, the Data Latches insure a blank character position on the screen.

The Character Generator ROM, U25, has seven character address inputs (A1 through A7), four scan line inputs (RS1 through RS4) and seven data outputs (B1 through B7). It is programmed to generate seven bits (dots) of character information for the selected scan line of the character row. U25 also automatically blanks scan lines that are not a part of the character and shifts the g, j, p, q, y, comma and semicolon to the fifth through 13th scan lines in the dot matrix (refer to Figures 8-2 and 8-3 on Page VIII-24). Complete patterns for the 6574 and 6575 Character Generator ROM's are provided in Figures 8-5 and 8-6 respectively. Note that the address bits A0 through A6 in Figures 8-4 and 8-5 correspond to the A1 through A7 inputs to U25 on the schematic, scan lines R0 through R8 are specified by the RS1 through RS4 inputs to U25 on the schematic, and the data output bits D0 through D6 correspond to the B1 through B7 outputs from U25 on the schematic.

Let's see how the Character Generator ROM produces a character using an uppercase "C" and "T" as an example. In this example, these two characters are to be displayed in the first and second character positions respectively on the third character row of the display screen. Remember that the character position and row parameters are contained in the Display RAM since the 7-bit ASCII-coded

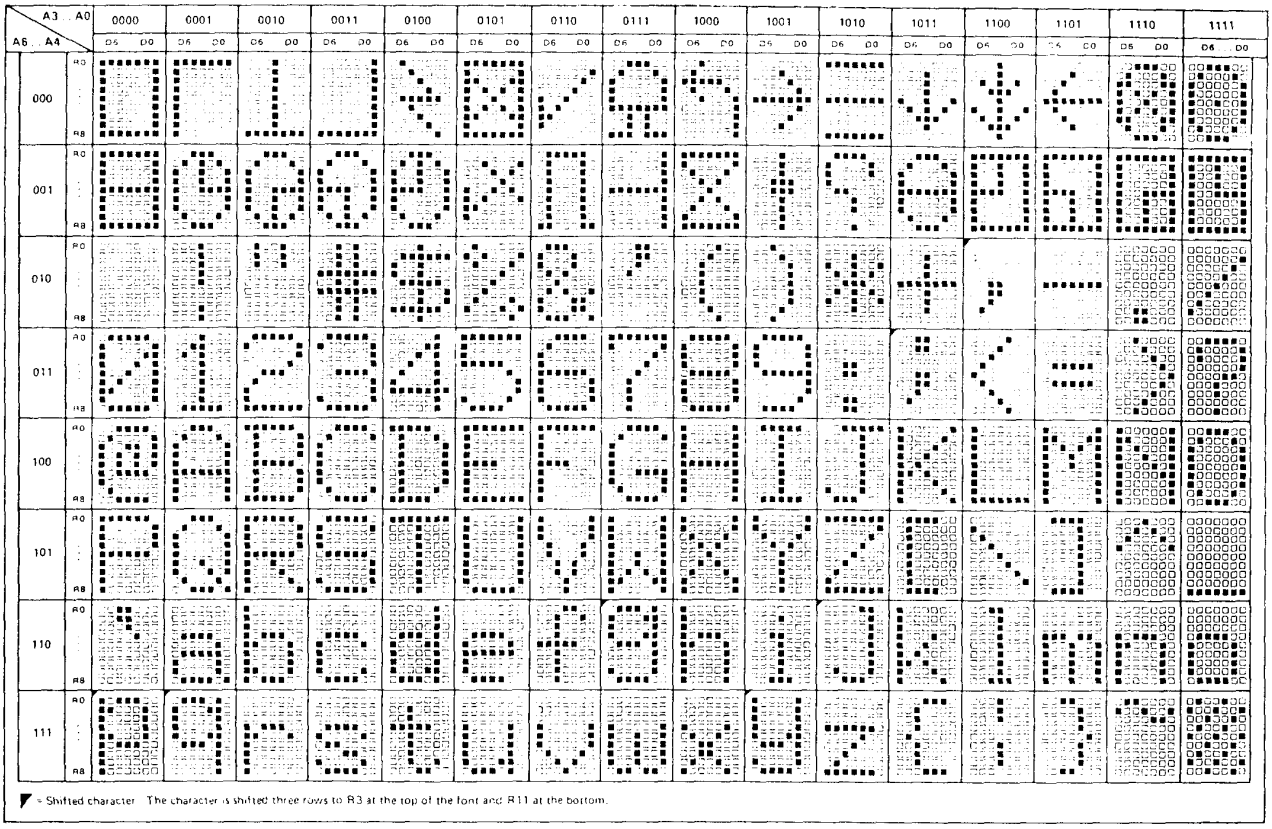


Figure 8-5. 6574 Character Generator ROM pattern.

"C" and "T" were stored in the RAM in the proper character positions in the third character row.

After the first two character rows have been displayed, the Scan Counter (U40) is reset to a binary count of 15 (1111) and the Character and Line Address Multiplexers (U30, U32 and U12) call up the "C" in the Display RAM. The Scan Counter output specifies line 15 in the Character Generator ROM on RSI through RS4. As previously mentioned, this line in the ROM is blank. Thus, the first scan line of the third character row is blank.

The 7-bit ASCII code for the "C" (1000011) is input from the Display RAM to address the Character Generator ROM by way of the Dat. Latches (U26 and U27). This address is applied to ROM inputs A7 through Al (A6 through A0 in Figures 8-5 and 8-6). The Scan Counter changes to a count of zero which specifies scan line R0 in the Chara' ter Generator ROM. As shown in Figures 8-5 and 8-6, the ROM in turn outputs a 7-bit word, 0011110, on D6 through D0 respectively (B7 through B1 on the schematic).

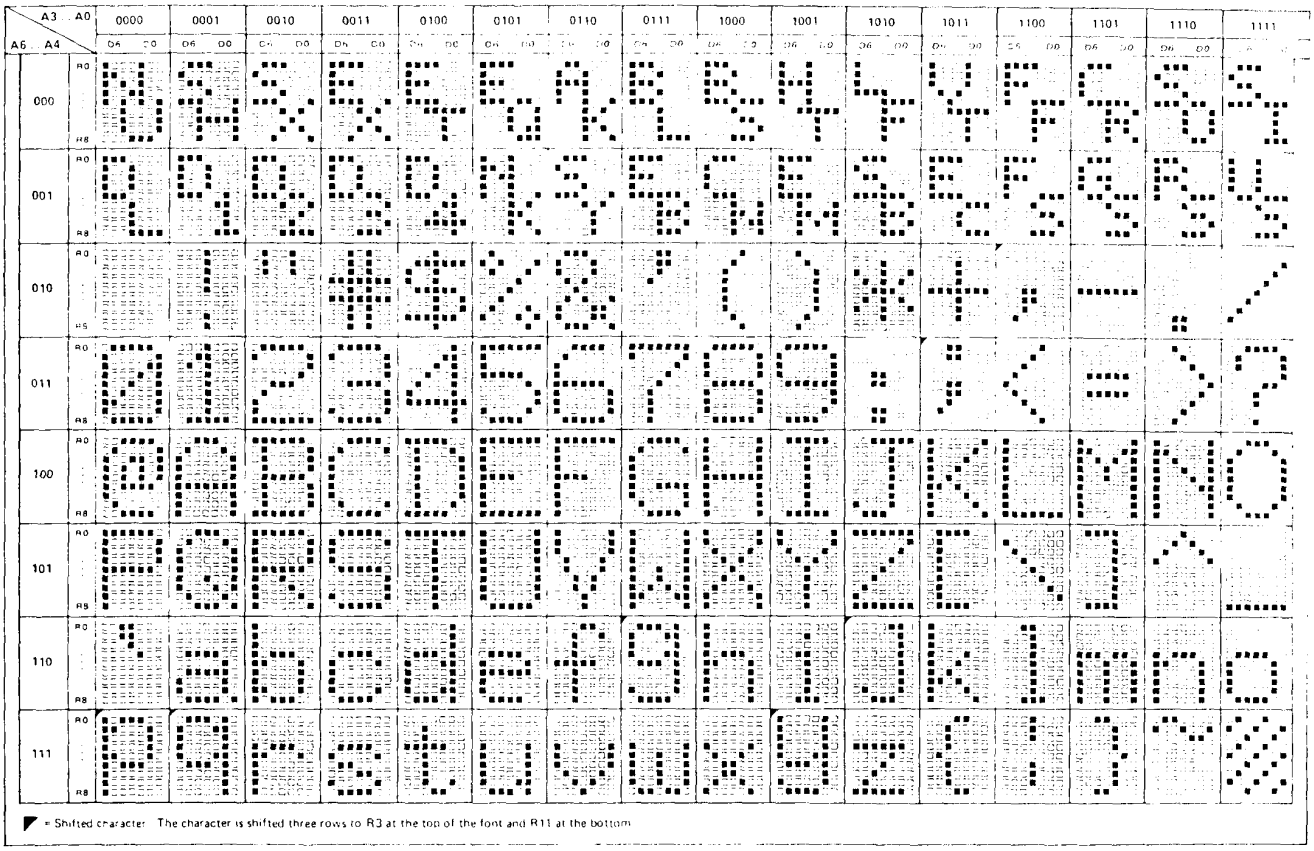


Figure 8-6. 6575 Character Generator ROM pattern.

For the second character position the Character and Line Address Multiplexers call up the "T" in the Display RAM. The resulting ASCII code for a "T" (1010100) ultimately appears on the address inputs to the Character Generator ROM. Since the Scan Counter is still at a count of zero, the ROM outputs 1111111. This process continues for the balance of the displayable portion of the video scan line.

At the end of the horizontal scan line, the Scan Counter changes to a binary count of 0001 which specifies scan line R1 in the Character Generator ROM. The "C" and "T" are again called up from the Display RAM for the first and second character position respectively. The ROM consequently outputs 0100001 and then 0001000. This sequence continues through scan line R8 when the Scan Counter is at a count of 8 (1000) to produce the "C" and "T".

As discussed earlier, the Scan Counter cycles through 13 counts or scan lines. For the "C" and "T" in our example, the Scan Counter has counted ten lines (15, 0, 1, 2, 3, 4, 5, 6, 7 and 8). The remaining three scan lines are not used in forming the "C" or "T", so on counts 9, 10 and 11 of the Scan Counter the Character

Generator ROM automatically outputs all zeros for these two character positions. After the last scan line in the third character row, the Scan Counter is reset to a count of 15 to start the fourth character row.

The Character Generator ROM output is converted from parallel to serial form in an 8-bit shift register (U41) that is clocked by DOT_CLOCK. For each high bit on the input, the serial output (QH, pin 13) of U41 is high for one DOT_CLOCK period. For each low bit, QH is low for one DOT_CLOCK period. Note that parallel input bit PH (pin 14) is tied to ground. This effectively adds a low bit (or dot) following the data and provides one of the spacer dots between characters. The second spacer dot is generated by connecting the serial input (pin 1) to ground and applying LOAD_CLOCK to the load (LD, pin 15) input to U41. When LOAD_CLOCK goes low, which it does every ninth DOT_CLOCK, U41 shifts in one zero.

A blink oscillator (two inverter sections in U88), a latch (one section in U42) and their associated components comprise the cursor circuit. The blink oscillator runs continuously at a rate set by R84 and C36. Its output has a nominal 0.5 sec period. If the blink option is selected with S1-5, the blink signal is applied to one input of a gate in U60. The other input to this gate is provided by the blink latch, one section in U41. If the cursor bit QA out of Data Latch U26 is high, D flip-flop U42 sets for the time the ROM is active on the character and remains set during the period when video data is shifted out of U41. The output of U42 is gated high through NAND gate U60 when BLINK (pin 6 of U88) is low. BLINK is held low when the blink option is not selected. The output of U60 is in turn gated with the video output of U41 in U74, an exclusive OR gate. U74 thus inverts the video if the output of U60 is high, and no inversion takes place if the output of U60 is low.

The video signal including the cursor, is gated to pin 9 of another U74 exclusive OR gate in the absence of any blanking signals at the other two inputs to NOR gate U59. If S1-4 is open, U74 inverts the video signal to produce a reverse (black on white) display. Raw video on pin 8 of U74 is supplied to pin 15 of J4. Video out on pin 6 of inverter U87 is combined with COMP_SYNC on pin 8 of another U87 inverter in a resistive mixer, R80-R82, to meet EIA composite video signal standards, and coupled to P1 for use by a video monitor. This mixer has a 61-ohm output impedance.

Both Beginning Address Counter U1 and First Screen Position Counter U11 are enabled to advance their counts when pin 9 of J-!K flip-flop U75 is low, which it is for about 600 nsec following !OVERFLOW_LINE; that is, after the Scan Counter (U40) is loaded. This, of course, occurs at the end of every scan line in the character row.

The scroll circuit consists of U1, U11, Scoll Control Latch U2 and Screen Position Control Latch Ul3 and their associated circuitry. U1 and U11 are up and down counters respectively that are pre-

set to the outputs of latches U2 and 13. U2 latches the starting row address from DIO0-3 and U13 latches the data on DIO4-7, with !PORT_OUT_FE being the strobe. Data on DIO4-7 specifies where the first line will be displayed. Thus, the number loaded into U1 is the address of the first displayable scan line, and the number loaded into U22 defines the character row (0 through 15).

U11 is preset by !VDISP from pin 9 of J-!K flip-flop U43. This means U11 is forced to its preset condition from the end of the displayed text to the top of the next character row. During this time, pin 6 of another U43 J-!K flip-flop is set high to preset U1. If U11 is preset to 0, its TC output on pin 7 is low and pin 6 of U43 is reset to a low. This allows U1 to count with each horizontal scan line.

If U11 is preset to any number other than 0, pin 6 of U43 cannot be reset low until U11 reaches zero. Assume U11 is preset to two. It must count down two character rows before U1 starts counting. During this time, pin 7 of U43 (PRE_BLANK) is low, and as previously discussed, the display is blanked.

We can now see that the PRE_BLANK time, often called "window shade", is variable with the number loaded into U11. Therefore, scrolling is performed by changing the numbers in U2 and U13 without the need to reposition the text within the Display RAM.

The remaining circuit in the Display Section consists of transistor Q2, one section of U87, 89 and 102. U88 and U102 are connected as a one-shot 250 msec timer that is triggered when !PORT_OUT_FE goes active (pin 1 of inverter U87 goes high). Thus, when data is loaded into U2 and U13, this timer starts. Tri-state driver U89, which is enabled by !PORT_IN_FE, transmits the state of this timer to D100 on the Bidirectional Data Bus. The CPU can consequently test the timer status by looking for a high on DIO0. This timing allows a 250 msec scroll rate without the need for complex timing routines in the CPU. Q2, R102 and C37 serve to speed up timer reset.

8.5.5 Audio Tape I/O

Refer to Audio Tape I/O Schematic in Section X, Page X-19.

Timing for the Audio Tape I/O is derived from the 1200, 2400, 4800, 19,200 and 38,400 Hz signals received from the Baud Rate Generator in the Input/Output section of Sol. The first two are used by the write data synchronizer (U100) and the digital-to-audio converter (U101).

The remaining three signals are fed to two sections of U111, a quad multiplexer or select gate. All four sections of U111 are used to select clocks for low speed or high speed operation according to the select inputs, pins 9 (A) and 14 (B). The states of these two select inputs must be complementary to each other in order to select

the high or low speed clocks. Specifically, A must be high and B low to select high speed clocks; the converse condition selects low speed clocks. The select inputs are supplied by TAPE_HI_SPEED and !TAPE_HI_SPEED.

The output of the second section on pin 11 of U111 is BYTE_ WRITE_CLOCK, 4800 Hz on low speed and 19.2 KHz on high speed. The third section outputs a 19.2 KHz (high speed) or 38.4 KHz (low speed) timing signal to input pin 10 of binary up counter (U112).

RECOVER_CLOCK is produced by a phase locked loop (U110), another U112 binary up counter and the first and fourth sections of U111. The signal input (pin 14) to U110 is supplied from output pin 1 of D flip-flop U113. It is a constant frequency, regardless of whether one or two transitions are detected in the read data during the count out time (12 counts) of the U112 counter with outputs on pins 13 and 14. A phase comparator in U110 compares the signal input to the output of a voltage controlled oscillator (VCO) in U110 (pin 4). By feeding the VCO output through a counter (the other half of U112) before feeding the counter output back to the compare input (pin 3) of U110, the circuit acts as a frequency multiplier. The output of this circuit remains locked, therefore, to a multiple of the signal input on pin 14 of U110.

The output of U110 is nominally 19.2 KHz. The actual output is determined by the signal input which in turn is a function of tape speed. In other words, the phase lock loop circuit tracks input frequency variations. And it will track such variations within its locking range which is determined by the setting of variable resistor VR3 (connected to pin 12 of U110).

For high speed, the divide-by-four output of U112 (pin 4) is selected as RECOVER_CLOCK. For low speed, the VCO output of U110 is selected for RECOVER_CLOCK. This clock serves as read clock for the CDI UART, U69.

CDI control involves !PORT_IN_FA, !PORT_IN_FB, !PORT_OUT_FB, TAPE_CONTROL_1 and _2, POC (power on clear), TAPE_HIGH_SPEED and !TAPE_HI_SPEED. The last two were previously explained in the discussion of U111. !PORT_IN_FA strobes the CDI UART status (DR, TBRE, OE and FE--refer to Page VIII-22 for definitions) to the Internal Data Bus, INT3-7. !PORT_IN_FB strobes received data on pins 5-12 of U69 to the Internal Data Bus, INT0-7. !PORT_OUT_FB loads data from the Bidirectional Data Bus (DIO0-7) into U69. POC simply resets U69 whenever power is applied to the Sol.

TAPE_CONTROL_1 and _2 are used to turn one or two recorder motors on and off. An active low TAPE_CONTROL_1 energizes K1 to close its contacts and turn recorder #l on; a high de-energizes K1 to turn the recorder off. TAPE_CONTROL_2 does the same thing with K2 to control another recorder. Diodes D13 and 14, which shunt K1 and K2

respectively, prevent damage to the logic circuitry in the Input/ Output section due to inductive kickback. R155 and 156 are current limiters that keep the relay contacts from "welding" together.

When the CDI is in the write mode, data is input to the UART (U69) under control of !PORT_OUT_FB. Upon completion of this strobe, the transmit sequence is initiated within the UART, with the transmission rate being governed by BYTE_WRITE_CLOCK.

The transmission sequence begins with a start bit, a low (data zero) on the UART's TO output. It is followed by eight data bits and two stop bits (high on the UART's TO output), with the number of bits being fixed by the connections to pins 34 through 39 of U69.

The data from U69 is applied to the D input of D flip-flop U100 which is clocked at 1200 Hz. Consequently, the output on pin 1 of U100 follows the input data on pin 5 after the rising edge of the 1200 Hz clock. This output is connected to the reset (pin 4) of U101, so when the data out of the UART is high, the first section in U101 is forced to a reset condition. In this condition the J and K inputs to the second stage of U101 are held high which allows the flip-flop to change state on the rising edge of the clock.

The clock for U101 (OUTPUT_CLOCK) is 2400 Hz in the high speed mode or 4800 Hz in the low speed mode. This clock is derived from 2400 Hz in conjunction with the low speed select signal in NAND gate U98 and exclusive-OR gate U99.

In the high speed mode, pins 12 and 13 of U98 are held low, thus holding pin 10 of U98 high. As a result the 2400 Hz signal is inverted in U99 to become the clock for U101.

Pins 12 and 13 of U98 are held high, however, in the low speed mode to enable U98. In this case R117 and C47 provide a delay in the U98 gate. When the 2400 Hz signal on pin 2 of U99 changes state, so does pin 3 of U99. Also, C47 charges through R117 for several usec, at which point pin 10 of U98 is brought to the opposite polarity. The output from U99 then goes high. A series of positive pulses, with a pulse width approximately equal to the R117, C47 time constant (10 usec) and occuring at every transition of the 2400 Hz signal, appears on pin 3 of U99. This circuit thus operates as a frequency doubler in the low speed mode to provide a 4800 Hz clock for U101.

The 2400 Hz signal from which the U101 clocks are derived also produces the 1200 Hz clock signal for U100. As a result the 1200 Hz signal changes state following a propagation delay after the 2400 Hz signal falls.

As previously stated, the second stage of U101 is allowed to change state on the positive going transitions of the OUTPUT_CLOCK as long as the data out of the synchronizer is a "1". The end result is an output on pin 14 of U101 that is one-half the clock frequency (1200 Hz and 2400 Hz in the high and low speed modes respectively).

Assume the data stream out of the UART goes low ("0"). On the next rising edge of the 1200 Hz signal, U100 will reset with Q low and !Q high. A low reset on pin 4 of U101 enables the first U101 stage to toggle on the next rising edge of the OUTPUT_CLOCK which occurs 1/2400 second after the synchronizer output falls. Remember that OUTPUT_CLOCK moves from a low to a high shortly before the 1200 Hz signal did. The reset on pin 4 of U101 is thus removed slightly after the OUTPUT_CLOCK occurred. With the J and K inputs to the first U101 stage high, its output will change state on each succeeding low to high transition of OUTPUT_CLOCK. The second U101 stage in turn can only toggle on the positive going transition of OUTPUT_CLOCK when its J and K inputs are high. Since the inputs are high at one-half the clock rate, by virtue of the first U101 stage, the second U101 stage toggles at one-fourth the OUTPUT_CLOCK rate.

The two sections of U101, therefore, operate as a frequency divider, dividing the OUTPUT_CLOCK by two when the write data is a "1" and by four when the data is a "0". Thus, in the low speed mode, four cycles of the 1200 Hz represent a "0" and eight cycles of 2400 Hz represent a "l". In the high speed mode, one cycle of 1200 Hz represents a "1" and one-half cycle of 600 represents a "0".

The output on pin 14 of U101 is applied to one section in U109 which provides sufficient current drive for the divider network. This divider and a jumper arrangement allow selecting one of three outputs to be fed to the audio output jack J6. The I-to-J jumper selects a 500 mv signal for the auxiliary input to an audio recorder; the I-to-H jumper selects a 50 mv signal for the microphone input to an audio recorder.

When the CDI is in the read mode, data from the recorders enters on J7. This input is fed to the negative input (pin 6) of operational amplifier U108.

The first section of U108 is a high gain amplifier, with its gain (approximately 100) being determined by R142 and R143. The output from this amplifier is coupled to input pin 2 of the following U108 stage and the base of a Darlington pair (Q4 and Q5) which provides high current gain.

Current into the base of transistor Q5 causes C67 to discharge. (C67 charges through R39 to 5 V dc.) The voltage on C67 in turn controls the gate of field effect transistor (FET) Q3. Q3 functions as a variable resistor which can be changed by its gate voltage. Since Q3 is connected between ground and the input network to the

first U108 stage, it serves as a variable shunt. A low gate voltage on Q3 decreases the shunt resistance and the input to U108. In a like manner, a high voltage on C67 results in an increased input to U108. 03, Q4 and Q5 with their associated circuitry, therefore, serve as an automatic gain control (AGC) circuit which limits the input to the second U108 stage to approximately a positive 2 volt peak signal.

The second stage of U108 is a comparator with hysteresis that performs the needed audio to digital conversion. Feedback resistor R147, in conjunction with R145, establishes the level on the positive input (pin 3) of U108. This level, be it positive or negative, is the threshold voltage, ±50 mv, which the negative input (pin 2) must exceed in order for the output of U108 to switch levels, positive to negative and the converse. Since the feedback loop is regenerative, U108 switches at its maximum rate, and U108 switches on each transition of the audio signal input. It is in this manner that U108 performs the audio to digital conversion.

The digital output of U108 is inverted in one section of inverter U109 and applied to pin 9 of exclusive OR gate U99 which is connected as a buffer without inversion. If the output of U109 is low, the output on pin 10 of U99 is also low and the output on pin 4 of another U99 exclusive OR gate is high. The voltage across C49 under this condition is minimal. When the output of U109 goes high, C49 starts to charge through R118 until pin 9 of U99 crosses the threshold of that gate. At this point pin 10 of U99 goes high, and since the two inputs to the second exclusive-OR gate are both high, pin 4 of U99 goes low. C49 now discharges because pins 9 and 10 of U99 are at the same level so that the circuit can repeat the operation on the next high to low transition at pin 4 of U109. R118, C49 and U99 consequently serve as a transition detector that produces a pulse less than one microsecond long for each transition of the output on pin 4 of U109, regardless of the polarity of the transition.

Transition pulses from U99 clock both D flip-flops in U113. A transition pulse clocks the top U113 at pin 3 which sets Q (pin 1) high and Q (pin 2) low to enable up binary counter U112 on pin 15. Pin 1 is applied to the T) input (pin 9) of the lower U113 and the circuit remains in this state until one of two things occurs: 1) a second transition pulse arrives before U112 reaches count 12 or 2) U112 reaches count 12.

If a second transition pulse arrives before count 12, the bottom U113 stage is set and presents a "1" to the D input (pin 9) of flip-flop U100. This is clocked by the !Q output on pin 2 of U113 as a low to pin 12 of U100.

If a transition pulse does not arrive before count 12, the bottom U113 stage outputs a "0" to input pin 9 of U100. On count 12, the C and D outputs of U112 go high to reset U113 by way of U98 at pin 4. As a result the U100 clock goes high, as does pin 12 of

U100. The output on pin 12 of U100 is inverted by U109 and applied to the receive input (pin 20) of the UART.

The Q output on pin 1 of U113, which occurs at the actual bit rate of the incoming data, is also used by the receive clock circuitry to reconstruct the receive clock from the data signal. Received data undergoes serial-to-parallel conversion in the UART and is placed on the RO1-8 data outputs of the UART when ROD (pin 4 of the UART) is low (!PORT_IN_FB active) and onto INT0-7. Four status outputs from the UART can also be enabled when SFD (pin 16) is low. These four bits are FE (framing error), OE (overrun error), DR (data ready) and TBRE (transmitter buffer register empty).

8.6 KEYBOARD

8.6.1 Block Diagram Analysis

A simplified block diagram of the keyboard is provided on Page X-25 in Section X.

The Clock Oscillator produces the basic timing signals for the keyboard, and they are distributed as indicated.

At the heart of the keyboard is a Key Switch Capacitive Matrix which can be viewed as a 16 x 16 X-Y matrix, with X being the column and Y the row. Conceptually, a key depression increases the capacitance between the X and Y coordinates that uniquely define that key.

The Column Scanner supplies a pulse train to the X lines in the matrix, with only one line being pulsed at any given point in time. When a key is depressed to increase the capacitance between the Column Scanner output and a Row Scanner input, the X-Y coordinates for that key are detected to provide an input to the Sense Circuit.

The Sense Circuit in turn generates an input to the Sequence Detector when a key closure occurs. This detector basically detects key closures and count cycles of the Row Scanner to discriminate against false key signals and insure that valid closures are serviced in order.

In the absence of key closures, the Sequence Detector feeds PKD to the Sense Circuit to increase its threshold. This action serves to increase the circuit's noise immunity. On valid key closures, the PKD input is such as to decrease the Sense Circuit's threshold. When valid key closures exist, the Sequence Detector strobes data into the Output Latch. The low order four bits to this latch are supplied by the Row Scanner; the high order four bits are

supplied by the Encoding ROM, with the data being determined by inputs from the Column Scanner and Function Latch Decoder. This strobe (Data Out) also enables the Strobe Generator to output !STROBE a 6 usec pulse that signals the Sol CPU that the Keyboard is ready to send data.

Eight bits of keyboard data (KBD0 through KBD7) are stored in the Output Latch. KBD0 through KBD6 represent the ASCII code for the character associated with the key closure, or closures, that initiated the Data Out strobe from the Sequence Detector. KBD7 is used only for special control characters (e.g. MODE SELECT, CLEAR and cursor movement) that are recognized by the Sol program. The data on KBD0-7 is input to the Sol CPU when it issues !PORT_IN_FC (refer to Paragraph 8.5.2 on Page VIII-14).

The Repeat Counter is enabled when the REPEAT key and a character key in the Key Switch Capacitive Matrix are pressed at the same time. When this occurs, Key Out (initiated by the character key closure) is active, and the Repeat Counter generates a periodic Repeat Strobe. This strobe disables the Sequence Detector and causes the Strobe Generator to output repetitive !STROBE pulses. Column 30 also prevents the Sequence Detector from strobing additional data into the Output Latch.

The Function Latch and Decoder latches and decodes the Low Order Count from the Row Scanner when the "function key" column in the Switch Matrix is selected by the Column Scanner. It then outputs, as appropriate, !LOCAL, !RST and !BRK to J1 and SHIFT/SHIFT_LOCK, UPPER_CASE and CONTROL bits to the Encoding ROM. The latter three supply three of the seven address bits to the ROM which specify the high order four KBD bits (KBD4-7).

All keyboard outputs are supplied to J1 which is connected to J3 on the Sol-PC.

8.6.2 Circuit Description

Refer to the Keyboard schematic in Section X, Page X-23.

Keyboard operation is controlled by a 3 usec clock circuit consisting of NAND gate U7, R7 and C7. U7 is connected as a Schmitt trigger inverter with negative feedback through R7 and C7. The output on pin 11 of U7, a square wave with a 3 usec period, is inverted in U4 (a NAND gate connected as a simple inverter) and applied to the clock input (pin 11) of U8. U8 operates in a toggle mode by virtue of feeding its !Q output on pin 8 to the D input on pin 12. Thus, its output state changes on each clock to produce a 6 usec and an inverted 6 usec clock on pins 9 and 8 respectively.

Each of these outputs is connected to a section of U7 where each is AND'ed with the 3 usec clock. This generates two negative going clocks at pins 8 and 6 of U7. These outputs are called !ϕ1 and

!ϕ2 respectively. This circuit thus generates a symmetrical two phase clock, with each phase having a 6 usec period with a 1.5 usec negative going pulse.

!ϕ1 advances the cascaded ripple counter, U5 and 6, in the Column Scanner circuit (U5, U6, NAND gates U4 and decoders U17 and U21). U6 divides !ϕ1 by two on each advance. The output on pin 12 is consequently a square wave with a 12 usec period, the output on pin 9 is a square wave with a 24 usec period, and so on to pin 11 which has a 96 usec period. The output on pin 11 is then divided by two in U5 to provide 192, 384, 760 and 1536 usec periods. We will call these Clock_1 for the 12 usec period, Clock_2 for the 24 usec period, Clock_4 for the 48 usec period, and so on from Clock_8, _16, _32, _64 and _128.

Clocks_16, _32 and _64 are applied to the A, B and C inputs of binary-to-decimal decoders U17 and U21. In order for these decoders to yield outputs, their D inputs (pin 12) must be low. U4 is used to enable one or the other of these inputs, with Clock 128 being the determining factor. When Clock_128 is low, U17 is selected through U4 when !ϕ1 is high at pin 4 of U4. U21 is selected when Clock_128 is high and !ϕ1 is high at pin 13 of U4. By AND'ing !ϕ1 and Clock_128, neither decoder is selected when !ϕ1 is low, the time U5 and U6 count. During this time false binary signals can appear on the outputs of U5 and 6.

The net effect is that only one of the 15 outputs from U17 and 21 will be low, and this low advances on each count advance. The low outputs of U17 and 21 drive the column lines in the key switch matrix.

Clocks_1 through _8 are connected to analog multiplexers U19 and U22. Only one channel from input to output is connected at one time. Note that Clock_8 and !Clock_8 from U6 enable U19 and U22 respectively. U19 and U22 (the Row Scanner) thus scan through the 16 rows in the sequence indicated by the numbers contained within the "boxes" of the key switch matrix. An entire scan of the rows is made before the next column is selected by U17 and 21.

We now have U17 and U21 driving the column lines and U19 and U22 testing each row line by connecting it to an input to the Capacitance Key switch (KTC) Detector. These two inputs are normally high at 5 volts. Within the switch matrix there is a small capacitance connected between each column and row line; that is, there is a capacitance associated with each key on the keyboard. When a key is depressed on the keyboard, the capacitance associated with that key increases. When the column and row lines associated with that key are selected, there is a significant voltage difference between the two and the capacitance charges to produce a small negative going spike at the input to the Capacitance Keyswitch Detector.

This detector circuit consists of three transistors, Q7, Q8, and Q9 (connected as a linear amplifier with negative feedback) followed by Q4 and Q2. Q4 and Q2 are large signal amplifiers biased in their cut-off region. The input to the detector is selectively connected to +5 V dc by way of the analog multiplexers (Ul9 and U22), the row matrix wires, and the 33K resistors. A key depression causes a negative current pulse through R16 to the base of the input amplifier transistor, Q8, which is biased near cut-off. The pulse is then amplified by Q8 with inversion to appear as a positive pulse at the input of Q7. Q7 is an emitter follower circuit which gives a positive pulse at its output, across R18, at a low impedance. This signal is coupled back to the input through transistor Q9, a common base amplifier which has its base clamped to 2.5 V dc by zener diode CR4. When the positive pulse appears at the emitter of Q9, it is amplified without inversion and applied to the input of Q8. Since the original input was a negative pulse, the positive pulse constitutes negative feedback. The output across R18, a positive pulse, is further amplified by pulse amplifier transistor Q4, a common base amplifier that is normally biased off. The output stage Q2 is biased in the cut-off region also, but a sufficient positive pulse from Q4 will cause Q2 to conduct to give a negative pulse output across R12.

Transistors Q1, Q6, Q5 and Q3, represent a second pulse amplifier circuit that is analogous to transistors Q9, Q8, Q7 and Q4 respectively. The output of this second amplifier, which appears at the collector of Q3, is also connected to the base of the output transistor Q2. An input pulse from either Ul9 or U22 will therefore supply an amplified negative pulse to pin 13 of NOR gate U14.

The !PKD signal through R24 helps to set the threshold at the base of Q4 and Q3. This threshold is normally high when !PKD is high, so the output from Q7 and Q5 has to overcome a higher threshold at the emitter of Q4 and Q3 in order to cause conduction of Q4 and Q3. On the second such pulse on the same count address, !PKD goes low to reduce the threshold at the bases of Q4 and Q3. This sensitizes the circuit, acting as a positive feedback path, and gives an output. Thus two consecutive detections of a key stroke are necessary to give an output. This feature provides noise immunity since a single noise pulse will not pass through the amplifier. The complete key switch matrix is scanned at a very high rate compared to the time it takes to physically press and release a key. Thus a key closure will be detected, even though the key is not held down for any appreciable time.

Two sections of NOR gate Ui4 are connected as a cross-coupled flip-flop. A low on pin 13 of Ui4 sets output pin 11 of U14 high, providing that the low is longer than 1.5 usec (which it is when a valid key closure is detected). That is because !ϕ1 is applied to pin 9 of U14. !ϕ1 effectively prevents switching noise, which is short in duration, from being interpreted as a key closure. The high, let's call it KEY, on pin 11 of U14 will remain until !ϕ1 again goes low about 4.5 usec later.

KEY is fed to pin 5 of 8-input NAND gate U25, pin 9 of ROM U20 and pin 1 of NAND gate U27. Let's examine the other inputs to U25.

KEY, as mentioned, is fed to pin 9 of U20 which is a 256 x 4 bit static ROM. Only two bits are used. For each possible row-column combination, there is one storage location in U20. DI1 and DO1 (pins 9 and 11) are the input and output respectively of one bit location; DI2 and DO2 serve the same functions for the other bit location. The row count is applied to A0-4 and the column count is applied to A5-7 to address U20.

When a key closure is detected, the counts are presented to U20 continuously. When the counts change shortly after the failing edge of !ϕ1, U20 outputs the status of the address that is already stored in the ROM about 1 usec later on pin 10. On the rising edge of ϕ1 after the address change, the status on pin 10 is latched in one-half of D flip-flop U26 and presented at output pins 9 and S. About 1.5 usec later the R/W signal on pin 20 of U20 goes low, and the KEY signal on pin 9 enters the specified location in U20. Note that this KEY is related with the new count address. The key stored in U26 represents the preceding address. We consequently call the KEY in U26 "KEY_minus_1", and it is applied to pin 11 of U25.

The remaining inputs to U25 are 1) ϕ2 (an inverted !ϕ2) on pin 12, 2) a repeat strobe signal on pin 4 (supplied by pin 11 of NAND gate U16 which is high without a repeat command), 3) PKD_minus_1 on pin 6 (supplied on pin 3 of U26 which is low if three or more count cycles have occurred since one key closure), and 4) the column output on pin 4 of U17 which is applied to pins 1, 2 and 3. The last signal drives the column associated with the special function keys on the keyboard (SHIFT, SHIFT_LOCK, LOCAL, BREAK, UPPER_CASE, REPEAT and CONTROL).

In order for U25 to output a low on pin 8, therefore, we need a current KEY, a KEY from the preceding count cycle, no repeat function, no drive on pin 4 (column 30, hexadecimal), and we must be on the second count cycle during the current key depression.

With these conditions satisfied output pin 3 of U25 goes low. It is inverted by U10 to a high on pin 11. This signal then clocks the output latches, U1 and 2. On this signal, the data present on the inputs are latched into U1 and 2, and it remains latched until the next output on pin 8 of U25 occurs.

A low on pin 8 of U25 also resets one-half of D flip-flop U11 at pin 13 which causes output pin 9 to go low. On the rising edge of the inverted 6 usec clock from US, the second U11 stage sets and out-

put pin 5 goes low to clear the first stage. The high on output pin 6 is inverted by NAND gate UIO to supply a low active !STROBE on pin 3 of J1. (Note that J1 on the keyboard connects to J3 on the Sol-PC.) The next inverted 6 usec clock resets the second U11 stage. We thus have a 6 usec strobe pulse following the latching of data into U1 and U2.

The complement of KEY_minus_1 on output pin 8 of U26 is fed to input pin 10 of NAND gate U16 and is translated to a high on pin 8. The other input on pin 9 is high at this time since it is driven by the signal which indicates the third count cycle. A three-input NAND gate, U27, thus has a high on pin 2. A second input on pin 1 is KEY which is active (high) from the first count cycle of the key closure. The remaining input on pin 13 is supplied by pin 11 of U16, and it is low only when the repeat function is operating. U27 is consequently satisfied and outputs a low on pin 12.

This low appears at pin 5 of NOR gate U16. Pin 4 of U5 is high at this point by virtue of a low on pin 1 of U16 which indicates the third count. Thus, the high on pin 6 of U16 will be stored in the second bit location U20 when !ϕ2 goes low at pin 20 of U20. When this happens D02 (pin 12) of U20 goes high to indicate the new status of this bit.

The D02 output is inverted in U10 and applied to input pin 2 of another U26 D flip-flop and to the Capacitance Keyswitch Detector as PKD. PKD serves to lower the detector threshold; that is, the detector offers less "resistance" to its input. This is positive feedback that allows the detector to discriminate between noise and a key closure. Note that two key closures are required before the detector threshold is lowered.

The inverted D02 output from U20 also appears at the D input (pin 2) of U26. Since this flip flop is clocked by !ϕ1, the prior status of !PKD, called "!PKD_minus_1", is already present in this latch on output pin 5. If we are on the second count cycle of a key closure, pin 5 is high. If we are on the third count or more, it is low to inhibit U25. As previously mentioned, !PKD_minus_1 is also connected to the NOR gate (U16) used to feed data to pin 11 of U20 from KEY_minus_1.

When the current KEY signal is released, pin 12 of NAND gate U27 and pin 5 of NAND gate U16 go high. The U16 NAND gate that inputs to pin 4 of U16 looks at KEY_minus_1 on pin 2 and the complement of !PKD_minus_1 on pin 1. Thus, pin 1 is high for the first one and a half counts and pin 2 is high for the first count. Upon release of KEY, therefore, pin 3 of U16 is low for the first count. On the second count, KEY_minus_I goes low--as do pin 6 of U16 and pin 12 of U20. On the next !ϕ2 clock, the data is read into U20. The output on pin 12 of U20 changes to remove !PKD which increases the Capacitance Keyswitch Detector threshold for greater noise immunity. It also sets !PKD_minus_1 on pin 5 of U26 on the third count cycle

following release of KEY. On the third cycle the circuit reverts to its original state.

This circuit, comprised of U20, U26, U16 and U17 serves two functions. By requiring two events during two consecutive count cycles before generating a KEY, it discriminates against false key closures. It also insures that multiple key strokes are serviced in order. (This is the n-key rollover feature.) That is because the row-column addresses are continuously presented to U20 and this circuit's cycle can occur for each possible key closure. U20 can thus contain data for all possible key closures, and the data will enter U1 and U2 on the KEY generated for each closure as the row-column count progresses.

The previously mentioned column 30 output on pin 4 of U17 drives the keyboard control key "switches". Data for these key closures, present on pins 1, 2 and 3 of addressable latch U12 is latched in U12 during Clock 8 and ϕ2 when column 30 is driven. Pin 13 of U12 is connected to the complement of PKD_minus_1. Thus, the data (active low) is strobed into U12 on the first count cycle. During the third count it will be strobed again and a high is read in. When the key is released, a low is strobed in again. As a result, a high active pulse appears on the output line related to the key that was closed for the duration of the key closure.

SHIFT and SHIFT_LOCK, on pins 11 and 10 respectively, are applied through U23 inverter stages to NOR gates U13 and U14. These are connected as a cross-coupled flip-flop. An active SHIFT sets this flip-flop at pin 5 of U13 to make output pin 6 of U13 and output pin 3 of U14 high. The latter is connected to pin 3 of U18, a 512 x 4 bit ROM. U18 is programmed to output the high-order four bits of the data to U1 according to the states of pins 1, 2 or 3.

The U13-14 flip-flop is set to a high on pin 6 if SHIFT_LOCK is active. As can be seen, the shift bit to U18 is high by virtue of the low on pin 6 of U13 and it will remain so until SHIFT again causes U13-14 to change state. When output pin 6 of U14 is high, pin 12 of U24 is low to turn light emitting diode LED1 on. This LED is located in the SHIFT_LOCK key and indicates the keyboard is in a locked shift condition.

When UPPER_CASE is active, pin 7 of U12 goes high to clock D flip-flop Ul5 on pin 3. This flip-flop is connected to operate in a toggle mode. On the UPPER_CASE "clock", pin 5 of U15 goes to make pin 2 of U18 low. The high on pin 6 of U15 is inverted by U24 to turn on LED2. LED2 is located in the UPPER CASE key. A second closure of this key toggles U15 to the opposite condition.

Now assume the LOCAL key is depressed, the output on pin 5 of U12 goes active high to clock the other D flip-flop U15 stage at pin 11. This stage also operates as a toggle, and output pin 9 goes low to become LOCAL on pin 14 of J1. Again, the high on output pin 8

causes LED3, the LOCAL light, to turn on. A second closure of the LOCAL key toggles this section of U15 to the opposite condition. Note that LOCAL has no affect on keyboard data.

The other outputs from U12 are BREAK (pin 12), CONTROL (pin 6) and REPEAT (pin 9). BREAK is inverted in U23 to become !BRK on pin 4 of J1. CONTROL is applied directly to input pin 1 of U18 so that the control character related to the low order bits enters U1 and U2.

REPEAT is applied to pins 10 and 11 of NAND gate U27 and pin 13 of NAND gate U16. The input to U27 is gated with UPPER_CASE to generate !RST at pin 13 of J1. This means, of course, that REPEAT and UPPER_CASE must be depressed at the same time to generate !RST.

On pin 13 of U16, REPEAT enables that gate so that U16 transmits the output on pin 9 of U9. U9 is connected as a two-stage shift register whose input (pin 2) is ground. It is clocked by clock_128 from U5.

U9 is initially set with output pins 5 and 9 high during the third count cycle by PKD_minus_1. This is also the time when U12 outputs data. If the key is released, U9 clears to a low on pin 9 five count cycles following KEY. If the key is held down, U9 cannot shift since PKD minus I remains on preset input pins 4 and 10.

When REPEAT exists at pin 13 of U16, pin 11 of U16 is low to inhibit U25 and U27 at pin 13. This prevents further KEY signals and disables the n-key rollover circuitry. The low on pin 11 of U16 is also inverted by open collector inverter U24 to enable the repeat oscillator (timer U3, R4, R5 and C3). U3 generates a square wave on pin 3 with a period determined by the RC network.

This clocks the first stage of D flip-flop U11, the !STROBE generator, and U11 produces the previously discussed 6 usec !STROBE. U11 continues to generate !STROBE at the repeat oscillator rate until either the REPEAT or character key is released. And with each !STROBE, of course, the data associated with the character key is latched into U1 and U2.

Eight ASCII-coded data bits are output by U1 and U2 to J1 as indicated. Seven bits (0-6) are used for ASCII characters, and the eighth bit (7) is set only for certain control characters that are recognized by the Sol program. These are used for control functions such as MODE_SELECT and cursor movement.

The remaining circuit, R32 and C14, initializes the keyboard when power is applied. That is, it resets the output latches and the SHIFT/SHIFT_LOCK, UPPER_CASE and LOCAL flip-flops. It also inhibits STROBE at pin 1 of NAND gate U10.

SECTION IX

SOFTWARE

Sol TERMINAL COMPUTER™

9.1 CONSOL

CONSOL is a 1024 byte program designed to allow the Sol TERMINAL/COMPUTER to operate as a standard CRT terminal and to provide access to the essential computer capabilities of the Sol. Using CONSOL, self test and small diagnostic programs can be entered to system memory and executed. This in addition to providing verification of correct system operation helps in finding errors in case of a malfunction.

In addition, CONSOL contains standardized entry points for all normal I/O operations. These routines are common with all Sol System Software allowing each personality module in the Sol line to interface with external programs in an almost identical manner.

A cassette read routine is also resident in the CONSOL module allowing Sol Software to be loaded and run in a system with additional memory. Sol System Software as of November 1976 includes BASIC, FOCAL, a Scientific Calculator and numerous "game" packages including a 8K assembly language version of STARTREK called TREK80.

When power is applied to the Sol unit, CONSOL initializes the system RAM area, clears the screen, and enters the terminal mode.

In this mode the Sol System acts as a standard CRT terminal sending keyboard data to an output port and displaying received data on the screen. The COMMAND KEYS of the keyboard are not transmitted to the output port but are interpreted as direct internal operation keys. CURSOR MOVEMENT, HOME and CLEAR SCREEN all operate in this manner, while MODE SELECT causes an immediate change in the operation of the unit.

When the MODE key is depressed CONSOL issues a prompt character (>) and waits for a command line to be input. The Sol is now operating as a computer and is ready to accept one of the following commands:

DUmp	Dump memory locations to screen
ENter	Enter data to memory
EXecute	Execute a program in external memory
BAsic	Execute a program located at address zero
TErminal	Return to terminal mode
TLoad	Load program or data from cassette tape
MODE	Press MODE SELECT key to start new command line

9.1.1 DUmp (addr) (addr)

The DUmp command displays memory data on the screen in a Hexidecimal representation. As with all Sol commands the command is recognized by the first two characters and up to ten additional characters can be input without an error being forced.

Thus, DU; DUST; DUMP; DUMPTHESE would all be recognized as being a DUmp command.

At least one address must follow the command or a error displaned on the screen. If two addresses are input then all values from the first address to the last will be displayed.

```
DUMP 0        EF
```

Up to ten blanks may be inserted between each parameter without forcing an error condition. Errors are indicated by a question mark (?) replacing the character where the error occurred. For example if the DU command were given without an address the question mark would appear ten spaces to the right of the "U".

9.1.2 ENter addr

The ENter command places sequential bytes into memory beginning at the specified address. Data, represented as hexadecimal values, are input from the keyboard for entry to memory. All CONSOL commands except MODE SELECT are executed when the RETURN key is pressed. After the ENTER, (address), RETURN sequence the Sol Displays a colon (:) prompt character. Values are then input one line at a time with each line terminated by a carriage return or linefeed. The ENter function itself is terminated with a slash (/) and the Sol goes back to the command mode when the slash is encountered.

With all command functions of CONSOL, input lines are terminated with a carriage return or line feed. If the terminator is a C/R, CONSOL will erase all characters from the current cursor location to the end of the screen line. In this case, all valid input should be to the left of the cursor. If an error occurred during input the cursor may be moved to the left using the "cursor-left" key and the erroneous characters changed. A linefeed would then be used as a terminator since LF does not erase the line prior to processing the characters. This is particularly useful when using the ENter command since the input line can be visually scanned and errors corrected prior to the actual entry of input data to memory.

9.1.3 TLoad (speed)

Included within COINSOL are routines to read standardized cassette tape Software which is recorded with a sixteen byte header that includes NAME, LOAD INFORMATION, FILE TYPE and execute address. CONSOL, because of space limitations, is unable to search for a

program or file by name. After receiving the TLoad command, CONSOL turns on the cassette player and waits for the next header, then uses the header information and loads the file to memory. The cassette recorder must be in play mode and properly connected before executing the TLoad command.

After loading the data, CONSOL returns to the command mode where the EXEC command can be used to execute the just loaded program. Also, a return can normally be made to the command mode by pressing the MODE SELECT key. Space limitations again limited escape during the header search, so if the system locks up in this routine the standard Sol restart must be used. To restart the Sol press UPPER CASE and REPEAT keys simultaneously.

The CUTS cassette interface electronics within the Sol will record or receive data at either of two standard speeds. TLoad will accept a parameter to select this speed, 0 being high speed and 1 being low. (1200 and 300 bits per second respectively). If no parameter is given CONSOL will default to high speed operation as all standard Processor Technology Sol-System Software is recorded at this speed.

9.1.4 EXecute addr

The execute command is used to run programs located in external memory. CONSOL branches to the external routine in a manner similar to an 8080 CALL instruction so the program can return to the command mode using a standard 8080 RET instruction if normal stack operations are used.

9.1.5 BAsic

The BAsic command is provided for executing programs whose starting address is 0, such as Sol-BASIC5.

9.2 STANDARD I/O ROUTINES

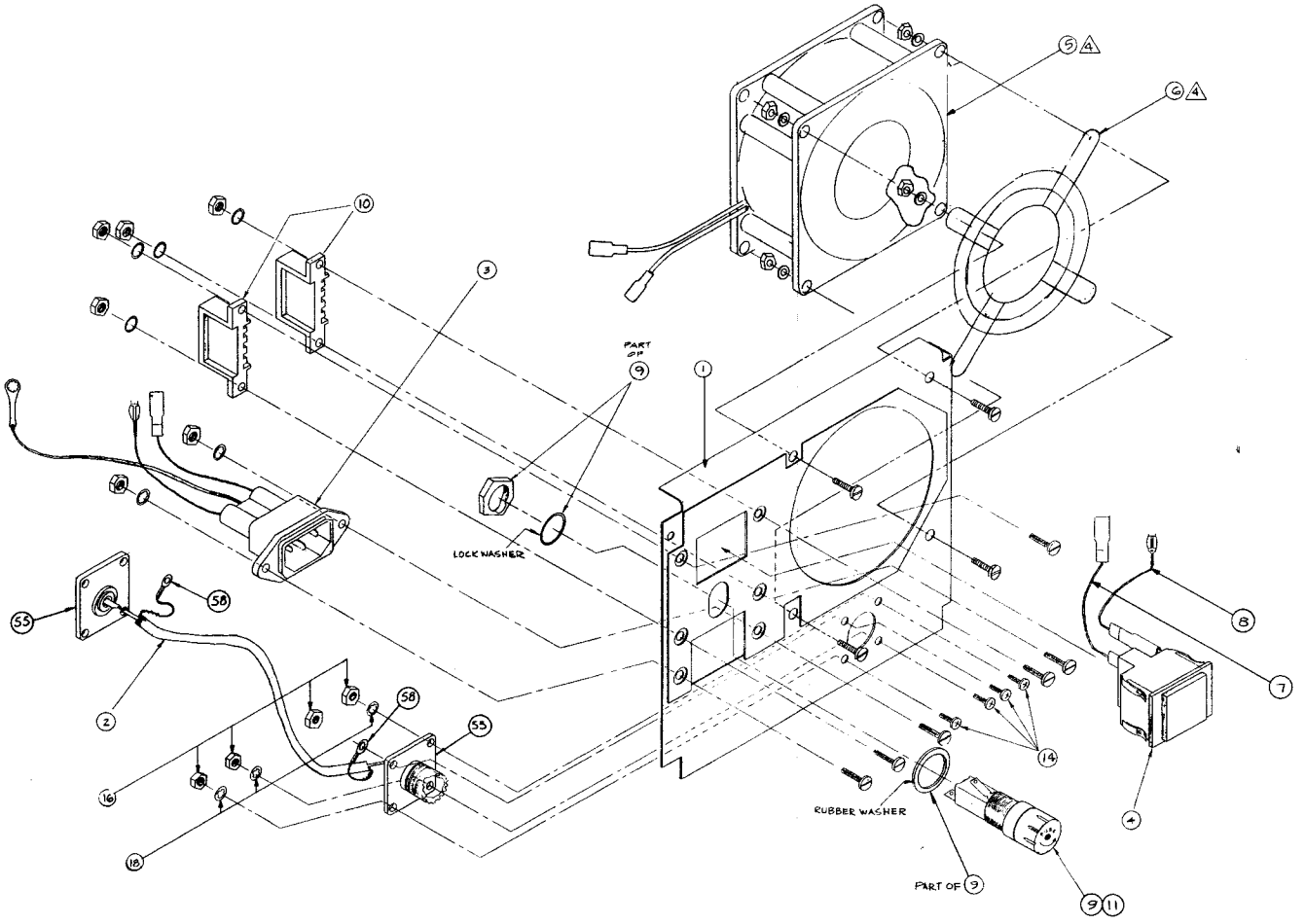
All Sol System personality modules contain similar I/O code for input/output operations. CONSOL, using 1K of memory, has routines for KEYBOARD and SERIAL PORT input as well as Serial Communications Channel and VIDEO DISPLAY OUTPUT. Although the same code for SOLOS and SOLED contains expanded functions, the I/O operations appear almost identical when used with external software.

Sol-BASIC5, for example, performs all I/O using the jump table of the personality modules. Thus, without altering BASIC the user may output to either the serial port or to the display screen. Provision is also made within BASIC to programatically change to any of the four available Input or Output options. CONSOL is of course limited to the two provided.

LTR	REVISION DESCRIPTION	DATE	APPROVED
B	ECN 10124 (DOCUMENTATION ONLY)	9-26-77	[illegible]
C	ECN 10226	12/14/77	[illegible]
D	ECN 10248	1/11/78	[illegible]

X-1

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL SCREWS ARE ITEM (18)
2. ALL LOCKWASHERS ARE ITEM (17)
3. ALL NUTS ARE ITEM (19)
4. USED ON -02 VERSION ONLY



REF DES	PART OR DWG. NO.	PART DESCRIPTION	QTY
HIGH ASSY.	USED ON		
105001-XX	101000-XX		

Processor Technology Corporation
2500 Ninth Street
Berkeley, CA 94608

DRAWN:	LTD / BS	DATE: 1. FEBRUARY 1978
DATE:	01-3-77	DATE: 14 AUG. 77
CHECKED:	LG	ENGINEER: Z. Zakovich
DATE:	8-16-77	DATE: 16 AUG 77

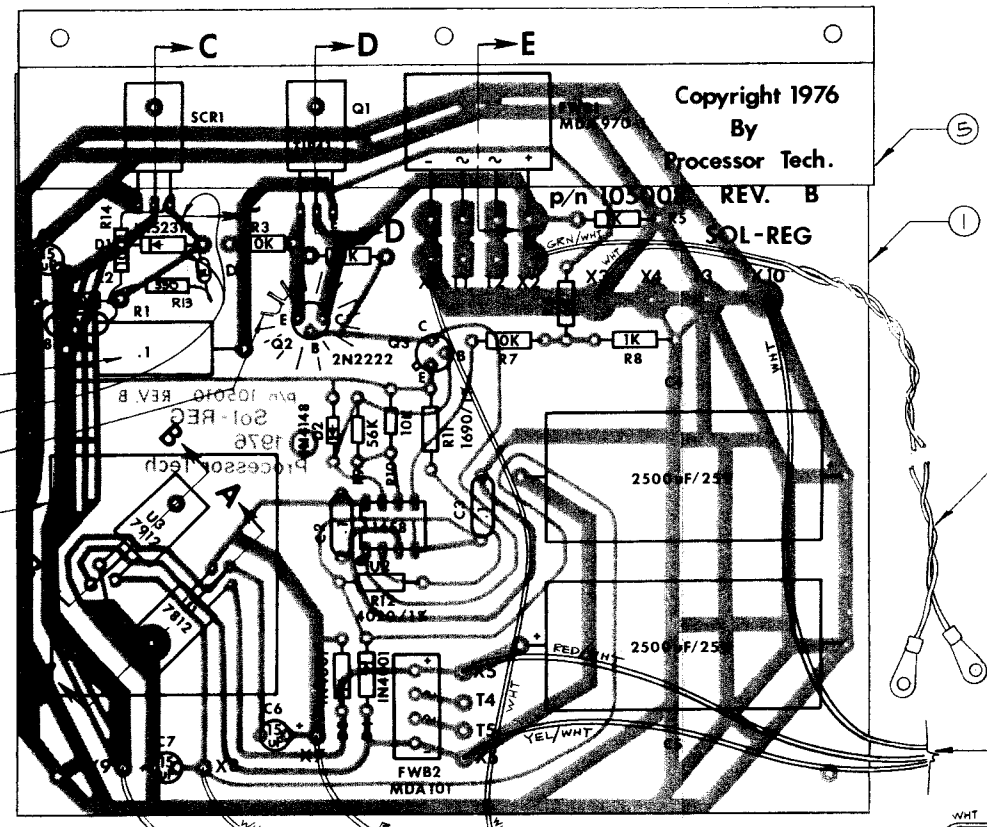
ASSEMBLY, FAN CLOSURE, 501

X-1

SIZE	DRAWING NO.	SCALE	REV
D	105014-XX	NONE	D
5/25		SHEET 1 OF 1	8SX

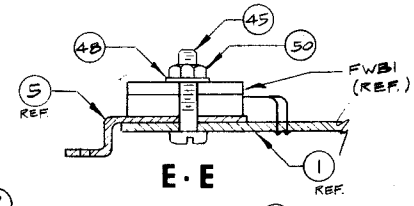
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
–	C	ECN 10124 (RE-DRAWN)	9-26-77	BMM
–	D	ECN 10242, 10244	1/11/78	

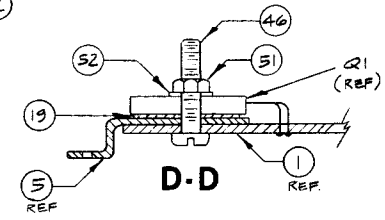
X-2

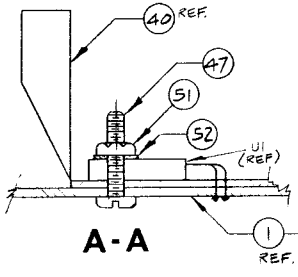


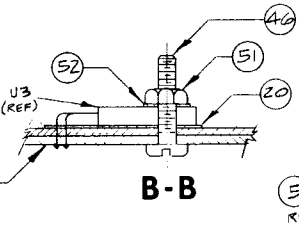
NOTES:

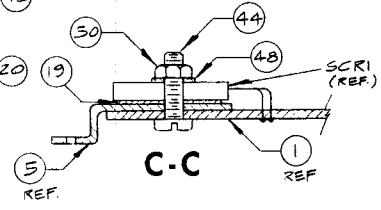
1. CUT THESE TRACES ON THE SOLDER SIDE OF THE PCB & ADD R13, R14 AND C8 AS SHOWN.
2. THIS IS A SINGLE SIDED BOARD. CONDUCTOR PATTERN SHOWN IS ON SOLDER SIDE ONLY.
3. MOUNT R1 APPROXIMATELY .15 FROM BOARD SURFACE.











REF DES	PART OR DWG. NO.	PART DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES:
TOLERANCES ARE:
FRACTIONS ± –
DECIMALS .xx ± – .xxx ± –
ANGLES ± –

ProcessorTechnology

DRAWN:	LITO	ENGR:	R. Mansell
DATE:	9-16-77	DATE:	9-28-77
CHECKED:	AS	RELEASED:	R. Mansell
DATE:	9-21-77	DATE:	1-28-78

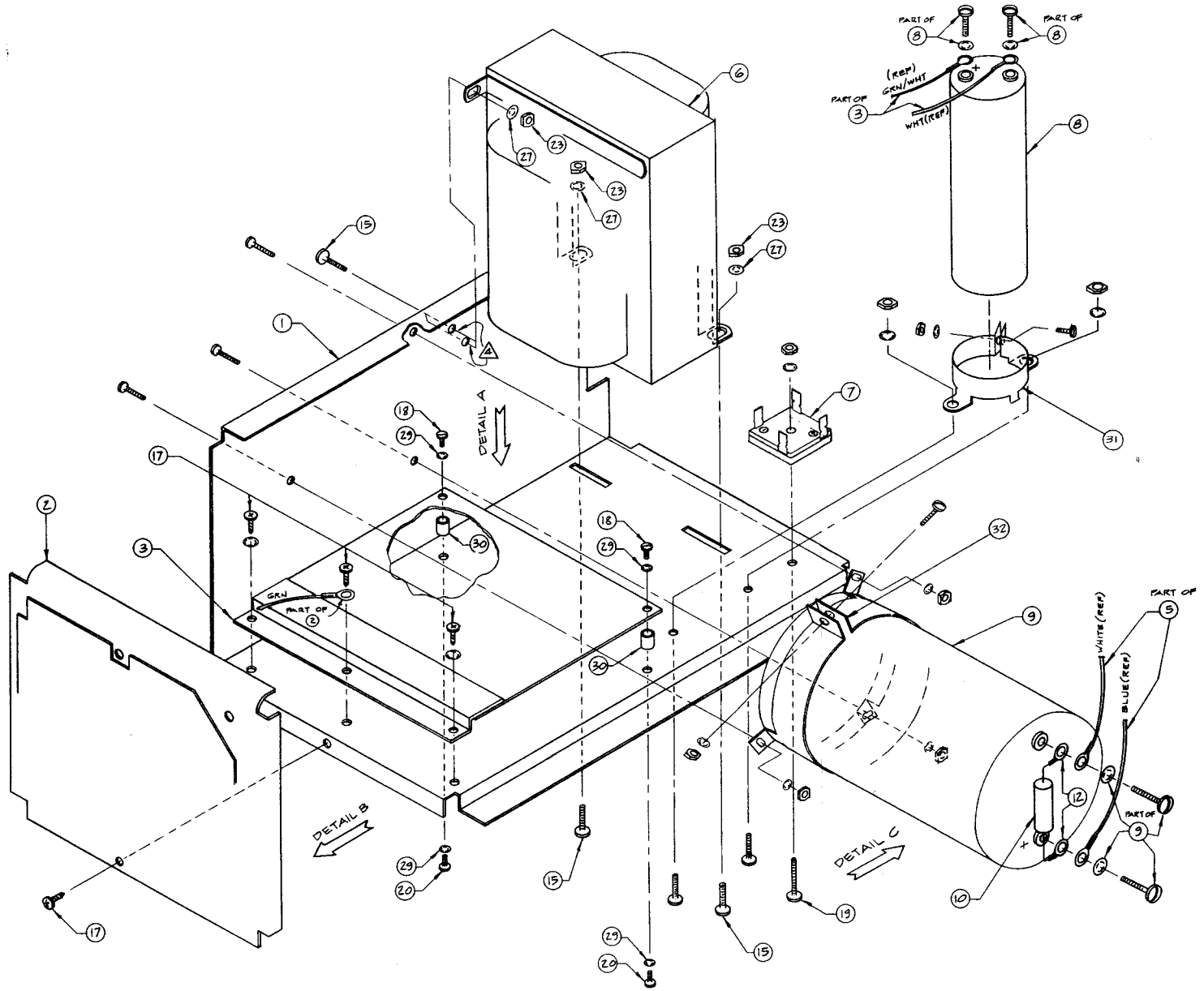
ASSY, PCB, SOL REGULATOR

NEXT ASSY. | USED ON

SIZE	SHT. 1 OF 1	SCALE:	DRAWING NO.	REV.
C		2/1	105008	D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-	E	ECN 10248, 10199, 10244 (REDRAWN)	1/11/78	

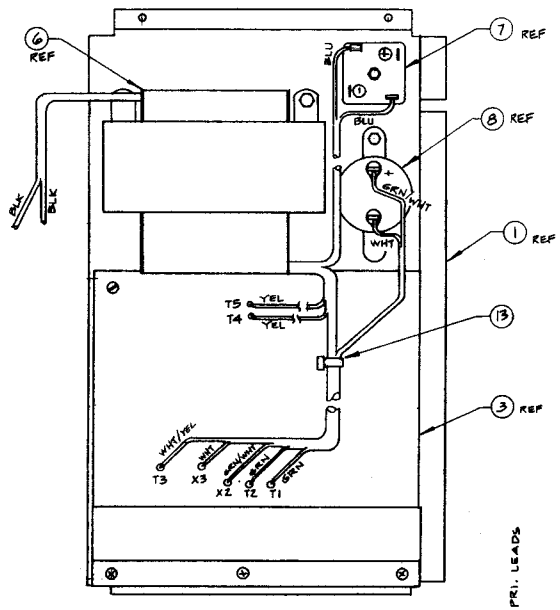
X-3



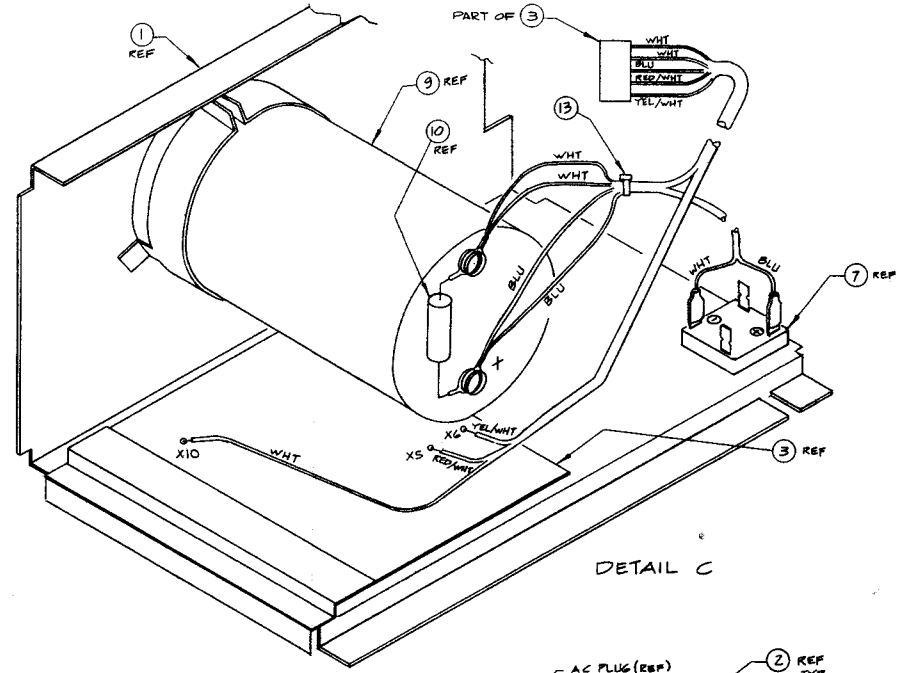
NOTES:
UNLESS OTHERWISE SPECIFIED;
1. ALL SCREWS ARE ITEM (16)
2. ALL NUTS ARE ITEM (24)
3. ALL LOCKWASHERS ARE ITEM (28)
4. ASSEMBLE THROUGH HOLE IN LINE WITH TRANSFORMER MOUNTING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES: TOLERANCES ARE: FRACTIONS ± — DECIMALS .XX ± — .XXX ± — ANGLES ± —	Processor Technology	DRAWN: LITO DATE: 11-8-77 CHECKED: AS DATE: 12-8-77	ENGR: DATE: 12/14/77 RELEASED: DATE:
101000-XX NEXT ASSY	101000-XX USED ON	SIZE D	SHT 1 OF 2	SCALE: NONE	DRAWING NO. 105001-XX	REV E

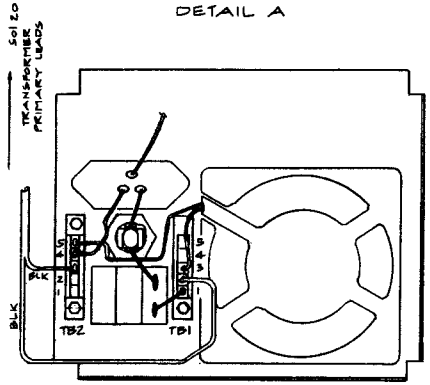
ASSY, POWER SUPPLY, SOL



DETAIL A

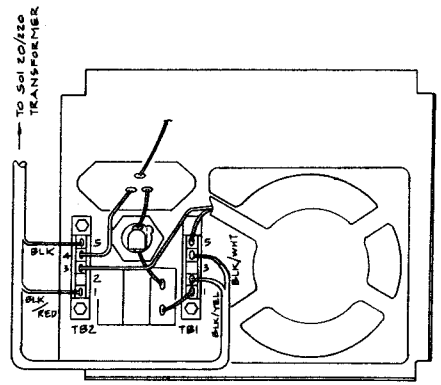


DETAIL C



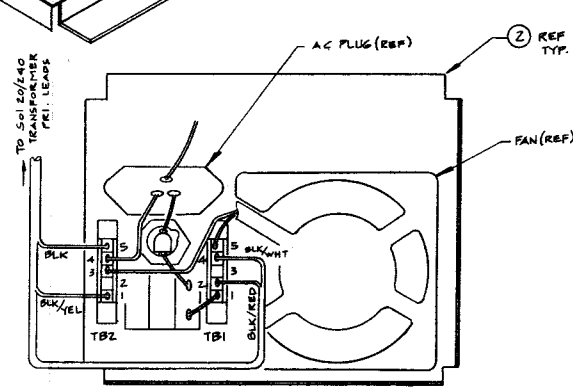
DETAIL B_1

WIRED FOR 115 VOLTS WITH SOL 20 TRANSFORMER (P/N 105028)



DETAIL B_2

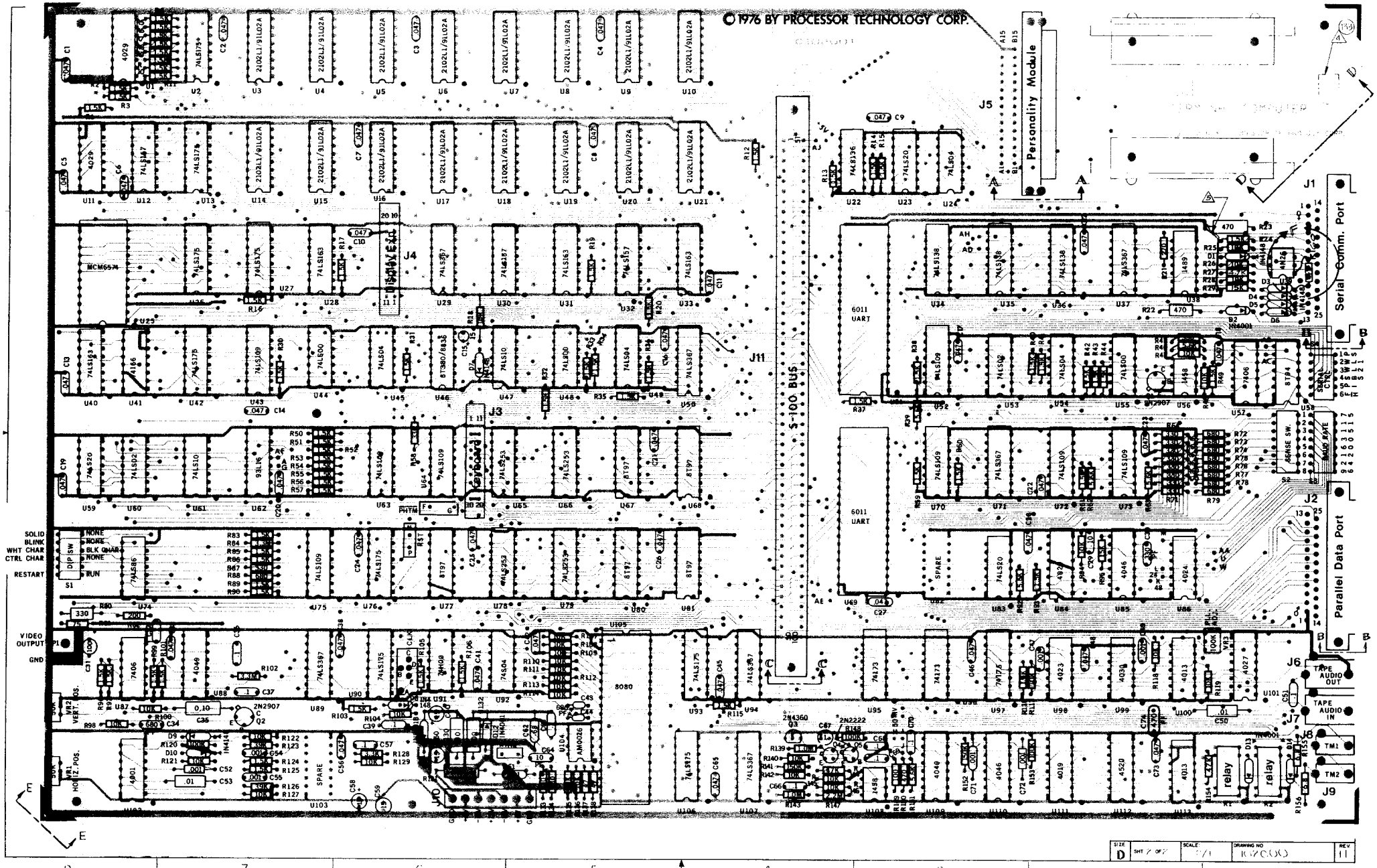
WIRED FOR 220 VOLTS WITH SOL 20/220 TRANSFORMER (P/N 105034)
REF. SCHEMATIC 105035



DETAIL B_3

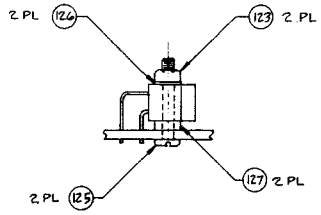
WIRED FOR 240 VOLTS WITH SOL 20/240 TRANSFORMER (P/N 105034)
REF. SCHEMATIC 105035

SIZE	SHT. 2 OF 2	SCALE:	DRAWING NO.	REV
D		NONE	105001-XX	E

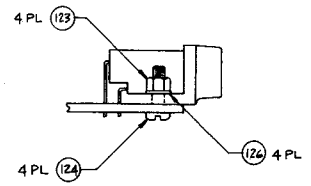

© 1976 BY PROCESSOR TECHNOLOGY CORP.
Personality Module
J5
J1
Serial Comm. Port
J2
Parallel Data Port
J3
J4
J11
S-100 BUS
6011 UART
SPARE
8080
MCM6571
J6
TAPE AUDIO OUT
J7
TAPE AUDIO IN
J8
J9
TM1
TM2
relay
VIDEO OUTPUT
GND
SOLID BLINK
WHT CHAR
CTRL CHAR
RESTART
RUN
HORIZ. POS.
VERT. POS.
SIZE
D
SCALE
DRAWING NO
REV
11

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
—	G	ECN 10124, 10131, 10136 REDRAWN	8-21-77	
—	H	ECN 10253	2-3-78	

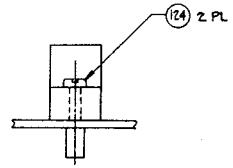
X-6



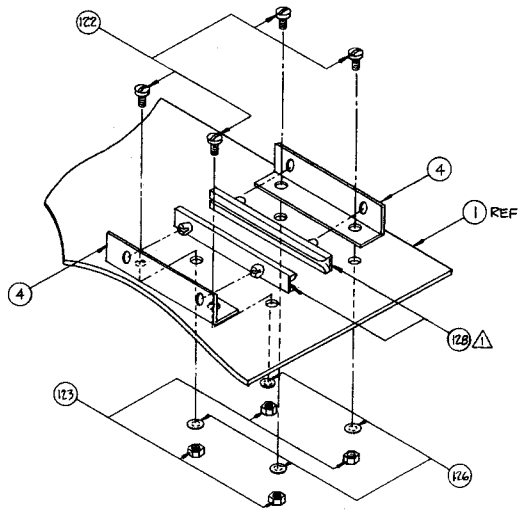
DETAIL A
MOUNTING OF J-5 ⚠2



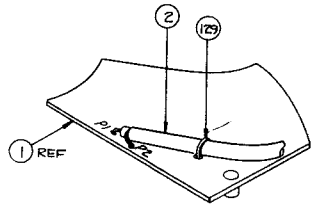
DETAIL B
MOUNTING OF J-1 AND J-2 ⚠2



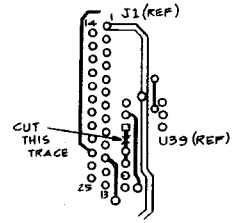
DETAIL C
MOUNTING OF BACKPLANE CONNECTOR (J-11) ⚠2



DETAIL D
PERSONALITY MODULE CARD GUIDE ASSY.



DETAIL E
MOUNTING OF VIDEO CABLE



DETAIL F
VIEWED FROM THE SOLDER SIDE

NOTES:

⚠1 INSERT CARD GUIDE WITH OPEN END AWAY FROM J-5 CONNECTOR.

⚠2 MOUNT CONNECTORS TO BOARD BEFORE SOLDERING.

3. R91 IS NOT USED.

⚠4 MARK WITH REVISION LETTER IN APPROXIMATE POSITION SHOWN.

⚠5 DISCONNECT LEFT LEAD OF R29 AND SOLDER JUMPER WIRE FROM LEFT LEAD OF R29 TO LEFT LEAD OF R23 AS SHOWN.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± —
DECIMALS .xx ± — .xxx ± —
ANGLES ± —

Processor Technology

DRAWN: AS 10-3-77
CHECKED: LITO 10-17-77
RELEASED: 10-21-77

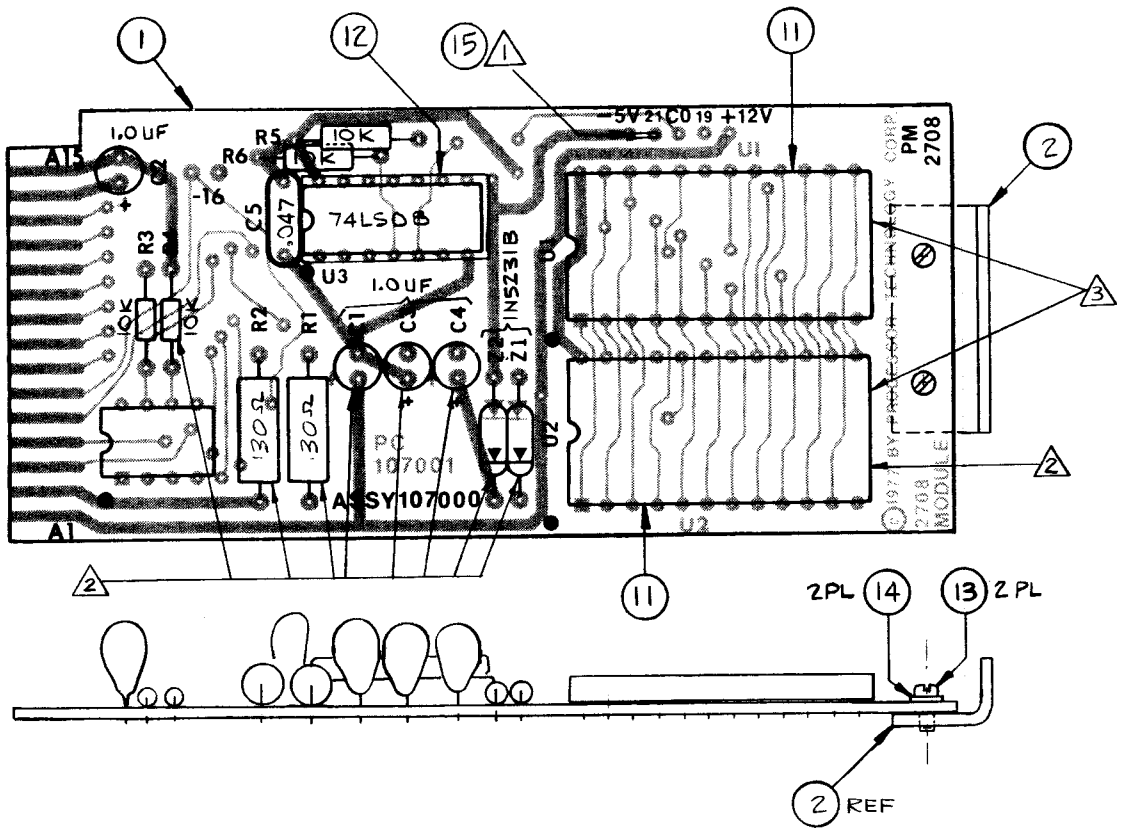
ASSEMBLY, PCB, Sol-PC

NEXT ASSY	USED ON
101000	101000

SIZE D | SHT 1 OF 2 | SCALE: NONE | DRAWING NO. 102000 | REV H

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
—	B	ECN 10124, 10148	11-29-77	[illegible]
—	C	ECN 10231	12-30-77	[illegible]

X-7



NOTES:

1. INSERT JUMPER WIRE, ITEM 15, BETWEEN "-5V" AND "21". CUT AND REMOVE TRACE ON THE SOLDER SIDE OF THE BOARD BETWEEN THE TWO PADS MARKED "CO" AND "21" ON THE 2708 VERSION ONLY
2. NOT USED ON 9216 VERSION.
3. EPROMS NOT SUPPLIED WITH 2708 VERSION.

REF. DES.	PART OR DWG. NO.	PART DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES:
TOLERANCES ARE:

FRACTIONS ± — DECIMALS .xx ± — .xxx ± — ANGLES ± —

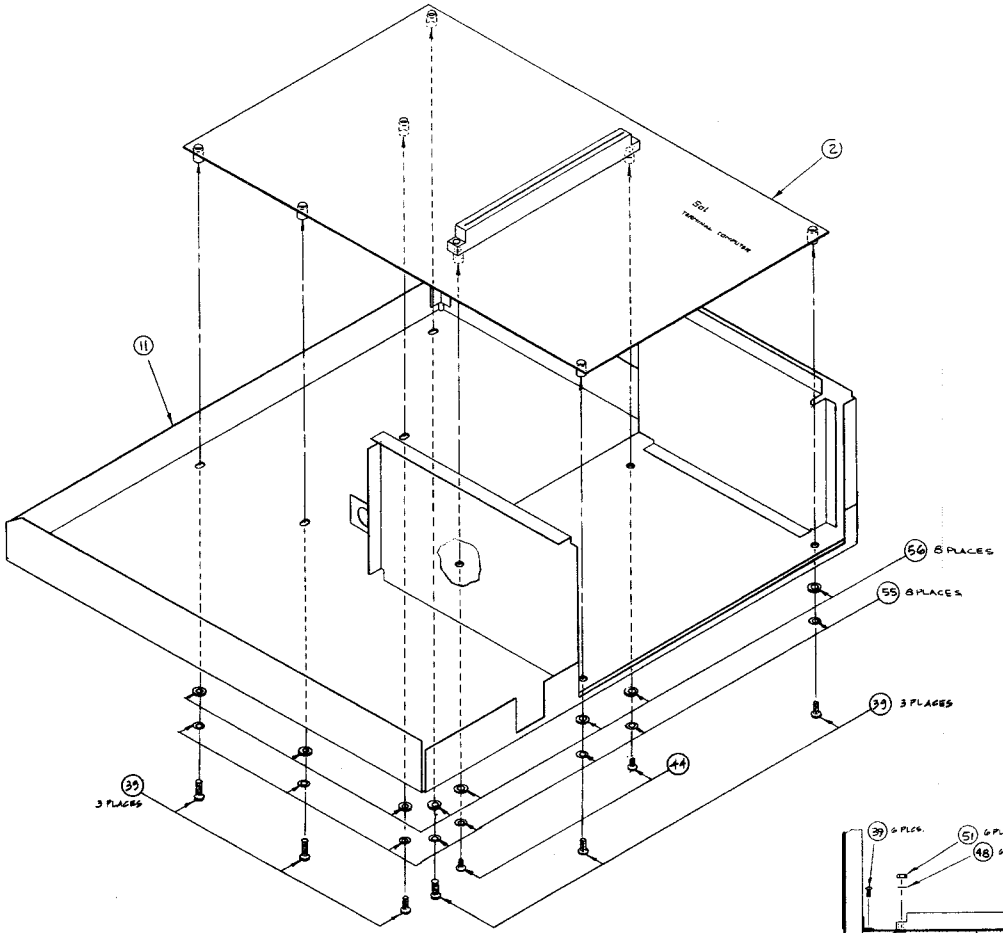
101000	101000
NEXT ASSY.	USED ON

ProcessorTechnology

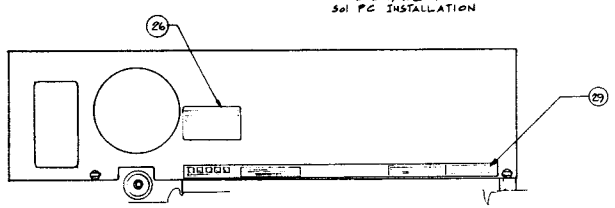
DRAWN:	A.S.	ENGR:	[illegible]
DATE:	11-20-77	DATE:	11-29-77
CHECKED:	LITO	RELEASED:	[illegible]
DATE:	11-28-77	DATE:	11-29-77

ASSY, PCB, PERSONALITY MODULE, 2708/9216

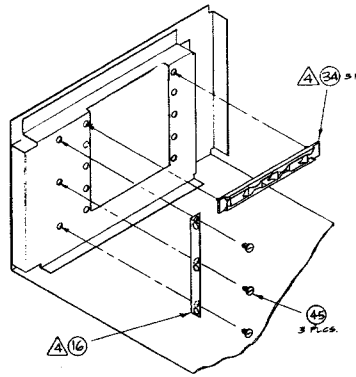
SIZE	SHT.	SCALE:	DRAWING NO.	REV.
B	1 OF 1	2/1	107000-01	C



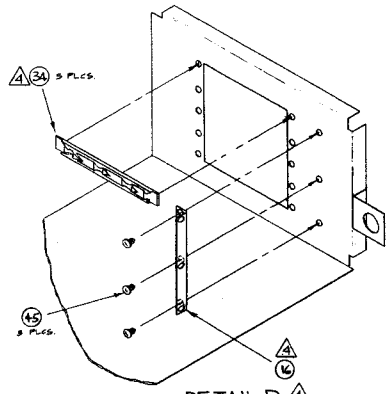
DETAIL F
SOL PC INSTALLATION



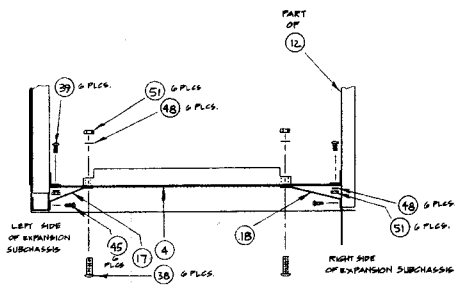
DETAIL A
REAR VIEW OF TOP COVER



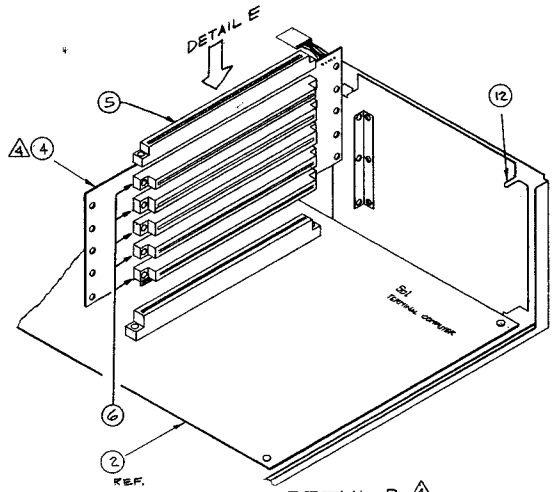
DETAIL C 4
LEFT SIDE EXPANSION SUBCHASSIS BRACKET AND CARD GUIDE MOUNTING



DETAIL D 4
RIGHT SIDE EXPANSION SUBCHASSIS BRACKET AND CARD GUIDE MOUNTING.



DETAIL E 3 4
MOUNTING OF BACKPLANE BOARD

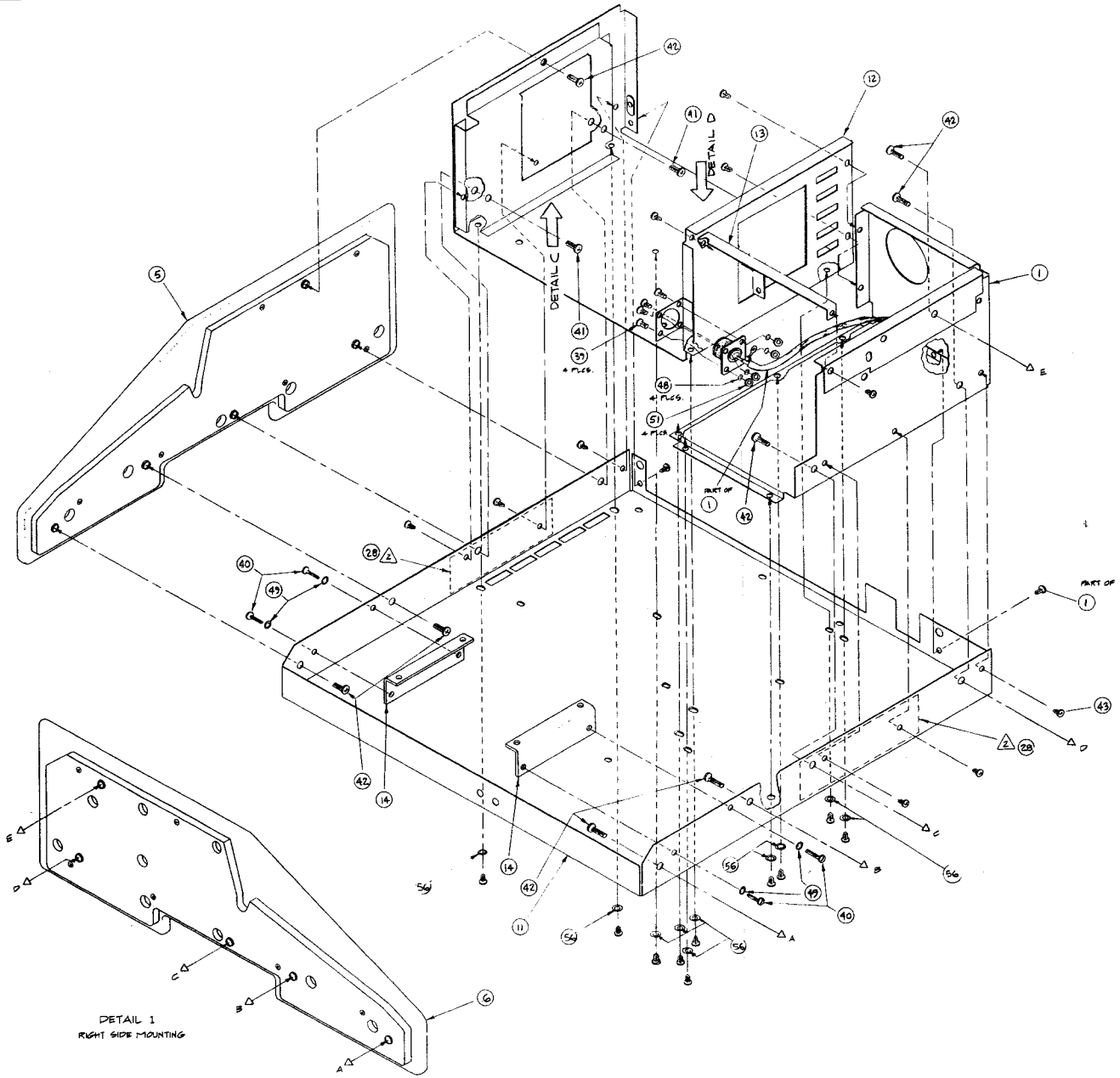


DETAIL B 4
BACKPLANE BOARD INSERTION INTO J11 OF SOL PC BOARD

NEXT ASSY.	USED ON	PART DESCRIPTION	
FINAL	—	Processor Technology Corporation, 6200 Hollis Street, Emeryville, CA 94608	DRAWN: LITO 1/5. DATE: 01-20-77
			CHECKED: L. Rubinstein DATE: 12 AUG 77
			DATE: 12 AUG 77

ASSY, TOP, SOL

D SIZE	101000(-XX)	SCALE: NONE	SHEET 3 OF 3



		PART DESCRIPTION	
NEXT ASSY.	USED ON	Processor Technology Corporation, 6200 Hollis Street, Emeryville, CA 94608	DRAWN: LITO / 13 DATE: 01-17-77
FINAL			CHECKED: L.E.S. VERIFIED DATE: 12 AUG. 77
			DRAWN: L. PALMER DATE: 12 AUG. 77
			APPROVED: J. TT DATE: 15 AUG. 77
		ASSY, TOP, SOI	
		D SIZE	101000 - XX SCALE: NONE SHEET 2 OF 3

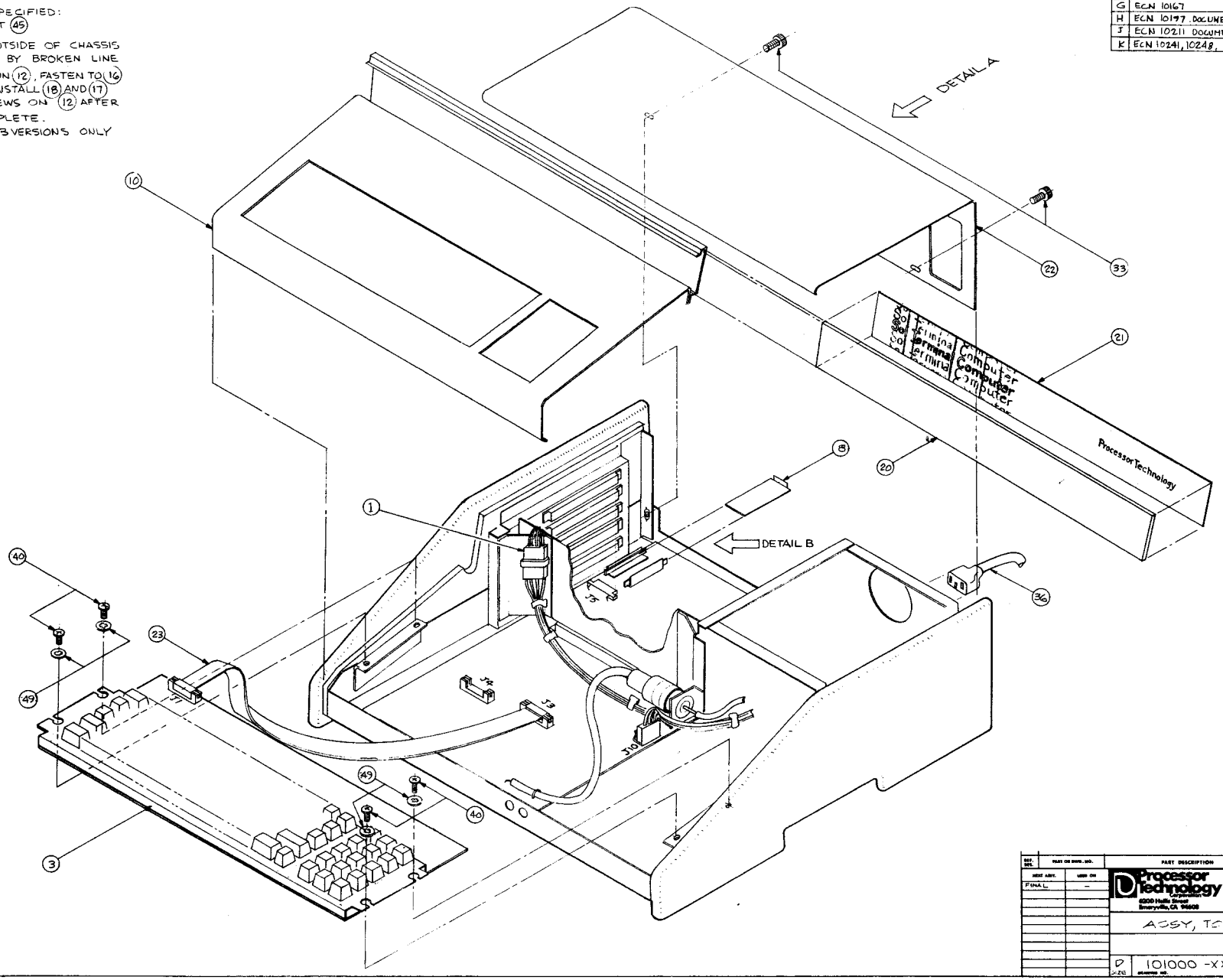
NOTES:

UNLESS OTHERWISE SPECIFIED:

1. ALL SCREWS ARE PART (45)
2. LABELS APPLIED TO OUTSIDE OF CHASSIS WITHIN AREA BOUNDED BY BROKEN LINE.
3. INSERT (14) INTO J11 ON (12), FASTEN TO (16) ON EACH SIDE, THEN INSTALL (18) AND (17) TIGHTEN MOUNTING SCREWS ON (12) AFTER INSTALLATION IS COMPLETE.
4. USED ON -02 AND -03 VERSIONS ONLY

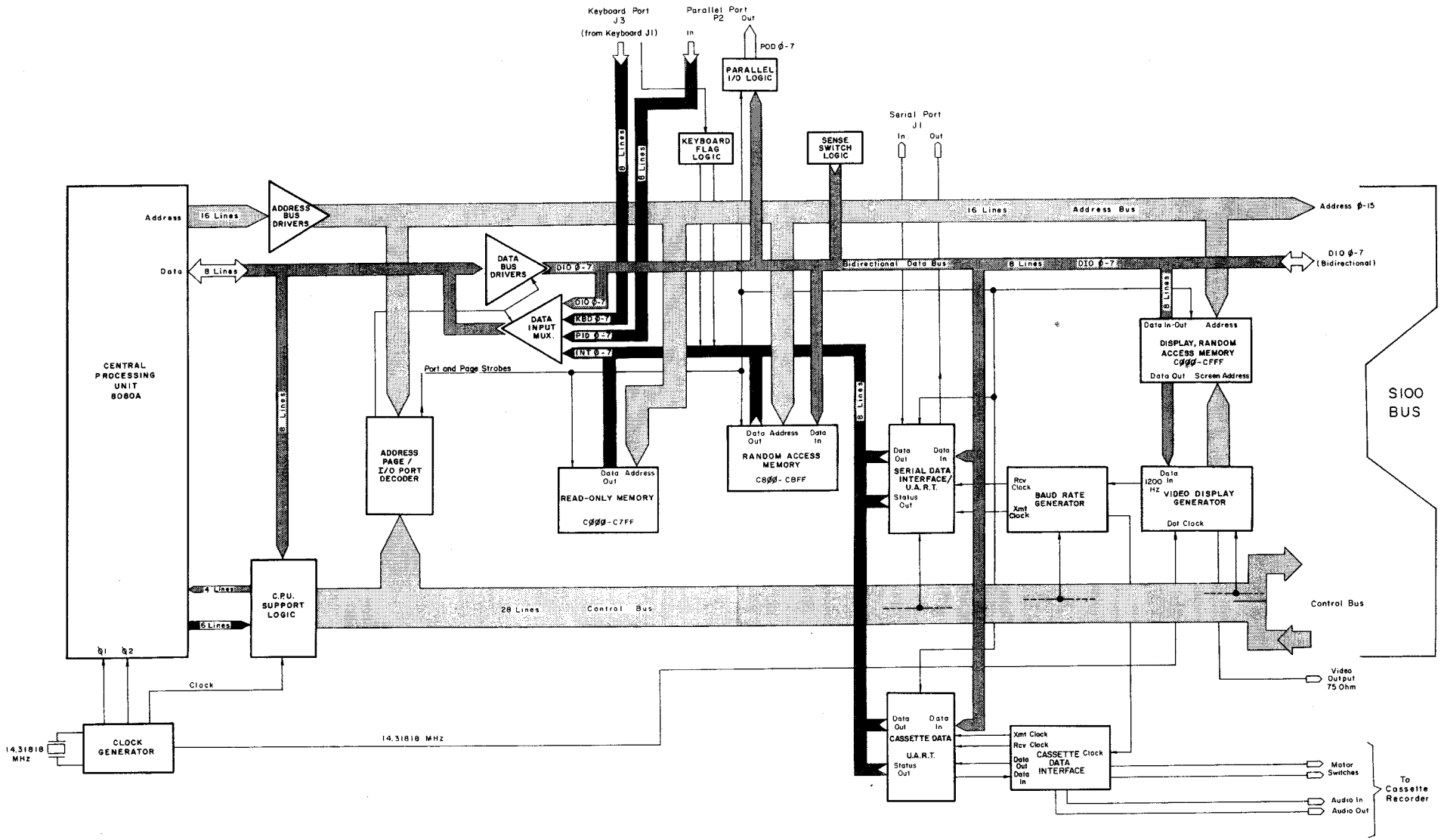
LTR	REVISION DESCRIPTION	DATE	APPR
F	ECN 10124 (DOCUMENTATION ONLY)	9-27-77	RM
G	ECN 10167	11-17-77	RM
H	ECN 10177 DOCUMENTATION ONLY	11-23-77	RM
J	ECN 10211 DOCUMENTATION ONLY	12-15-77	RM
K	ECN 10241, 10248,	1/11/78	RM

X-10



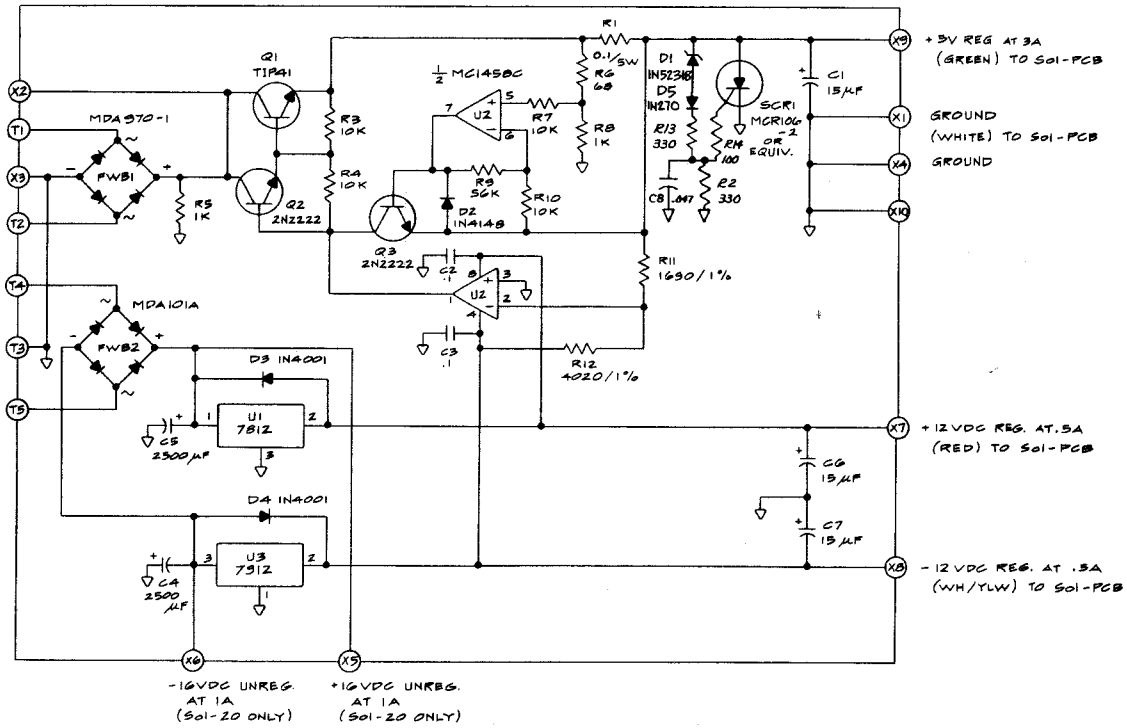
PART DESCRIPTION			
Processor Technology Corporation, 6200 Hollis Street, Emeryville, CA 94608	DRAWN: A.S. 7-7-77	ISSUED: L. FELLERS 12/19/77	
	CHECKED: L. FELLERS 12/19/77	RELEASED: 12 AUG 77	
ASSY, TCP, SOI			
SIZE: D	101000-XX	SCALE: NONE	SHEET 1 OF 3

Sol-P.C. BLOCK DIAGRAM-Rev. D,E



B	R13, R14, C8 ADDED PER ECO 10018	6-1-77	K.I.
C	ECN 10242	11/4/77	

X-12



REF. DES.	PART OR DWG. NO.	PART DESCRIPTION
NEXT ASSY.	USED ON	
105008	101000	

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

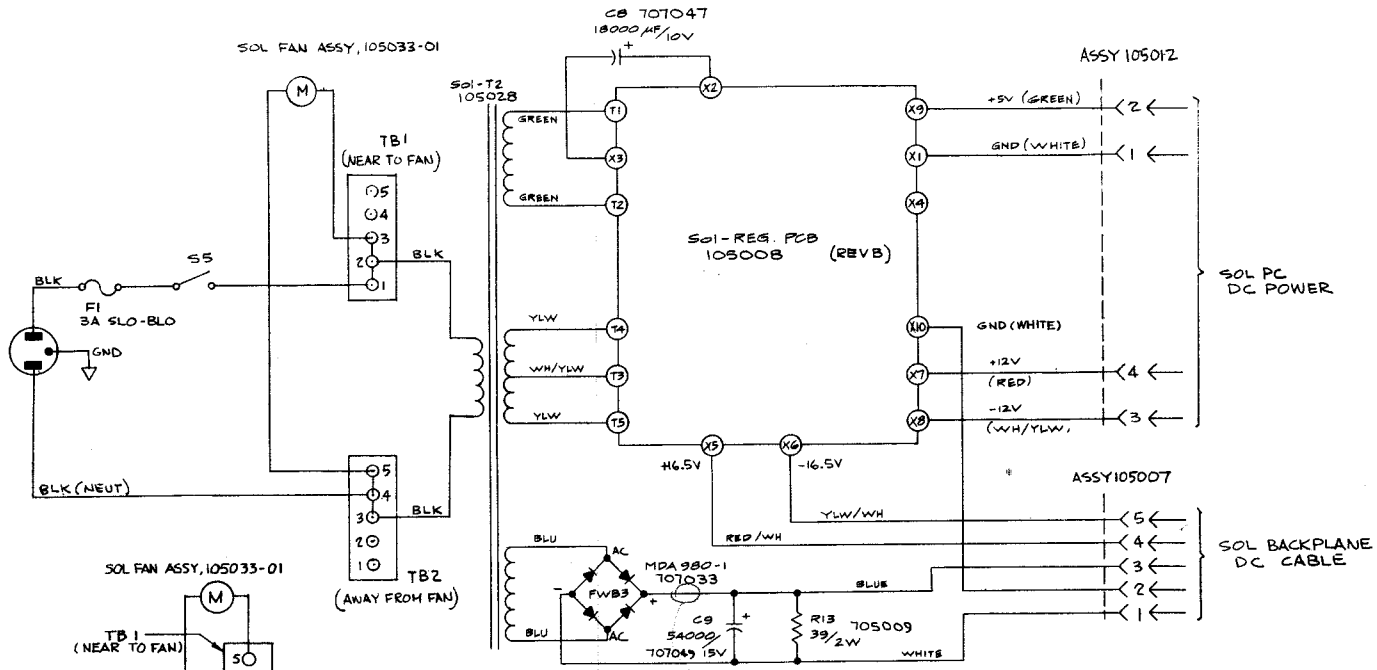
DRAWN: LITO		ENGR: L. FELSENSTEIN
DATE: 11-12-76		DATE: 6-1-77
CHECKED:		RELEASED: L. FELSENSTEIN
DATE: 6/1/77		DATE: 6-1-77

SCHEMATIC, SOI REGULATOR

SIZE	DRAWING NO.	SCALE: NONE	REV.
C	105009	SHEET 1 OF 1	C

LTR	REVISION DESCRIPTION	DATE	APPRVD
B	RELEASED AS REV B. (ECO 10003)	8-23-77	
C	ECN 10114	9/6/77	
D	ECN 10124 (DOCUMENTATION ONLY)	10-7 77	

X-13



PRMARY CIRCUIT FOR
Sol 20/220 & 20/240.

NOTES:

1. 220 VOLT OPTION HOOKUP: (AS SHOWN) TRANSFORMER BLK/YEL LEAD IS CONNECTED TO AC POWER AT TERMINAL POSITION #2 ON TB1 AS SHOWN. BLK/RED LEAD IS CONNECTED TO SPARE TERMINAL POSITION #1 ON TB2 (TERM BLOCK AWAY FROM FAN)

240 VOLT OPTION HOOKUP: TRANSFORMER BLK/RED LEAD IS CONNECTED TO AC POWER POS #2 ON TB1; BLK/YEL LEAD IS PLUGGED INTO SPARE TERMINAL POSITION #1 ON TB2 (TERM BLOCK AWAY FROM FAN)

REF. DES.	PART OR DWG. NO.	PART DESCRIPTION
NEXT ASSY.	USED ON	
103001-02	101000-02	

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

DRAWN: LITO 11-10-76
CHECKED: AS 21 AUG 77
ENGR: C. FELSENSTEIN 23 Aug 77
RELEASED: 23 AUG 77

SCHEMATIC, SOL POWER SUPPLY

C SIZE | DRAWING NO. 105002 | SCALE: NONE | SHEET 1 OF 1

LTR	REVISION DESCRIPTION	DATE	APPD
–	SEE HISTORY FILE FOR PREVIOUS REV.	–	–
G	ECN 10129, 10136, 10124		
H	ECN 10253	2-3-78	

X-14

NOTE: SEE DRAWING 5

C.P.U. SUPPORT LOGIC

CLOCK GENERATOR

C.P.U.

DATA BUS DRIVER

DATA INPUT MUX.

ADDRESS BUS DRIVERS

J11 SMEMR 47
J11 SINP 49
J11 SM1 44
J11 SOUT 43
J11 STAT DSB 18
J11 SHLTA 48
J11 SSTACK 98
J11 SWO 97
J11 SINTA 96
J11 DO DSB 28
J3 KBD RESTART 13
J11 PSYNC 76
J11 PINTE 28
J11 PHLDA 26
J11 PWR 77
J11 PWAIT 27
J11 PDBIN 78
J11 MWRITE 68
J11 FRDY 58
J11 C/C DSB 19
J11 PRDY 72
J11 XRDY 3
J11 CLOCK 49
J11 PRESET 75
(DWG. 2,3,4) PSYNC·Ø2
(DWG. 3,5) POC
J11 POC 39
J11 PHOLD 74
J11 PINT 78
(DWG. 4) 14.3 MHZ
(DWG. 2) MEM SEL (HEX ADDRESS 000-CBFF)

SI-1 RESTART
SYNC
INTE
HLDA
WR
WAIT
DBIN
READY
RESET
HOLD
INT
+5V
+12V
Ø1
Ø2
GND
-5V

D7 6 5 4 3 2 1 0
A15 36 35 34 33 32 31 30 29 27 26 25 A0

(DWG. 2,4) PAGE CC (DISPLAY)
(DWG. 2,3) PORT IN FC (KEYPORT PORT)
(DWG. 2,3) (PARALLEL PORT) PORT IN FD
(DWG. 2) INT SEL

MFX ADR A
MFX ADR B
OUT DSBC
FOC
DBIN

KBD 7 J3 18 → PID 7 J2 6 → INT 7 (DWG. 2,3,5)
KBD 6 J3 17 → PID 6 J2 7 → INT 6 (DWG. 2,3,5)
KBD 5 J3 16 → PID 5 J2 8 → INT 5 (DWG. 2,3,5)
KBD 4 J3 15 → PID 4 J2 5 → INT 4 (DWG. 2,3,5)
KBD 3 J3 8 → PID 3 J2 10 → INT 3 (DWG. 2,3,5)
KBD 2 J3 7 → PID 2 J2 11 → INT 2 (DWG. 2,3,5)
KBD 1 J3 6 → PID 1 J2 12 → INT 1 (DWG. 2,3,5)
KBD Ø J3 5 → PID Ø J2 13 → INT Ø (DWG. 2,3,5)
90/43 DID 7 J11
40/93 DID 6 J11
39/92 DID 5 J11
38/91 DID 4 J11
89/42 DID 3 J11
88/41 DID 2 J11
86/94 DID 1 J11
36/95 DID Ø J11

J11 ADR15 32
J11 ADR14 86
J11 ADR13 85
J11 ADR12 33
J11 ADR11 87
J11 ADR10 37
J11 ADR9 34
J11 ADR8 84
J11 ADR7 83
J11 ADR6 82
J11 ADR5 29
J11 ADR4 30
J11 ADR3 31
J11 ADR2 81
J11 ADR1 80
J11 ADR Ø 79

J11 +8V 1
J11 ADD DSB 23
J10 +5V 2
J10 +12V 4
J10 -12V 3
J10 GND 1
J11 PHANTOM 67
GROUND 50, 100
PROTECT 70
J11 Ø1 25
J11 Ø2 24
J11 DIG1 57

REF. DES.	PART OR DWG. NO.	PART DESCRIPTION
NEXT ASSY.	USED ON	
102000	501	

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

DRAWN: LITO — DATE: 3-23-76
CHECKED: — DATE:
ENGR: L. FRANKENSTEIN — DATE: 4-26-77
RELEASED: L. FRANKENSTEIN — DATE: 4-26-77

SCHEMATIC, PCB, 501 PC

CPU & BUS

H REV. — DRAWING NO. 102002 — SCALE: — — SHEET 1 OF 5 — D SIZE

LTR	REVISION DESCRIPTION	DATE	APPD
-	SEE SHT. 1	-	-

X-15

NOTE: SEE DRAWING 5

ADDRESS PAGE / I/O PORT DECODER

RANDOM ACCESS MEMORY

(DWG. 1,3,4) PSYNC · Ø2

J11 SINTA 36 — J11 Ø2 24 — J11 PHANTOM 67 — J11 ADR 15 32 — J11 ADR 14 86 — J11 ADR 13 85 — J11 ADR 12 33 — J11 SINP 46 — J11 ADR 11 87

ST34 U58 74LS04 — AE AC — AB AD

U24 74LS04 — 74LS136 U22 — R13 1.5K — R14 1.5K — R15 1.5K — +5V

74LS20 U23

74LS138 U34 MEM. DECODER — 74LS138 U35 I/O PORT DECODER — 74LS138 U36 I/O PORT DECODER

74LS02 U39 — 74LS04 U54 — 74LS109 U70 — R60 1.5K — 74LS367 U71 — 74LS02 U33 — 74LS20 U23

J11 PWR 77 — J11 SOUT 45

0 AH (ALARM)

U2A 74LS04 — J11 PDBIN 78

U24 74LS04 — 13 12

J11 ADR 10 37 — J11 ADR 9 34 — J11 ADR 8 84 — J11 MWRITE 68 — J11 ADR 7 83 — J11 ADR 6 82 — J11 ADR 5 29 — J11 ADR 4 30 — J11 ADR 3 31 — J11 ADR 2 81 — J11 ADR 1 80 — J11 ADR 0 79

9102A U3 RAM — 9102A U4 RAM — 9102A U5 RAM — 9102A U6 RAM — 9102A U7 RAM — 9102A U8 RAM — 9102A U9 RAM — 9102A U10 RAM

DI DO CE WE

J11 DIO 0 36/95 — J11 DIO 1 35/94 — J11 DIO 2 41/88 — J11 DIO 3 42/89 — J11 DIO 4 38/91 — J11 DIO 5 39/92 — J11 DIO 6 40/93 — J11 DIO 7 43/90

PAGE C4 — PAGE C0 — PAGE C8

J5 PERSONALITY MODULE CONNECTOR — ROM

A6 C4 — A5 C0 — B13 A9 — B12 A8 — B11 A7 — A7 A6 — A8 A5 — A12 A4 — A11 A3 — A10 A2 — A9 A1 — A13 A0

A1 +12V — A2 −12V — A,B14 +5V — A,B15 — J5

A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

INT 0 (DWG. 1,3,5) — INT 1 — INT 2 — INT 3 — INT 4 — INT 5 — INT 6 — INT 7 (DWG. 1,3,5)

PAGE 02 DISPLAY SECT. MEMORY (DWG. 4)

MEM SEL (DWG. 1) (000 - C8FF)

PORT OUT FE DISPLAY SECTION (DWG. 4)
PORT OUT FD PARALLEL (DWG. 3)
PORT OUT FB TAPE (DWG. 5)
PORT OUT FA AUX CTRL (DWG. 3,5)
PORT OUT F9 UART (DWG. 3)
PORT OUT F8 CTRL (DWG. 3)

INT SEL (DWG. 1)

PORT IN FF SENSE SWITCH
PORT IN FE DISPLAY SECTION (DWG. 4)
PORT IN FD PARALLEL (DWG. 1)
PORT IN FC KEYBOARD (DWG. 1)
PORT IN FB TAPE (DWG. 5)
PORT IN FA AUX STATUS (DWG. 5)
PORT IN F9 UART (DWG. 3)
PORT IN F8 STATUS (DWG. 3)

J11 PRDY 72

SCHEMATIC, PCB, SOL PC

MEMORY & DECODER

H REV.	DRAWING NO. 102002	SCALE: —	SHEET 2 OF 5	D SIZE

LTR	REVISION DESCRIPTION	DATE	APPD
-	SEE SHT. 1	-	-

X-16

SERIAL DATA INTERFACE/ UART

SENSE SWITCH LOGIC

BAUD RATE GENERATOR

PARALLEL I/O LOGIC

KEY-BOARD LOGIC

J1 (CLEAR TO SEND-EIA) SCTS
J1 (CARRIER DETECT-EIA) SCD
J1 (DATA SET READY-EIA) SDSR
(DWG.2) PORT OUT F8
(DWG.2) PORT OUT FA
(DWG.2) PORT IN F8
(DWG.2) PORT IN F9
(DWG.1,5) POC
J1 (SERIAL LOOP CURRENT SOURCE) SLCS
J1 (RECEIVED DATA - EIA) SRD
J1 (SERIAL LOOP RECEIVE 1) SLR1
J1 (SERIAL LOOP RECEIVE 2) SLR2
J9 (KEYBOARD BREAK) BRK
POC
(DWG.2) PORT OUT F8
J11 DIO 7 90/43
J11 DIO 6 40/88
J11 DIO 5 39/85
J11 DIO 4 38/91
(DWG.2) PORT OUT FD
J11 DIO 3 89/42
J11 DIO 2 88/41
J11 DIO 1 33/84
J11 DIO 0 34/93
(DWG.2) PORT IN FF
J2 (PARALLEL DATA. RDY) PDR
J2 (PARALLEL EXT. DEV. RDY) PXDR
(DWG. 3) 2400 HZ
(DWG. 3) 4800 HZ
(DWG. 3) 1200 HZ (A)
(DWG.3) 9600 HZ
(DWG.3) 38400 HZ
(DWG.3) 19200 HZ
(DWG.4) PLL 1200 HZ (REF)
(DWG.2) PORT IN FD
J11 Ø2
(DWG.2) PORT IN FC
J9 KEYBOARD DATA READY
(DWG.2) PORT IN FA
(DWG.1,2,4) PSYNC · Ø2

TAPE CTRL LATCH (PORT FA)
PIE LATCH
HALF DUPLEX/LOCAL DATA
PARITY INHIBIT
STOP BIT SELECT
WORD LENGHT 2
WORD LENGHT 1
PARITY SELECT
BAUD RATE SW
153.6 KHZ
PARALLEL INPUT PORT STATUS
PARALLEL OUTPUT PORT STROBE
KEYBOARD STATUS
FULL/HALF DUPLEX S4-6
IN FD
IN FC

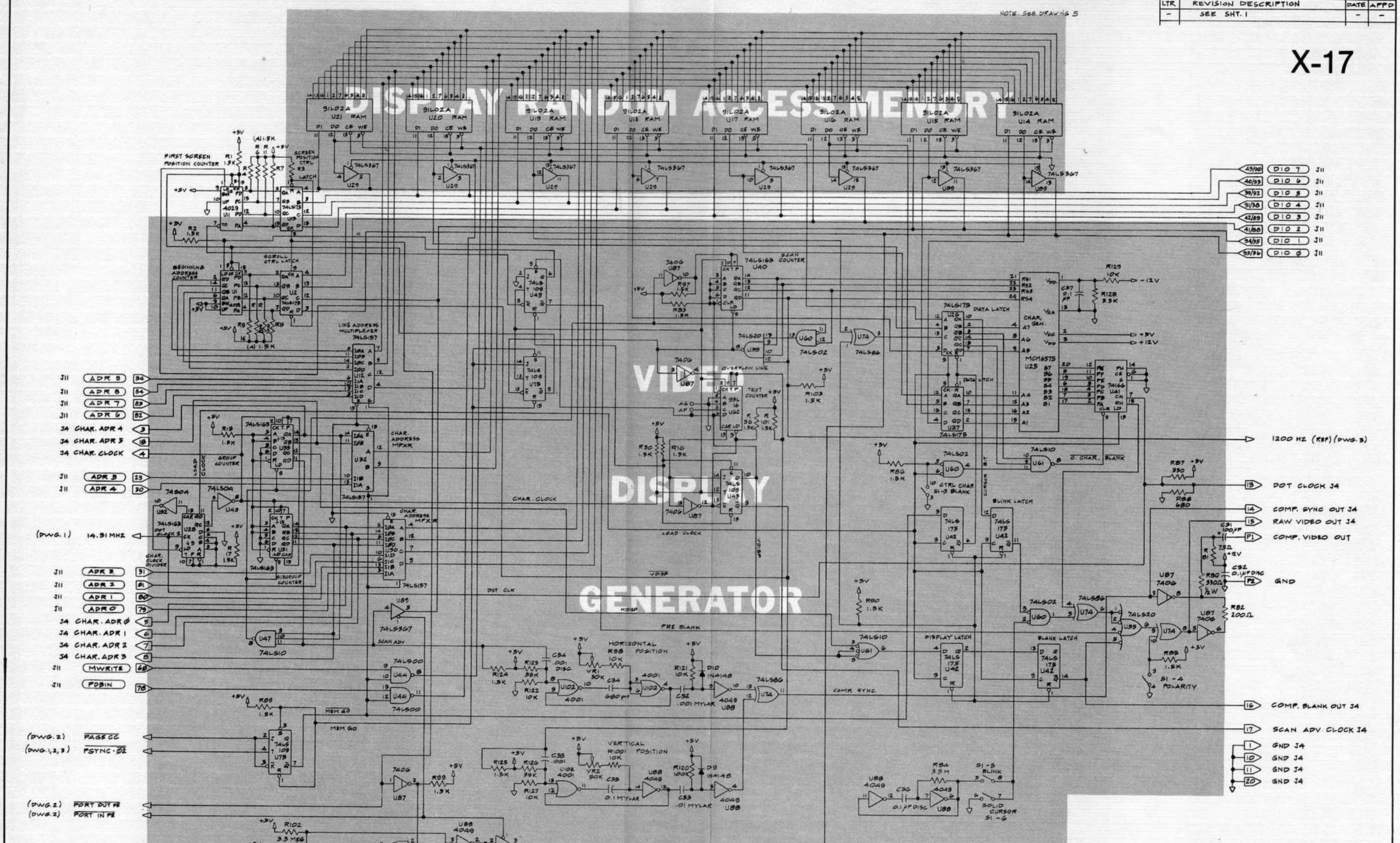
J3 PIE (PARALLEL INPUT ENABLE) J2
TAPE HI SPEED (DWG.9)
TAPE CONTROL 1 (DWG.5)
TAPE CONTROL 2 (DWG.5)
TAPE HI SPEED (DWG.5)
J4 PUS (PARALLEL UNIT SELECT) J2
J1 SCLO (SERIAL CURRENT LOOP OUT) J1
INT 7 (DWG.1,2,5)
INT 6 (DWG.1,2,5)
INT 5 (DWG.1,2,5)
INT 4 (DWG.1,2,5)
INT 3 (DWG.1,2,5)
INT 2 (DWG.1,2,5)
INT 1 (DWG.1,2,5)
INT Ø (DWG.1,3,5)
J4 KBD LOC J8
J1 STD (TRANSMITTED DATA-EIA) J1
J1 SDTR (DATA TERMINAL READY-EIA) J1
J1 SRTS (REQUEST TO SEND-EIA) J1
J1 GND J1
J1 GND J1
J2 POD 7 J2
J2 POD 6 J2
J2 POD 5 J2
J2 POD 4 J2
J2 GND J2
J2 GND J2
J2 POB (PARALLEL OUTPUT END) J2
J2 POD 3 J2
J2 POD 2 J2
J2 POD 1 J2
J2 POD Ø J2
J2 PIAK (PARALLEL INPUT ACK) J2
J2 POL (PARALLEL OUTPUT LOAD) J2

NOTE: SEE DRAWING 5

SCHEMATIC, PCB, 501 PC
INPUT / OUTPUT
H REV. 102002 DRAWING NO. SCALE: — SHEET 3 OF 5 D SIZE

LTR	REVISION DESCRIPTION	DATE	APPD
–	SEE SHT. 1	–	–

X-17



SCHEMATIC, PCB, SOL PC

DISPLAY SECTION

REV.	DRAWING NO.	SCALE	SHEET	SIZE
H	102002	—	4 OF 5	D

LTR	REVISION DESCRIPTION	DATE	APPD
-	SEE SHT. 1	-	-

X-18

NOTES:

1. * DO NOT SUBSTITUTE
2. ADR Ø — S-100 BUS SIGNAL NAME
3. 100 — S-100 BUS PINS
4. 100 — S-100 BUS PINS
5. 25 — I/O CONNECTORS, POWER SUPPLY, PERSONALITY MODULE
6. 25 — I/O CONNECTORS, POWER SUPPLY, PERSONALITY MODULE
7. ON CARD CONNECTION
8. ON CARD CONNECTION
9. CAPACITORS IN MICROFARADS UNLESS NOTED OTHERWISE.
10. ALL RESISTORS 1/4 W UNLESS MARKED OTHERWISE, RESISTANCE IN OHMS.

J7 AUDIO IN

Q3 2N4360 · Q5 2N2222 · Q4 2N2222 · +5VDC · R139 1M AGC DET · C67 1µF · R148 100K · R143 1M · AGC AMP · C50 MYLAR 0.01 · R141 150K · R142 10K · R140 10K · C66 0.1 DISC · C68 0.1 DISC · C69 .01 · -12VDC · R146 10K · R145 10K · R147 2.2M · HYSTERESIS COMPARATOR · +12VDC · R144 47K · R118 10K · C49 .001 DISC · C74 470PF DISC · DIFF DATA · RECOVERED NRZ DATA · 1X CLK · RECOVER CLK (1X) · RECOVER CLOCK (16X) · BYTE WRITE CLOCK (16X) · C72 .001 MYLAR · FLL ADJ. · VR3 100K · R154 47K · R153 100K · C71 .001 DISC · R152 150K · 1200 HZ · OUTPUT CLOCK · C47 .001 DISC · R117 10K · R119 10K · C51 DISC 0.1 · R151 5.6K · R150 470 · R149 100 · C70 0.1 DISC · (500 MV) · 0 H (50 MV) · AUDIO OUT J6

(DWG.2) PORT IN FA — J11 DIO Ø 34/93 · DIO 1 35/94 · DIO 2 36/95 · DIO 3 37/96 · DIO 4 38/97 · DIO 5 39/98 · DIO 6 40/99 · DIO 7 90/43

(DWG.2) PORT IN FB

(DWG.1,3) POC

(DWG.3) 9,600 HZ — AA

(DWG.3) 4,800 HZ — U V

(DWG.3) 19,200 HZ — S T

(DWG.3) 38,400 HZ — Q R

(DWG.3) TAPE HI SPEED

(DWG.3) TAPE HI SPEED

(DWG.3) 1,200 HZ (A) — Y Z

(DWG.3) 2,400 HZ — W X

J8 TAPE MOTOR 1 · +5V · R139 4.82 ½W · K1 · D13 IN4001 · K2 · D14 IN4001

J9 TAPE MOTOR 2 · R136 4.82 ½W

(DWG.3) TAPE CONTROL 1

(DWG.3) TAPE CONTROL 2

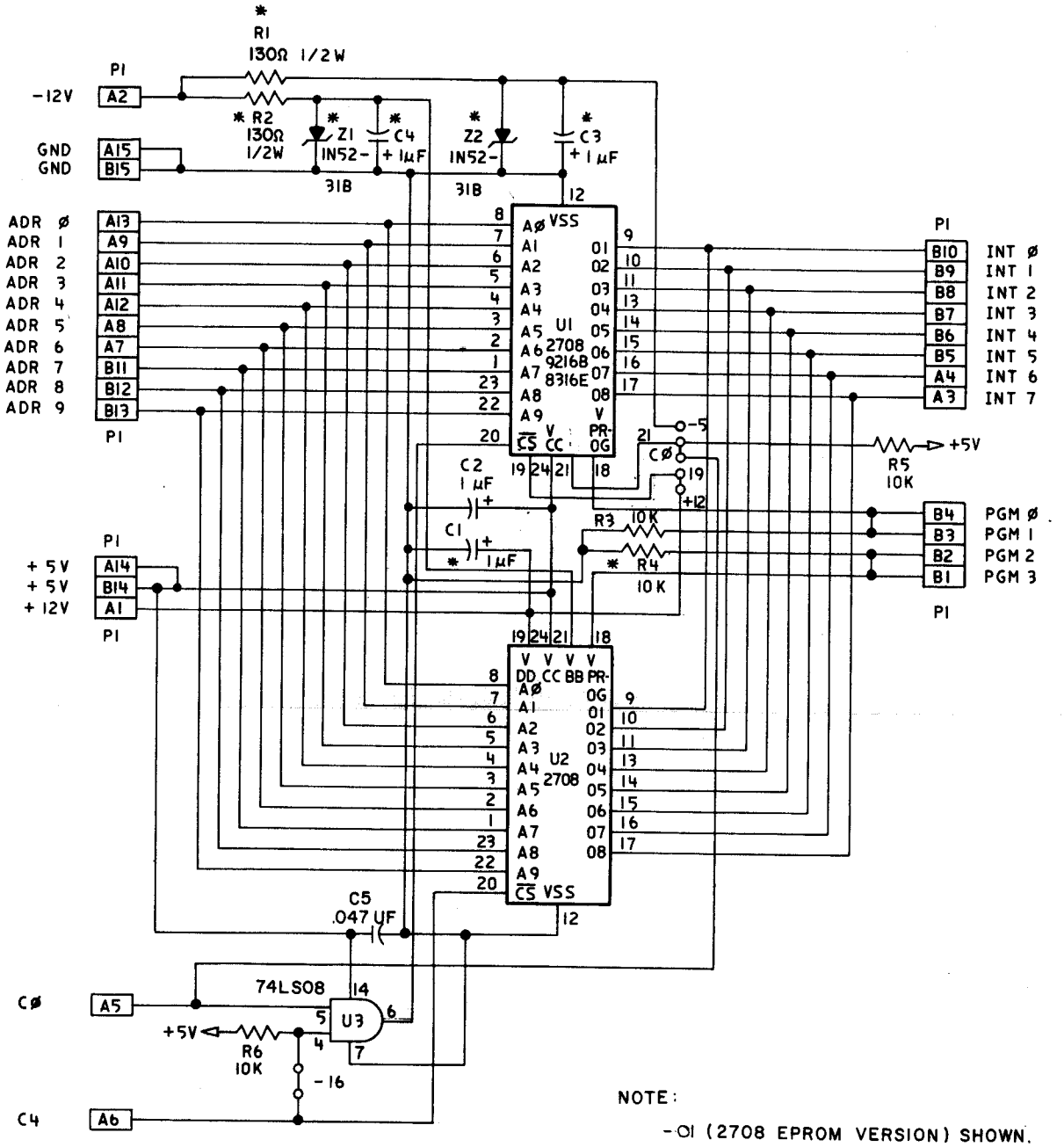
U69 UART TMS6011 — RI TI1 TI2 TI3 TI4 TI5 TI6 TI7 TI8 RDD DRR MR SBS PI PS WLS1 WLS2 CRL RC TC VSS VBB VDD RO1 RO2 RO3 RO4 RO5 RO6 RO7 RO8 DR TBMT OR FE TBRL TO

INT 0 (DWG. 1,2,3) · INT 1 · INT 2 · INT 3 · INT 4 · INT 5 · INT 6 · INT 7 (DWG. 1,2,3)

PORT OUT FB (DWG.2)

U109 4049 · U108 4049 · U112 4520 · U111 4019 · U110 4046 · U100 4013 · U101 4027 · U98 4023 · U99 4030 · U113 4013

SCHEMATIC, PCB, SOL PC			
AUDIO TAPE I/O			
H REV.	102002 DRAWING NO.	SCALE: — SHEET 5 OF 5	D SIZE



NOTE:

-01 (2708 EPROM VERSION) SHOWN.

* = PART WHICH IS MISSING FROM 9216 MASKED ROM VERSION

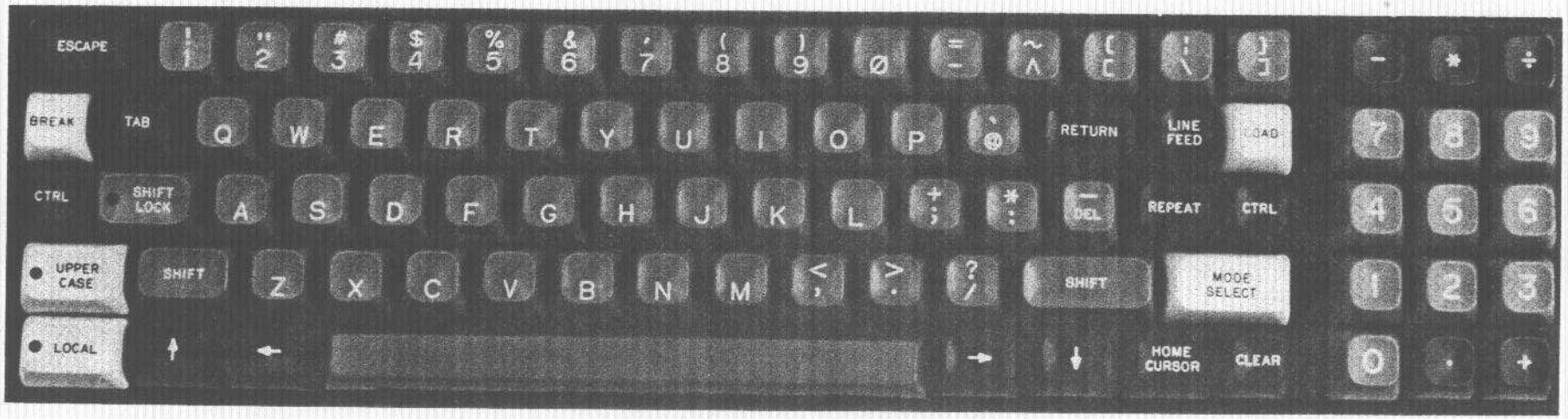
REF. DES.	PART OR DWG. NO.	PART DESCRIPTION
NEXT ASSY.	USED ON	
107000	501	

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

DRAWN: LITO		ENGR: L. FELSENSTEIN	
DATE: 10-20-76		DATE: 6-30-77	
CHECKED:		RELEASED: K Tobash	
DATE:		DATE: 6-30-77	

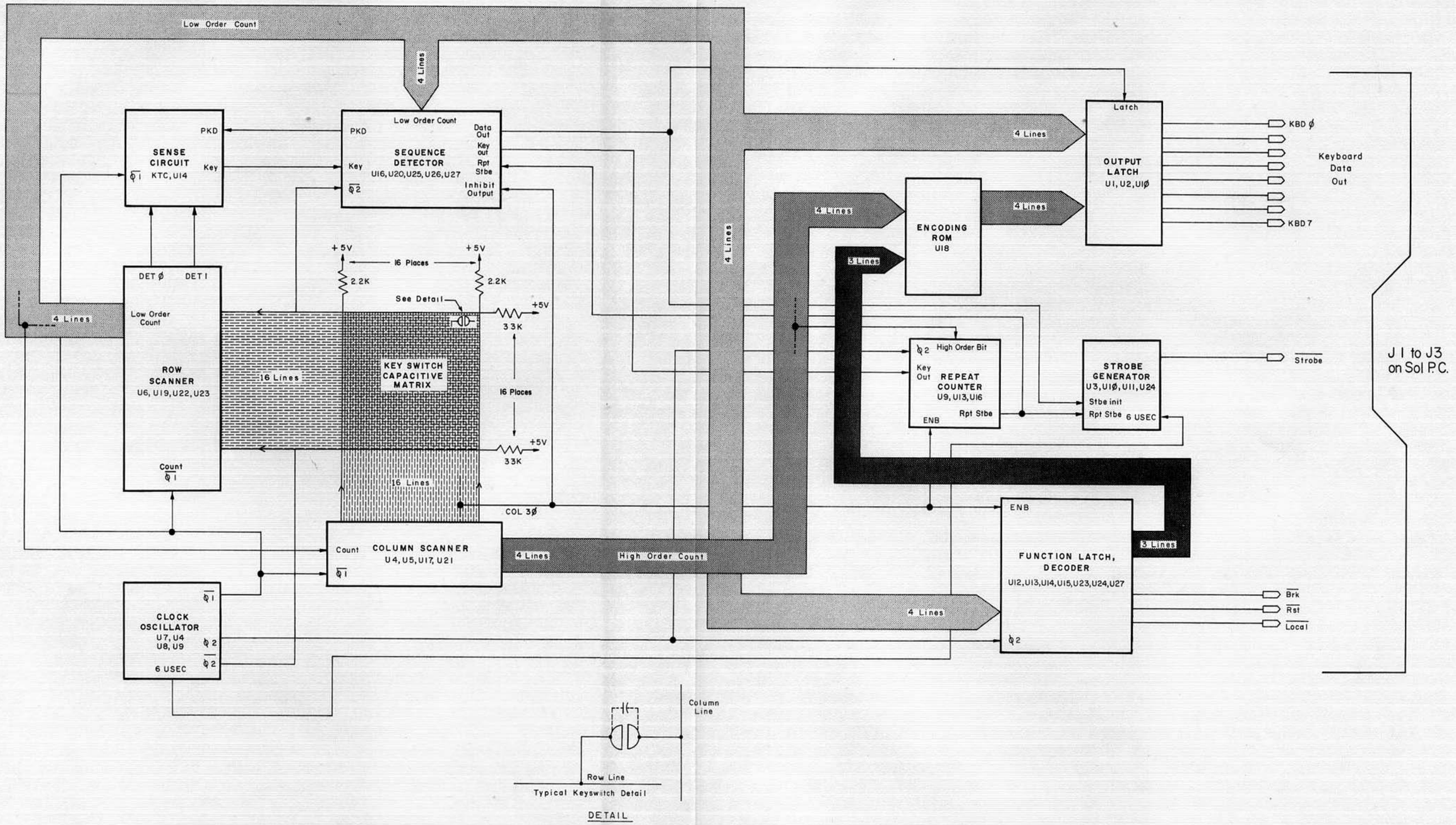
SCHEMATIC, PERSONALITY MODULE 2708/9216

B	107002	SCALE: NONE	B
REV.	DRAWING NO.	SHEET 1 OF 1	SIZE


ESCAPE
BREAK
TAB
CTRL
SHIFT LOCK
UPPER CASE
SHIFT
LOCAL
RETURN
LINE FEED
REPEAT
CTRL
DEL
SHIFT
MODE SELECT
HOME CURSOR
CLEAR

Sol - KEYBOARD BLOCK DIAGRAM - Rev. B, C

X-21



LTR	REVISION DESCRIPTION	DATE	APPVD
B	PINS 1 AND 4 OF U11 TIED TO +5V: WERE FLOATING. KEYS 13-16 UNCHANGED	5-18-77	J.T.
C			K.K.
D			

X-22

U5 7493 BIN A B C D

U17 7442

U21 7442

U6 7493

U4 74LS00

U7 74LS132

U10 74LS00

74LS74 U8

R8 1.5K

R7 1K

C7 .0047 μF

1.5K(3) R13 R14 R15

U19 4051

U22 4051

33K (16 PLS)

2.2K (15 PLS)

R34

K.T.C. DET. 5

IN1 IN2 OUT PKD

SEE DETAIL A

U14 74LS00

U25 74LS30

U26 74LS74

U20 2101

R33 1.5K

R26 680

U18 8T74 OR 74187A

U2 74LS175

U1 74LS175

U11 74LS74

U10 74LS00

U16 74LS00

U27 74LS10

U3 555

R4 68K

R5 560K

C4 .01

C3 0.1μF MYLAR ±10%

R32 68K

C14 15 μF

C2,5,6, C12,13 .047 (5 PLS.)

C1 15 μF DIPPED TANT

U9 74LS74

R25 1.5K

U24 7406

U23 74LS04

U13 74LS10

U12 8334 OR 9334 OR 83L34

R28 1.5K

R3 150

LED1 MV5752

U15 74LS74

"UPPER CASE" R2 150

LED 2 MV5752

"LOCAL" R1 150

LED 3 MV5752

R29 1.5K

R30 1.5K

R31 1.5K

J1

5	BIT 0
6	BIT 1
7	BIT 2
8	BIT 3
15	BIT 4
16	BIT 5
17	BIT 6
18	BIT 7
3	STROBE
2, 9, 12, 19	+5V
1, 10, 11 20	GROUND
4	BRK
13	RST
14	LOCAL

IN1 R16 1K; IN2 R23 1K

Q8 2N3640; Q9 2N4274; Q7 2N3640; Q4 2N3640; Q2 2N4274; Q6 2N3640; Q5 2N3640; Q3 2N3640; Q1 2N4274

C9 220PF; C10 220PF; C11 .01; C8 470PF

R18 1K; R19 10; R12 2K; R20 1K; R11 3K; R22 3K; R10 3K; R17 390; R21 1K; R9 3K; R24 1K

CR4 IN5221B

DETAIL A
CAPACITIVE SWITCH DETECTOR CIRCUIT

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4W ±5%

REF DES	PART OR DWG. NO.	PART DESCRIPTION
NEXT ASSY.	USED ON	
104000	SOL	

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

DRAWN: LITO DATE: 11-8-76
CHECKED: DATE: 3/18/77
ENGR: L. FELSENSTEIN DATE: 21 MARCH 77
RELEASED: L. FELSENSTEIN DATE: 21 MARCH 77

SCHEMATIC, KEYBOARD, SOL

C REV. 104002 DRAWING NO. SCALE: NONE SHEET 1 OF 1 D SIZE

84330 PRINTED ON NO. 1000H-10 CLEARPRINT

APPENDICES

I Statement of Warranty

II 8080 Operating Codes

III Standard Color Code

IV Loading DIP Devices, Soldering Tips and Installing Augat Pins

V IC Pin Configurations

VI TV Interface

VII Memory and I/O Allocation Chart

Processor Technology

Warranty

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by **Processor Technology Corporation** are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled modules, following the date of purchase. The defective part must be returned postpaid to **Processor Technology Corporation** within the warranty period.

Any malfunctioning module, purchased as a kit directly from **Processor Technology** and returned to the factory within the three-month warranty period, which in the judgement of **PTC** has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, without charge. Kits purchased from authorized **PTC** dealers should be returned to the selling dealer for the same warranty service.

Any modules purchased as a kit and returned to **PTC,** which in the judgement of **PTC** are not covered by the above conditions, will be repaired and returned at a cost commensurate with the work required. In any case, this charge will not exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least one year following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to **PTCO** postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

00	NOP		28	---		50	MOV	D,B	78	MOV	A,B	A0	ANA	B	C8	RZ		F0	RP				
01	LXI	B,D16	29	DAD	H	51	MOV	D,C	79	MOV	A,C	A1	ANA	C	C9	RET		F1	POP	PSW			
02	STAX	B	2A	LHLD	Adr	52	MOV	D,D	7A	MOV	A,D	A2	ANA	D	CA	JZ		F2	JP	Adr			
03	INX	B	2B	DCX	H	53	MOV	D,E	7B	MOV	A,E	A3	ANA	E	CB	---		F3	DI				
04	INR	B	2C	INR	L	54	MOV	D,H	7C	MOV	A,H	A4	ANA	H	CC	CZ	Adr	F4	CP	Adr			
05	DCR	B	2D	DCR	L	55	MOV	D,L	7D	MOV	A,L	A5	ANA	L	CD	CALL	Adr	F5	PUSH	PSW			
06	MVI	B,D8	2E	MVI	L,D8	56	MOV	D,M	7E	MOV	A,M	A6	ANA	M	CE	ACI	D8	F6	ORI	D8			
07	RLC		2F	CMA		57	MOV	D,A	7F	MOV	A,A	A7	ANA	A	CF	RST	1	F7	RST	6			
08	---		30	---		58	MOV	E,B	80	ADD	B	A8	XRA	B	D0	RNC		F8	RM				
09	DAD	B	31	LXI	SP,D16	59	MOV	E,C	81	ADD	C	A9	XRA	C	D1	POP	D	F9	SPHL				
0A	LDAX	B	32	STA	Adr	5A	MOV	E,D	82	ADD	D	AA	XRA	D	D2	JNC	Adr	FA	JM	Adr			
0B	DCX	B	33	INX	SP	5B	MOV	E,E	83	ADD	E	AB	XRA	E	D3	OUT	D8	FB	EI				
0C	INR	C	34	INR	M	5C	MOV	E,H	84	ADD	H	AC	XRA	H	D4	CNC	Adr	FC	CM	Adr			
0D	DCR	C	35	DCR	M	5D	MOV	E,L	85	ADD	L	AD	XRA	L	D5	PUSH	D	FD	---				
0E	MVI	C,D8	36	MVI	M,D8	5E	MOV	E,M	86	ADD	M	AE	XRA	M	D6	SUI	D8	FE	CPI	D8			
0F	RRC		37	STC		5F	MOV	E,A	87	ADD	A	AF	XRA	A	D7	RST	2	FF	RST	7			
10	---		38	---		60	MOV	H,B	88	ADC	B	B0	ORA	B	D8	RC							
11	LXI	D,D16	39	DAD	SP	61	MOV	H,C	89	ADC	C	B1	ORA	C	D9	---							
12	STAX	D	3A	LDA	Adr	62	MOV	H,D	8A	ADC	D	B2	ORA	D	DA	JC	Adr						
13	INX	D	3B	DCX	SP	63	MOV	H,E	8B	ADC	E	B3	ORA	E	DB	IN	D8						
14	INR	D	3C	INR	A	64	MOV	H,H	8C	ADC	H	B4	ORA	H	DC	CC	Adr						
15	DCR	D	3D	DCR	A	65	MOV	H,L	8D	ADC	L	B5	ORA	L	DD	---							
16	MVI	D,D8	3E	MVI	A,D8	66	MOV	H,M	8E	ADC	M	B6	ORA	M	DE	SBI	D8	**HEX-ASCII TABLE**					
17	RAL		3F	CMC		67	MOV	H,A	8F	ADC	A	B7	ORA	A	DF	RST	3						
18	---		40	MOV	B,B	68	MOV	L,B	90	SUB	B	B8	CMP	B	E0	RPO		Non-Printing					
19	DAD	D	41	MOV	B,C	69	MOV	L,C	91	SUB	C	B9	CMP	C	E1	POP	H						
1A	LDAX	D	42	MOV	B,D	6A	MOV	L,D	92	SUB	D	BA	CMP	D	E2	JPO	Adr	00	NULL				
1B	DCX	D	43	MOV	B,E	6B	MOV	L,E	93	SUB	E	BB	CMP	E	E3	XTHL		07	BELL				
1C	INR	E	44	MOV	B,H	6C	MOV	L,H	94	SUB	H	BC	CMP	H	E4	CPO	Adr	09	TAB				
1D	DCR	E	45	MOV	B,L	6D	MOV	L,L	95	SUB	L	BD	CMP	L	E5	PUSH	H	0A	LF				
1E	MVI	E,D8	46	MOV	B,M	6E	MOV	L,M	96	SUB	M	BE	CMP	M	E6	ANI	D8	0B	VT				
1F	RAR		47	MOV	B,A	6F	MOV	L,A	97	SUB	A	BF	CMP	A	E7	RST	4	0C	FORM				
20	---		48	MOV	C,B	70	MOV	M,B	98	SBB	B	C0	RNZ		E8	RPE		0D	CR				
21	LXI	H,D16	49	MOV	C,C	71	MOV	M,C	99	SBB	C	C1	POP	B	E9	PCHL		11	X-ON				
22	SHLD	Adr	4A	MOV	C,D	72	MOV	M,D	9A	SBB	D	C2	JNZ	Adr	EA	JPE	Adr	12	TAPE				
23	INX	H	4B	MOV	C,E	73	MOV	M,E	9B	SBB	E	C3	JMP	Adr	EB	XCHG		13	X-OFF				
24	INR	H	4C	MOV	C,H	74	MOV	M,H	9C	SBB	H	C4	CNZ	Adr	EC	CPE	Adr	14					
25	DCR	H	4D	MOV	C,L	75	MOV	M,L	9D	SBB	L	C5	PUSH	B	ED	---		1B	ESC				
26	MVI	H,D8	4E	MOV	C,M	76	HLT		9E	SBB	M	C6	ADI	D8	EE	XRI	D8	7D	ALT MODE				
27	DAA		4F	MOV	C,A	77	MOV	M,A	9F	SBB	A	C7	RST	0	EF	RST	5	7F	RUB OUT				

HEX-ASCII TABLE

Printing		Characters	
30	0	40	@
31	1	20	space
32	2	21	!
33	3	22	"
34	4	23	#
35	5	24	$
36	6	25	%
37	7	26	&
38	8	27	'
39	9	28	(
		29	)
41	A	2A	*
42	B	2B	+
43	C	2C	,
44	D	2D	-
45	E	2E	.
46	F	2F	/
47	G	3A	:
48	H	3B	;
49	I	3C	<
4A	J	3D	=
4B	K	3E	>
4C	L	3F	?
4D	M	5B	[
4E	N	5C	\
4F	O	5D	]
50	P	5E	↑ (^)
51	Q	5F	← (_)
52	R		
53	S		
54	T		
55	U		
56	V		
57	W		
58	X		
59	Y		
5A	Z		

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

Processor Technology Corp.

APPENDIX II

JUMP

C3	JMP	Adr
C2	JNZ	Adr
CA	JZ	Adr
D2	JNC	Adr
DA	JC	Adr
E2	JPO	Adr
EA	JPE	Adr
F2	JP	Adr
FA	JM	Adr
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	Adr
CC	CZ	Adr
D4	CNC	Adr
DC	CC	Adr
E4	CPO	Adr
EC	CPE	Adr
F4	CP	Adr
FC	CM	Adr

RETURN

C9	RET	
C0	RNZ	
C8	RZ	
D0	RNC	
D8	RC	
E0	RPO	
E8	RPE	
F0	RP	
F8	RM	

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC	
0F	RRC	
17	RAL	
1F	RAR	

CONTROL

00	NOP	
76	HLT	
F3	DI	
FB	EI	

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L

77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

CONSTANT DEFINITION

0BDH, 1AH	Hex
105D, 105	Decimal
72O, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A', 'B'	ASCII

OPERATORS

MOVE IMMEDIATE

06	MVI	B, D8
0E	MVI	C, D8
16	MVI	D, D8
1E	MVI	E, D8
26	MVI	H, D8
2E	MVI	L, D8
36	MVI	M, D8
3E	MVI	A, D8

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	D8
D6	SUI	D8
DE	SBI	D8
E6	ANI	D8
EE	XRI	D8
F6	ORI	D8
FE	CPI	D8

LOAD IMMEDIATE

01	LXI	B, D16
11	LXI	D, D16
21	LXI	H, D16
31	LXI	SP, D16

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC†	
3F	CMC†	

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

MOVE

40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[ ]
DW	D16	[ ]

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

* = all Flags (C,Z,S,P) affected

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

STANDARD COLOR CODE FOR RESISTORS AND CAPACITORS

COLOR	SIGNIFICANT FIGURE	DECIMAL MULTIPLIER	TOLERANCE (%)	VOLTAGE RATING*
Black	0	1		--
Brown	1	10		100
Red	2	100		200
Orange	3	1,000		300
Yellow	4	10,000		400
Green	5	100,000		500
Blue	6	1,000,000		600
Violet	7	10,000,000		700
Gray	8	100,000,000		800
White	9	1,000,000,000		900
Gold	-	0.1	5	1000
Silver	-	0.01	10	2000
No Color	-	---	20	500

*Applies to capacitors only.

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alighment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45° angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

(1) Use a low-wattage iron--25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder

melts the rest of the joint will be hot enough for the solder to "take", (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

INSTALLING AUGAT PINS

Augat pins are normally supplied on carriers (e.g., 8-pin and 16-pin carriers). In many cases the PC board layout permits Augat pins to be installed while still attached to the carrier or a portion of the carrier. In other cases the pins must be installed singly.

To install two or more pins that are still attached to the carrier, proceed as follows:

NOTE

It is perfectly alright to appropriately cut a carrier to accommodate the installation. For example, an 8-pin carrier can be cut in half (4 pins each) across the short dimension to fit a 4-pin, 4-corner layout. It may also be cut in half along the long dimension to fit a 4-pin, inline layout.

(1) Insert pins in the mounting holes from the front (component) side of board. (The carrier will hold the pins perpendicular to the board.)

(2) Solder all pins from back (solder) side of board so the solder "wicks up" to the front side.

(3) Check for solder bridges.

(4) Remove carrier.

To install single pins, proceed as follows:

(1) Hold board between two objects so that it stands on edge.

(2) Insert pins in the mounting holes from front (component) side of board.

(3) Solder pins from back (solder) side of board so the solder "wicks up" to the front side. (This will hold the pins firmly in place.)

(4) Insert a component lead into one pin and reheat the solder. Using the component lead, adjust pin until it is perpendicular to board. Allow solder to cool while holding the pin as steady as possible. Remove component lead. Repeat this procedure with other pins.

NOTE

If cooled solder is mottled or crystallized, a "cold joint" is indicated, and the solder should be reheated.

(5) Check each installation for cold joints and solder bridges.

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Television Interface

Anyone with a bunch of memory circuits, control logic and a wire wrap gun can whip up a digital video generator with TTL output levels. The problem as I see it is to get that digital video signal into a form that the TV set can digest. The care and feeding of digital inputs to the TV set is the subject of Don Lancaster's contribution to BYTE 2 – an excerpt from his forthcoming book, *TV Typewriter Cookbook*, to be published by Howard W. Sams, Indianapolis, Indiana.

... CARL

by
Don Lancaster
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We can get between a TV typewriter and a television style display system either by an rf modulator or a direct video method.

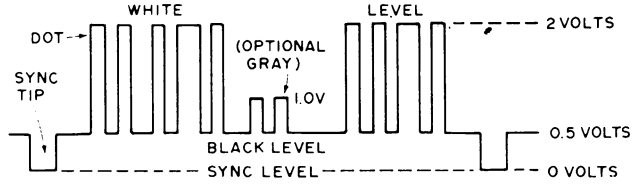
In the rf modulator method, we build a miniature, low power, direct wired TV transmitter that clips onto the antenna terminals of the TV set. This has the big advantage of letting you use any old TV set and ending up with an essentially free display that can be used just about anywhere. No set modifications are needed, and you have the additional advantage of automatic safety isolation and freedom from hot chassis shock problems.

There are two major restrictions to the rf modulator method. The first of these is that transmitters of this type must meet certain exactly spelled out FCC regulations and that system type approval is required. The second limitation is one of bandwidth. The best you can possibly hope for is 3.5 MHz for black and white and only 3 MHz for color, and many economy sets will provide far less. Thus, long character line lengths, sharp characters, and premium (lots of dots) character generators simply aren't compatible with clip-on rf entry.

In the direct video method, we enter the TV set immediately following its video detector but before sync is picked off. A few premium TV sets and all monitors already have a video input directly available, but these are still expensive and rare. Thus, you usually have to modify your TV set, either adding a video input and a selector switch or else dedicating the set to exclusive TV typewriter use. Direct video eliminates the bandwidth restrictions provided by the tuner, i-f strip, and video detector filter. Response can be further extended by removing or shorting the 4.5 MHz sound trap and by other modifications to provide us with longer line lengths and premium characters. No FCC approval is needed, and several sets or monitors are easily driven at once without complicated distribution problems.

There are two limitations to the direct video technique. One is that the set has to be modified to provide direct video entry. A second, and far more severe, restriction, is that many television sets are "hot chassis" or ac-dc sets with one side of their chassis connected to the power line. **These sets introduce a severe shock hazard and cannot be used as TV typewriter video entry displays unless some isolation technique is used with them.** If the TV set has a power transformer, there is usually no hot chassis problem. Transistor television sets and IC sets using no vacuum tubes tend to have power transformers, as do older premium tube type sets. All others (around half the sets around today) do not.

Fig. 1. Standard video interface levels. (Source impedance = 72 or 100 Ohms.)



Direct Video Methods

With either interface approach, we usually start by getting the dot matrix data, blanking, cursor, and sync signals together into one composite video signal whose

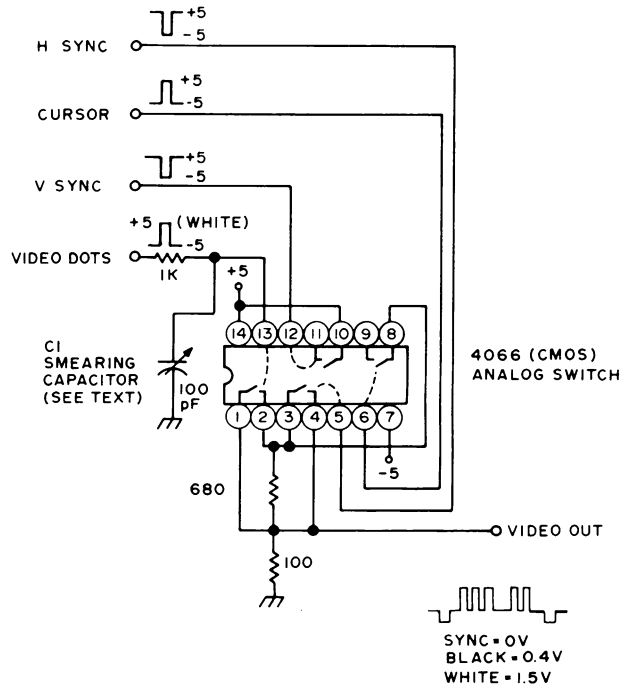
form is useful to monitors and TV sets. A good set of standards is shown in Fig. 1. The signal is dc coupled and always positive going. Sync tips are grounded and blacker than black. The normal open circuit black level is positive by one-half a volt, and the white level is two volts positive. In most TV camera systems, intermediate levels between the half volt black level and the two volt white level will be some shade of gray, proportionately brighter with increasing positive voltage. With most TV typewriter systems, only the three states of zero volts (sync), half a volt (black), and two volts (white dot) would be used. One possible exception would be an additional one volt dot level for a dim but still visible portion of a message or a single word.

The usual video source impedance is either 72 or 100 Ohms. Regardless of how far we travel with a composite video output, some sort of shielding is absolutely essential.

For short runs from board to board or inside equipment, tightly twisted conductors should be OK, as should properly guarded PC runs. Fully shielded cables should be used for interconnections between the TVT and the monitor or TV set, along with other long runs. As long as the total cable capacitance is less than 500 pF or so (this is around 18 feet of RG178-U miniature coax), the receiving end of the cable need not be terminated in a 72 or 100 Ohm resistor. When terminated cable systems are in use for long line runs or multiple outputs, they should be arranged to deliver the signal levels of Fig. 1 at their output under termination. Generally, terminated cable systems should be avoided as they need extra in the way of drivers and supply power.

The exact width of the horizontal and vertical sync pulses isn't usually too important, so long as the shape and risetime of these pulses are independent of position control settings and power supply variations. One exception to this is when you're using a color receiver and a color display. Here, the horizontal sync pulse should be held closely to 5.1 microseconds, so the receiver's color burst sampling does in fact intercept a valid color burst. More on this later.

Fig. 2. Analog switch combiner generates composite video.



Intentional Smear

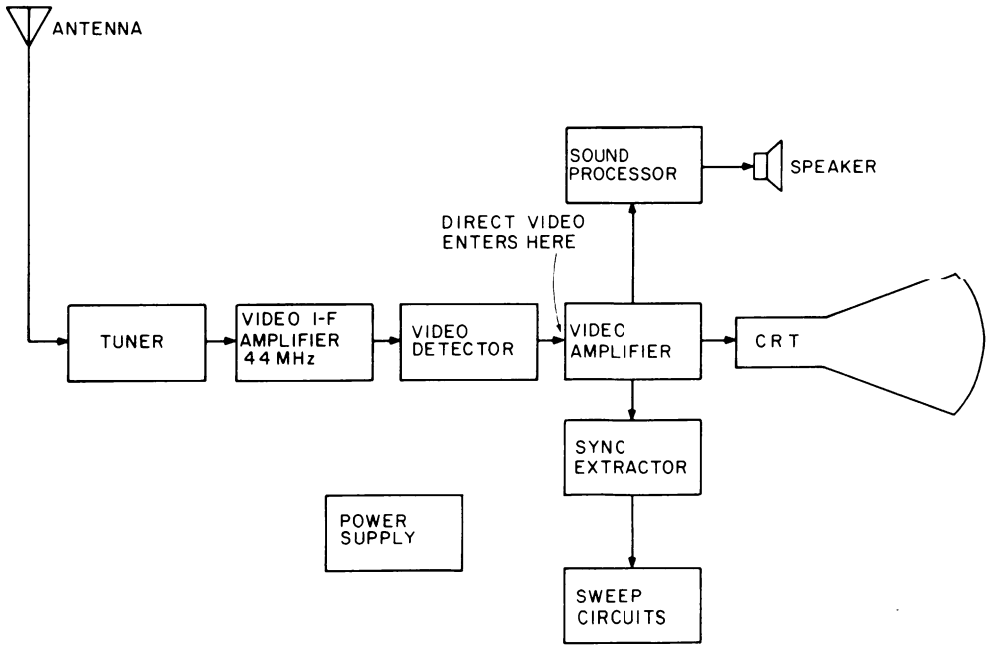
Fig. 2 shows us a typical composite video driver using a 4066 quad analog switch. It gives us a 100 Ohm output impedance and the proper signal levels. Capacitor C1 is used to purposely reduce the video rise and fall times. It is called a smearing capacitor.

Why would we want to further reduce the bandwidth and response of a TV system that's already hurting to begin with? In the case of a quality video monitor, we wouldn't. But if we're using an ordinary run-of-the-mill TV set, particularly one using rf entry, this capacitor can very much improve the display legibility and contrast. Why?

Because we are interested in getting the most legible character of the highest contrast we can. This is not necessarily the one having the sharpest dot rise and fall times. Many things interact to determine the upper video response of a TV display. These include the tuner settings and the i-f response and alignment, the video detector response, video peaking, the sound trap setting, rf cable reflections, and a host of other responses. Many of these stages are underdamped and will ring if fed too sharp a risetime input, giving us a ghosted, shabby, or washed out character. By reducing the video bandwidth going into the system, we can move the dot matrix energy lower in frequency, resulting in cleaner characters of higher contrast.

For most TV displays, intentional smearing will help the contrast, legibility, and overall appearance. The ultimate limit to this occurs when the dots overlap and become illegible. The

Fig. 3. Block diagram of typical B and W television.



optimum amount of intentional smear is usually the value of capacitance that is needed to just close the inside of a "W" presented to the display.

Adding a Video Input

Video inputs are easy to add to the average television set, provided you follow some reasonable cautions. First and foremost, you must have an accurate and complete schematic of the set to be modified, preferably a Sams Photofact or something similar. The first thing to check is the power supply on the set. If it has a power transformer and has the chassis properly safety isolated from the power line, it's a good choice for a TVT monitor. This is particularly true of recent small screen, solid state portable TV sets. On the other hand, if you have a hot chassis type with one side of the power line connected to the chassis, you should avoid its use if at all possible. If you must use this type of set, be absolutely certain to use one of the safety techniques outlined later in Fig. 8.

A block diagram of a typical TV set appears in Fig. 3. UHF or VHF signals picked up by the tuner are downconverted in frequency to a video i-f frequency of 44 MHz and then filtered and amplified. The output of the video i-f is transformer coupled to a video detector, most often a small signal germanium diode. The video detector output is filtered to remove the carrier and then routed to a video amplifier made up of one or more tubes or transistors.

At some point in the video amplification, the black and white signal is split three ways. First, a reduced bandwidth output routes sync pulses to the sync separator stage to lock the set's horizontal and vertical scanning to the video. A second bandpass output sharply filtered to 4.5 MHz extracts the FM sound subcarrier and routes this to a sound i-f amplifier for further processing. The third output is video, which is strongly amplified and then capacitively coupled to the cathode of the picture tube.

The gain of the video amplifier sets the contrast of the display, while the bias setting on the cathode of the picture tube (with respect to its grounded control grid) sets the display brightness. Somewhere in the video amplifier, further rejection of the 4.5 MHz sound subcarrier is usually picked up to minimize picture interference. This is called a sound trap. Sound traps can be a series resonant circuit to ground, a parallel resonant circuit in the video signal path, or simply part of the transformer that is picking off the sound for more processing.

The video detector output is usually around 2 volts peak to peak and usually subtracts from a white level bias setting. The stronger the signal, the more negative the swing, and the blacker the picture. Sync tips are blacker than black, helping to blank the display during retrace times.

Fig. 4 shows us the typical video circuitry of a transistor black and white television. Our basic circuit consists of a diode detector, a unity gain emitter follower, and a variable gain video output stage that is capacitively coupled to the picture tube. The cathode bias sets the brightness, while the video gain sets the contrast. Amplified signals for sync and sound are removed from the collector of the video driver by way of a 4.5 MHz resonant transformer for the sound and a low pass filter for the sync. A parallel resonant trap set to 4.5 MHz eliminates sound interference. Peaking coils on each stage extend the bandwidth by providing higher impedances and thus higher gain to high frequency video signals.

Note particularly the biasing of the video driver. A bias network provides us with a stable source of 3 volts. In the absence of input video, this 3 volts sets the white level of the display, as well as establishing proper bias for both stages. As an increasing signal appears at the last video output transformer, it is negatively rectified by the video detector, thus lowering the 3 volts proportionately. The stronger the signal, the blacker the picture. Sync will be the strongest of all, giving us a blacker than black bias level of only one volt.

The base of our video driver has the right sensitivity we need for video entry, accepting a maximum of a 2 volt peak to peak signal. It also has the right polarity, for a positive going bias level means a whiter picture. *But, an unmodified set is already biased to the white level, and if we want to enter our own video, this bias must be shifted to the black level.*

We have a choice in any TV of direct or ac coupling of our input video. Direct coupling is almost always better as it eliminates any

Fig. 4. Typical video circuitry of transistor B and W TV set.

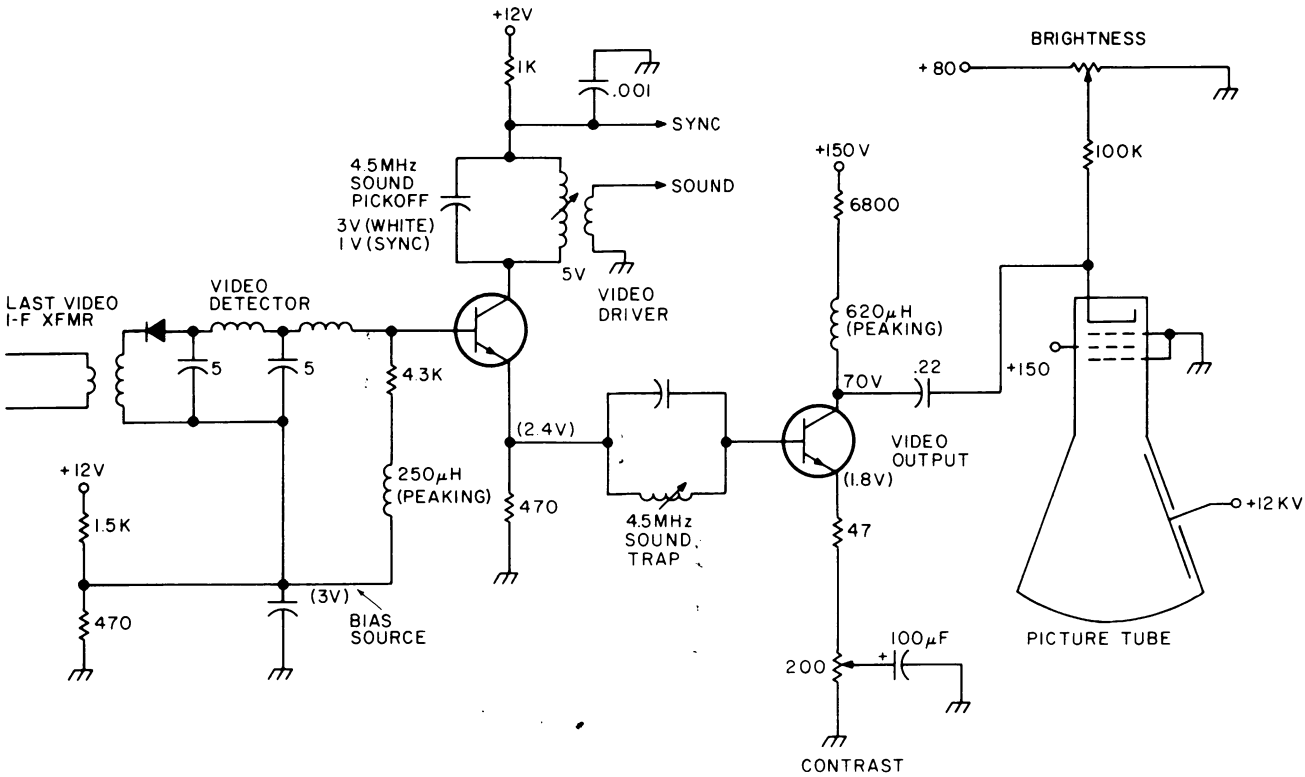
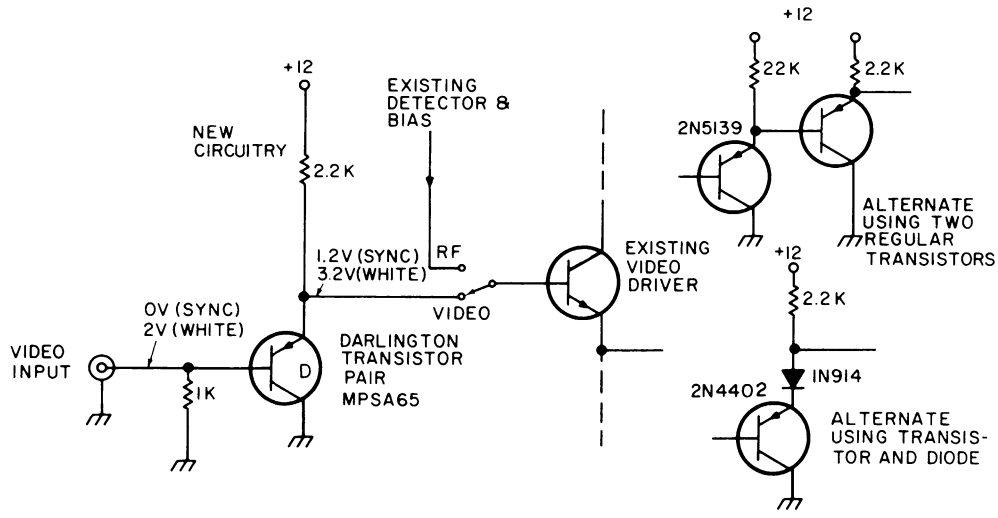


Fig. 5. Direct coupled video uses 1.2 volt offset of Darlington transistor as bias.



shading effects or any change of background level as additional characters are added to the screen. Fig. 5 shows how we can direct couple our video into a transistor black and white set. We provide a video input, usually a BNC or a phono jack, and route this to a PNP Darlington transistor or transistor pair, borrowing around 5 mils from the set's +12 volt supply. This output is routed to the existing video driver stage through a SPDT switch that either picks the video input or the existing video detector and bias network.

The two base-emitter diode drops in our Darlington transistor add up to a 1.2 volt positive going offset; so, in the absence of a video input or at the base of a sync tip, the video driver is biased to a blacker than black sync level of 1.2 volts. With a white video input of 2 volts, the video driver gets biased to its usual 3.2 volts of white level. Thus, our input transistor provides just the amount of offset we need to match the white and black bias levels of our video driver. Note that the old bias network is on the other side of the switch and does nothing in the video position.

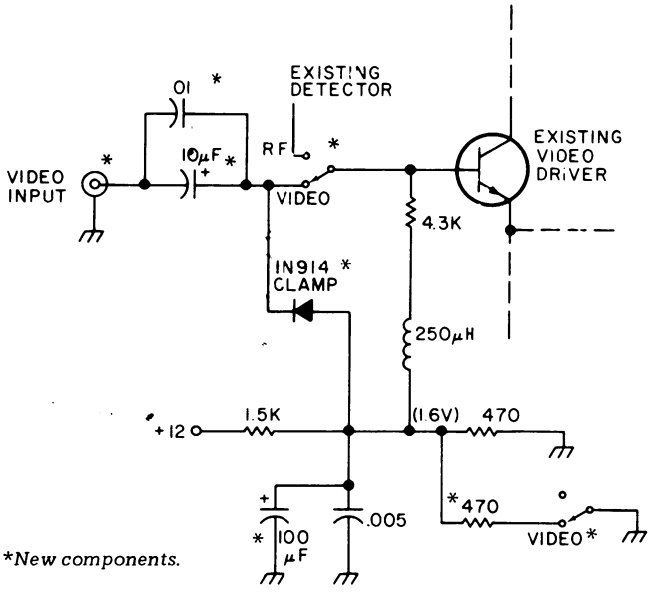
Two other ways to offset our video input are to use two ordinary transistors connected in the Darlington configuration, or to use one transistor and a series diode to pick up the same amount of offset, as shown in Fig. 5. If more or less offset is needed, diodes or transistors can be stacked up further to pick up the right amount of offset.

The important thing is that the video driver ends up with the same level for white bias and for black bias in either position of the switch.

Ac or capacitively coupled video inputs should be avoided. Fig. 6 shows a typical circuit. The TV's existing bias network is lowered in voltage by adding a new parallel resistor to ground to give us a voltage that is 0.6 volts more positive than the blacker than black sync tip voltage. For instance, with a 3 volt white level, and 2 volt peak to peak video, the sync tip voltage would be 1 volt; the optimum bias is then 1.6 volts. Input video is capacitively coupled by a fairly large electrolytic capacitor in parallel with a good high frequency capacitor. This provides for a minimum of screen shading and still couples high frequency signals properly. A clamping diode constantly clamps the sync tips to their bias value, with the 0.6 volt drop of this diode being taken out by the extra 0.6 volts provided for in the bias network. This clamping diode automatically holds the sync tips to their proper value, regardless of the number of white dots in the picture. Additional bypassing of the bias network by a large electrolytic may be needed for proper operation of the clamping diode, as shown in Fig. 6. Note that our bias network is used in both switch positions – its level is shifted as needed for the direct video input.

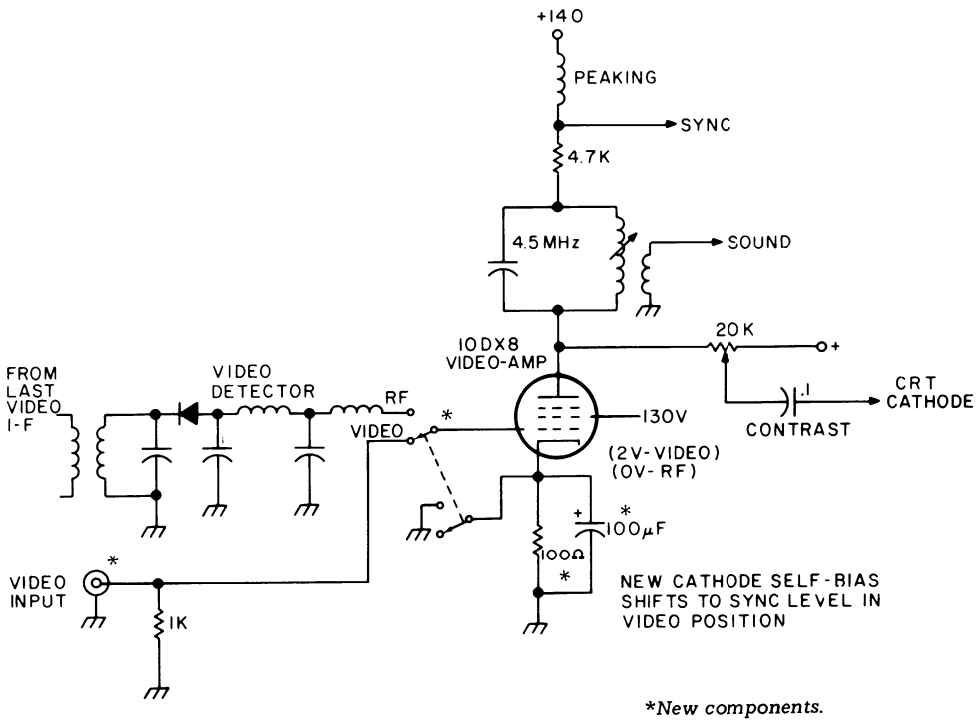
Tube type sets present about the same interface problems as the solid state versions do. Fig. 7 shows a typical direct coupled tube interface. In the unmodified

Fig. 6. Ac coupled video needs shift of bias to black level plus a clamping diode.



*New components.

Fig. 7. Direct coupled video added to tube type B and W television.



**New components.*

circuit, the white level is zero volts and the sync tip black level is minus two volts. If we can find a negative supply (scarce in tube type circuits), we could offset our video in the negative direction by two volts to meet these bias levels.

Instead of this, it is usually possible to self bias the video amplifier to a cathode voltage of +2 volts. This is done by breaking the cathode to ground connection and adding a small resistor (50 to 100 Ohms) between cathode and ground to get a cathode voltage of +2 volts. Once this value is found, a heavy electrolytic bypass of 100 microfarads or more is placed in parallel with the resistor. Switching then grounds the cathode in the normal rf mode and makes it +2 volts in the video entry mode.

In the direct video mode, a sync tip grounded input presents zero volts to the grid, which is self biased minus two volts with respect to the cathode. A white level presents +2 volts to the grid, which equals zero volts grid to cathode.

Should there already be a self bias network on the cathode, it is increased in value as needed to get the black rather than white level bias in the direct video mode.

Hot Chassis Problems

There is usually no shock hazard when we use clip-on rf entry or when we use a direct video jack on a transformer-powered TV. A very severe shock hazard can exist if we use direct video entry with a TV set having one side of the power line connected to the chassis. Depending on which way the line cord is plugged in, there is a 50-50 chance of the hot side of the power line being connected directly to the chassis.

Hot chassis sets, particularly older, power hungry tube versions, should be avoided entirely for direct video entry. If one absolutely must be used, some of the suggestions of Fig. 8 may ease the hazard. These include using an isolation transformer, husky back-to-back filament transformers, three wire power systems, optical coupling of the video input,

and total package isolation. Far and away the best route is simply never to attempt direct video entry onto a hot chassis TV.

Making the Conversion

Fig. 9 sums up how we modify a TV for direct video entry. Always have a complete schematic on hand, and use a transformer style TV set if at all possible. Late models, small screen, medium to high quality solid state sets are often the best display choice. Avoid using junk sets, particularly very old ones. Direct coupling of video is far preferable to ac capacitor coupling. Either method has to maintain the black and white bias levels on the first video amplifier stage. A shift of the first stage quiescent bias from normally white to normally black is also a must. Use short, shielded leads between the video input jack and the rest of the circuit. If a changeover switch is used, keep it as close to the rest of the video circuitry as you possibly can.

Extending Video and Display Bandwidth

By using the direct video input route, we eliminate any bandwidth and response restrictions of an rf modulator, the tuner, video i-f strip, and the video detector filter. Direct video entry should bring us to a 3 MHz bandwidth for a color set and perhaps 3.5 MHz for a black and white model, unless we are using an extremely bad set. The resultant 6 to 7 million dot per second rate is adequate for short character lines of 32, 40, and possibly 48 characters per line. But the characters will smear and be illegible if we try to use longer line lengths and premium (lots of dots) character generators on an ordinary TV. Is there anything we can do to the set to extend the video bandwidth and display response for these longer line lengths?

In the case of a color TV, the answer is probably no. The video response of a color set is limited by an essential delay line and an essential 3.58 MHz trap. Even if we were willing to totally separate the chrominance and luminance channels, we'd still be faced with an absolute limit set by the number of holes per horizontal line in the shadow mask of the tube. This explains why video color displays are so expensive and so rare. Later on, we'll look at what's involved in adding color to the shorter line lengths.

With a black and white TV, there is often quite a bit

Fig. 8. Getting Around a Hot Chassis Problem.

Hot chassis problems can be avoided entirely by using only transformer-powered TV circuits or by using clip-on rf entry. If a hot chassis set must be used, here are some possible ways around the problem:

1. Add an isolation transformer.

A 110 volt to 110 volt isolation transformer whose wattage exceeds that of the set may be used. These are usually expensive, but a workable substitute can be made by placing two large surplus filament transformers back to back. For instance, a pair of 24 volt, 4 Amp transformers can handle around 100 Watts of set.

2. Use a three wire system with a solid ground.

Three prong plug wiring, properly polarized, will force the hot chassis connection to the cold side of the power line. This protection is useful only when three wire plugs are used in properly wired outlets. A severe shock hazard is reintroduced if a user elects to use an adaptor or plugs the system into an unknown or improperly wired outlet. The three wire system should **NOT** be used if anyone but yourself is **ever** to use the system.

3. Optically couple the input video.

Light emitting diode-photocell pairs are low in cost and can be used to optically couple direct video, completely isolating the video input from the hot chassis. Most of these optoelectronic couplers do not have enough bandwidth for direct video use; the Litronix IL-100 is one exception. Probably the simplest route is to use two separate opto-isolators, one for video and one for sync, and then recombine the signals inside the TV on the hot side of the circuit.

4. Use a totally packaged and sealed system.

If you are only interested in displaying messages and have no other input/output devices, you can run the entire circuit hot chassis, provided everything is sealed inside one case and has no chassis-to-people access. Interface to teletypes, cassettes, etc., cannot be done without additional isolation, and servicing the circuit presents the same shock hazards that servicing a hot chassis I V does.

we can do to present long lines of characters, depending on what set you start out with and how much you are willing to modify the set.

The best test signal you can use for bandwidth extension is the dot matrix data you actually want to display, for the frequency response, time delay, ringing, and overshoot all get into the act. What we want to end up with is a combination that gives us reasonably legible characters.

A good oscilloscope (15 MHz or better bandwidth) is very useful during bandwidth extension to show where the signal loses its response in the circuit. At any time during the modification process, there is usually one response bottleneck. This, of course, is what should be attacked first. Obviously the better a TV you start with, the easier will be the task. Tube type gutless wonders, particularly older ones, will be much more difficult to work with than with a modern, small screen, quality solid state portable.

Several of the things we can do are watching the control settings, getting rid of the sound trap, minimizing circuit strays, optimizing spot size, controlling peaking, and shifting to higher current operation. Let's take a look at these in turn.

Control Settings

Always run a data display at the lowest possible contrast and using only as much brightness as you really need. In many circuits, low contrast means a lower video amplifier gain, and thus less of a gain-bandwidth restriction.

Eliminate the Sound Trap

The sound trap adds a notch at 4.5 MHz to the video response. If it is eliminated or switched out of the circuit, a wider video bandwidth automatically

Fig. 9. How to Add a Direct Video Input to a TV Set.

1. Get an accurate and complete schematic of the set — either from the manufacturer's service data or a Photofact set. **Do not try adding an input without this schematic!**

2. Check the power supply to see if a power transformer is used. If it is, there will be no shock hazard, and the set is probably a good choice for direct video use. If the set has one side of the power line connected to the chassis, a severe shock hazard exists, and one of the techniques of Fig. 8 should be used. **Avoid the use of hot chassis sets.**

3. Find the input to the first video amplifier stage. Find out what the white level and sync level bias voltages are. The marked or quiescent voltage is usually the white level; sync is usually 2 volts less. A transistor TV will typically have a +3 volt white level and a +1 volt sync level. A tube type TV will typically have a zero volt white level and a -2 volt sync level.

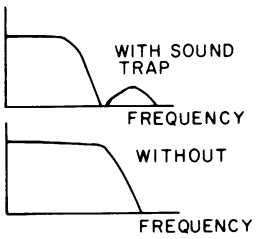
4. Add a changeover switch using minimum possible lead lengths. Add an input connector, either a phono jack or the premium BNC type connector. Use shielded lead for interconnections exceeding three inches in length.

5. Select a circuit that couples the video and biases the first video amplifier stage so that the white and sync levels are preserved. For transistor sets, the direct coupled circuits of Fig. 5 may be used. For tube sets, the circuit of Fig. 7 is recommended. Avoid the use of ac coupled video inputs as they may introduce shading problems and changes of background as the screen is filled.

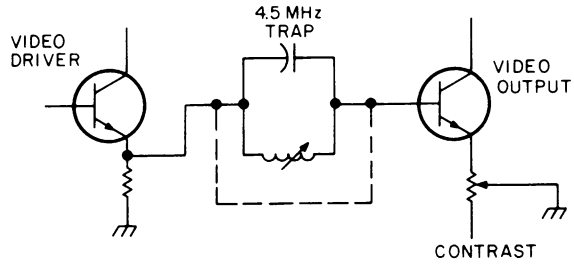
6. Check the operation. If problems with contrast or sync tearing crop up, recheck and adjust the white and sync input levels to match what the set uses during normal rf operation. Note that the first video stage must be biased to the **white** level during rf operation and to the **sync** level for direct video use. The white level is normally two volts more positive than the sync level.

Fig. 10. Removing the sound trap can extend video bandwidth.

(a) Response

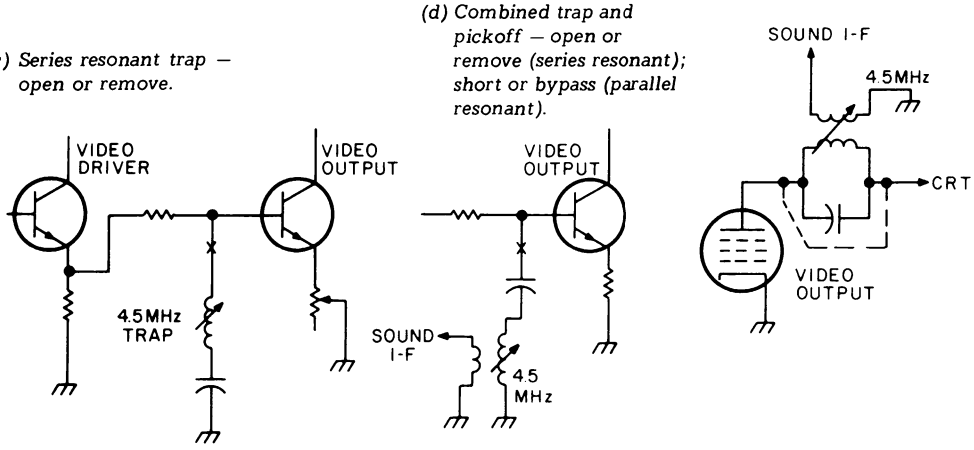


(b) Parallel resonant trap — short or bypass.



(c) Series resonant trap — open or remove.

(d) Combined trap and pickoff — open or remove (series resonant); short or bypass (parallel resonant).



results. Fig. 10 shows us the response changes and the several positions for this trap. Generally, series resonant traps are opened and parallel resonant traps are shorted or bypassed through suitable switching or outright elimination. The trap has to go back into the circuit if the set is ever again used for ordinary program reception. Sometimes simply backing the slug on the trap all the way out will improve things enough to be useful.

Minimizing Strays

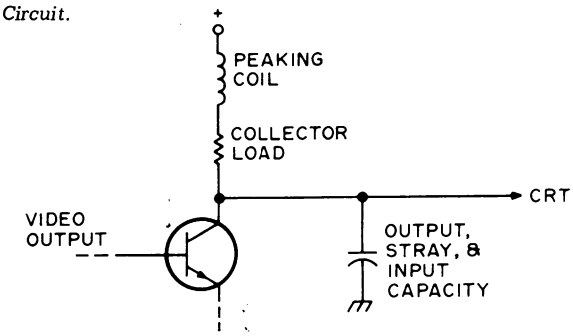
One of the limits of the video bandwidth is the stray capacitance both inside the video output stage and in the external circuitry. If the contrast control is directly in the signal path and if it has long leads going to it, it may be hurting the response. If you are using the TV set exclusively for data display, can you rearrange the control location and simplify and shorten the video output to picture tube interconnections?

Additional Peaking

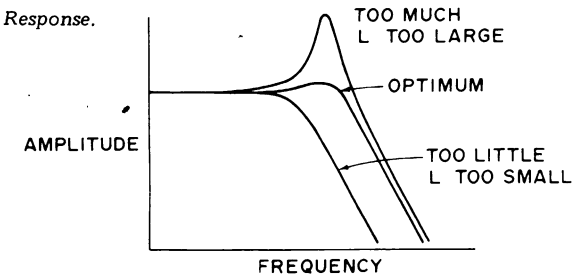
Most TV sets have two peaking networks. The first of these is at the video detector output and compensates for the vestigial sideband transmission signal that makes sync and other low frequency signals double the amplitude of the higher frequency ones. The second of these goes to the collector or plate of the video output stage and raises the circuit impedance and thus the effective gain for very high frequencies. Sometimes you can alter this second network to favor dot presentations. Fig. 11 shows a typical peaking network and the effects of too little or too much peaking. Note that the stray capacitance also enters into the peaking, along with the video amplifier output capacitance and the picture tube's input capacitance. Generally, too little peaking will give you low contrast dots, while too much will give you sharp dots, but will run dots together and shift the more continuous portions of the characters objectionably. Peaking is changed by increasing or decreasing the series inductor from its design value.

Fig. 11. Adjusting the peaking coil can extend video response.

(a) Circuit.



(b) Response.



Running Hot

Sometimes increasing the operating current of the video output stage can increase the system bandwidth — IF this stage is in fact the limiting response, IF the power supply can handle the extra current, IF the stage isn't already parked at its gain-bandwidth peak, and IF the extra heat can be gotten rid of without burning anything up. Usually, you can try adding a resistor three times the plate or collector load resistor in parallel, and see if it increases bandwidth by 1/3. Generally, the higher the current, the wider the bandwidth, but watch

carefully any dissipation limits. Be sure to provide extra ventilation and additional heatsinking, and check the power supply for unhappiness as well. For major changes in operating current, the emitter resistors and other biasing components should also be proportionately reduced in value.

Spot Size

Even with excellent video bandwidth, if you have an out-of-focus, blooming, or changing spot size, it can completely mask character sharpness. Spot size ends up the ultimate limit to resolution, regardless of video bandwidth.

Once again, brightness and contrast settings will have a profound effect, with too much of either blooming the spot. Most sets have a focus jumper in which ground or a positive voltage is selected. You can try intermediate values of voltage for maximum sharpness. Extra power supply filtering can sometimes minimize hum and noise modulation of the spot.

Anything that externally raises display contrast will let you run with a smaller beam current and a sharper spot. Using circularly polarized filters, graticule masks, or simple colored filters can minimize display washout from ambient lighting. Fig. 12 lists several sources of material for contrast improvement. Much of this is rather expensive, with pricing from $10 to $25 per square foot being typical. Simply adding a hood and positioning the display away from room lighting will also help and is obviously much cheaper.

Fig. 12. Contrast Enhancing Filter Materials.

Circularly polarized filters:

Polaroid Corp.
Cambridge MA 02139

Anti-reflection filters:

Panelgraphic Corp.
10 Henderson Dr.
West Caldwell NJ 07006

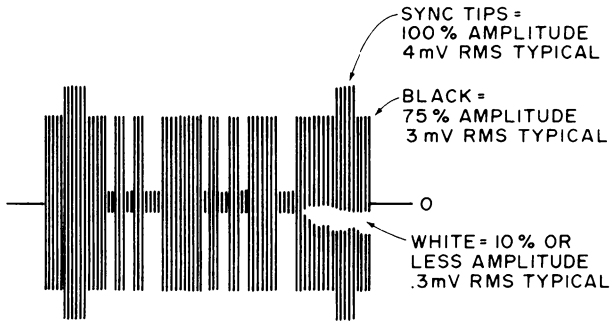
Light control film:

3M Visual Products Div.
3M Center
St. Paul MN 55101

Acrylic plexiglas filter sheets:

Rohm and Haas
Philadelphia PA 19105

Fig. 13. Standard rf interface levels. Impedance = 300Ω. Carrier frequency per Fig. 14.



Direct Rf Entry

If we want the convenience of a "free" display, the freedom from hot chassis problems, and "use it anywhere" ability, direct rf entry is the obvious choice. Its two big limitations are the need for FCC type approval, and a limited video bandwidth that in turn limits the number of characters per line and the number of dots per character.

An rf interface standard is shown in Fig. 13. It consists of an amplitude modulated carrier of one of the standard television channel video frequencies of Fig. 14. Channel 2 is most often used with a 55.250 MHz carrier frequency, except in areas where a local commercial Channel 2 broadcast is intolerably strong. Circuit cost, filtering problems, and stability problems tend to increase with increasing channel number.

The sync tips are the strongest part of the signal, representing 100% modulation, often something around 4 millivolts rms across a 300 Ohm line. The black level is 75% of the sync level, or about 3 millivolts for 4 millivolt sync tips. White level is less than 10% of maximum. Note that the signal is weakest when white and strongest when sync. This is the exact opposite of the video interface of Fig. 1.

Rf modulators suitable for clip-on rf entry TV typewriter use are called Class 1 TV Devices by the FCC. A Class 1 TV device is supposed to meet the rules and regulations summarized in Fig. 15.

Fig. 16 shows us a block diagram of the essential parts of a TV modulator. We start

Fig. 14. Television Picture Carrier Frequencies.

Channel 2	**55.25 MHz**
Channel 3	**61.25 MHz**
Channel 4	**67.25 MHz**
Channel 5	**77.25 MHz**
Channel 6	**83.25 MHz**

Fig. 15. FCC Regulations on Class 1 TV Devices. More complete information appears in subpart H of Part 15 and subpart F of Part 2 of the Federal Communications Commission Rules and Regulations. *It is available at many large technical libraries.*

A Class 1 TV device generates a video modulated rf carrier of a standard television channel frequency. It is directly connected to the antenna terminals of the TV set.

The maximum rms rf voltage must be less than 6 millivolts using a 300 Ohm output line.

The maximum rf voltage on any frequency more than 3 MHz away from the operating channel must be more than 30 dB below the peak in-channel output voltage.

An antenna disconnect switch of at least 60 dB attenuation must be provided.

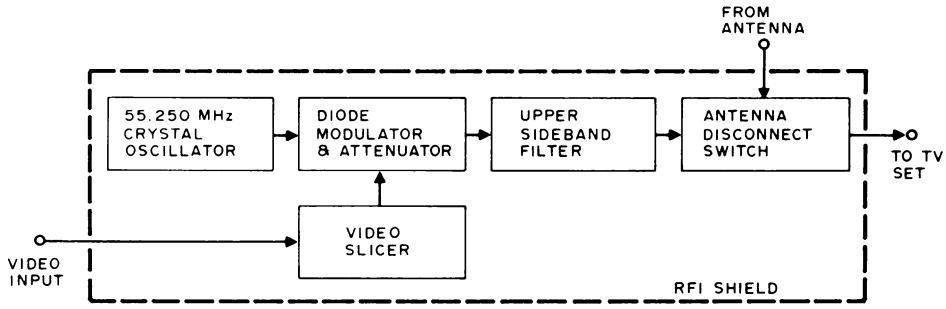
No user adjustments are permitted that would exceed any of the above specifications.

Residual rf radiation from case, leads and cabinet must be less than 15 microvolts per meter.

A Class 1 TV device must not interfere with TV reception.

Type approval of the circuit is required. A filing fee of $50 and an acceptance fee of $250 is involved.

Fig. 16. Block diagram of rf modulator.



with a stable oscillator tuned to one of the Fig. 14 frequencies. A crystal oscillator is a good choice, and low cost modules are widely available. The output of this oscillator is then amplitude modulated. This can be done by changing the bias current through a silicon small signal diode. One milliampere of bias current makes the diode show an ac and rf impedance of 26 Ohms. Half a mil will look like 52 Ohms, and so on. The diode acts as a variable resistance attenuator in the rf circuit, whose bias is set and changed by the video circuit.

Since diode modulators are non-linear, we can't simply apply a standard video signal to them and get a standard rf signal out. A differential amplifier circuit called a video slicer may be used to compensate for this non-linearity. The video slicer provides three distinct currents to the diode modulator. One of these is almost zero for the white level, while the other two provide the black and sync levels. A contrast control that sets the slicing level lets you adjust the sync tip height with respect to the black level. The video slicer also minimizes rf getting back into the video. An attenuator to reduce the size of the modulated signal usually follows the diode modulator.

An upper side band filter removes most of the lower sideband from the AM modulated output, giving us a vestigial sideband signal that stays inside the channel band limits. This same filter eliminates second harmonic effects and other spurious noise. The filter's output is usually routed to an antenna disconnect switch and the TV's antenna terminals. A special switch is needed to provide enough isolation.

Some of the actual circuitry involved is shown in Fig. 17. The video slicer consists of a pair of high gain, small signal NPN transistors, while the oscillator is a commercially available module.

Rf entry systems always must be direct coupled to the antenna terminals of the set and should never provide any more rf than is needed for a minimum snow-free picture. They should be permanently tuned to a single TV channel. Under no circumstances should an antenna or cable service hookup remain connected to the set during TVT use, nor should radiation rather than a direct rf cable connection ever be used.

Color Techniques

We can add a full color capability to a TV typewriter system fairly easily and cheaply — provided its usual black and white video dot rate is low enough in frequency to be attractively displayed on an ordinary color TV. Color may be used to emphasize portions of a message, to attract attention, as part of an electronic game, or as obvious added value to a graphics display. Color techniques work best on TV typewriter systems having a horizontal frequency very near 15,735 Hertz.

All we basically have to do is generate a subcarrier sine wave to add to the video output. The phase of this subcarrier (or its time delay) is shifted with respect to what the phase was immediately after each horizontal sync pulse to generate the various colors.

Fig. 18 shows us the differences between normal color and black and white operation. Black and white baseband video is some 4 MHz wide and has a narrow 4.5 MHz sound subcarrier. The video is amplitude modulated, while the sound is narrow band frequency

Fig. 17. Channel two oscillator, modulator, video slicer and attenuator. R sets output level.

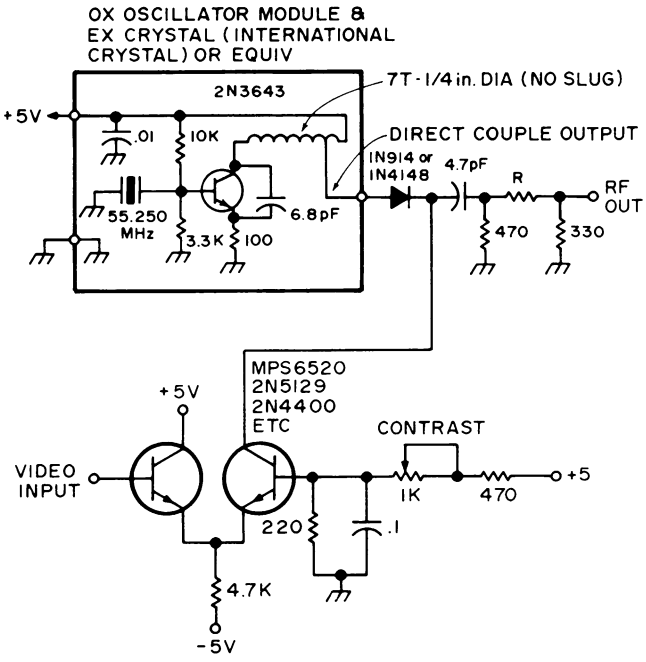
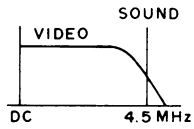
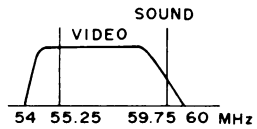


Fig. 18. Differences between color and black and white spectra.

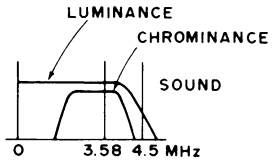
(a) Black and white – baseband video.

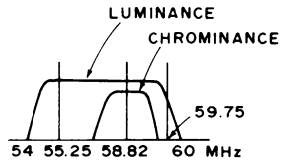




(b) Black and white – Channel two rf.

(c) Color – baseband video.





(d) Color – Channel two rf.

modulated. This translates up to a 6 MHz rf channel with a vestigial lower sideband as shown in Fig. 18(b).

To generate color, we add a new pilot or subcarrier at a magic frequency of 3.579545 MHz – see Fig. 18(c). What was the video is now called the luminance, and is the same as the brightness in a black and white system. The new subcarrier and its modulation is called the chrominance signal and determines what color gets displayed and how saturated the color is to be.

Since the black and white information is a sampled data system that is scanned at the vertical and horizontal rates, there are lots of discrete holes in the video spectrum that aren't used. The color subcarrier is designed to stuff itself into these holes (exactly in a NSTC color system, and pretty much in a TVT display). Both chrominance and luminance signals use the same spectral space, with the one being where the other one isn't, overlapping comb style.

The phase or relative delay of the chrominance signal with respect to a reference determines the instantaneous color, while the amplitude of this signal with respect to the luminance sets the saturation of the color. Low amplitudes generate white or pastel shades, while high amplitudes of the chrominance signal produce saturated and deep colors.

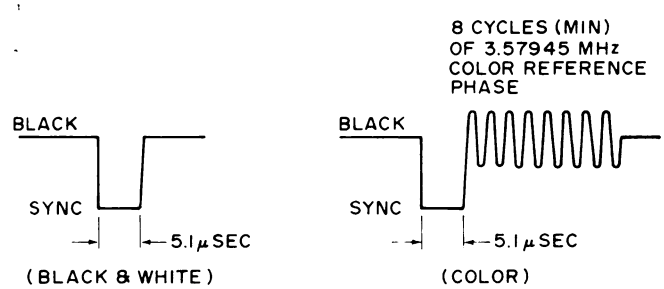
At least eight cycles of a reference or burst color phase are transmitted immediately following each horizontal sync pulse as a timing reference, as shown in Fig. 19. The burst is around 25% of maximum amplitude, or about the peak to peak height of a sync pulse.

The TV set has been trained at the factory to sort all this out. After video detection, the set splits out the chrominance channel with a bandpass amplifier and then synchronously demodulates it with respect to an internal 3.58 MHz reference. The phase of this demodulation sets the color and the amplitude sets the saturation by setting the ratios of electron beam currents on the picture tube's red, blue and green guns.

Meanwhile, the luminance channel gets amplified as brightness style video. It is delayed with a delay line to make up for the time delay involved in the narrower band color processing channel. It is then filtered with two traps – the 4.5 MHz sound trap, and a new trap to get rid of any remaining 3.58 MHz color subcarrier that's left. The luminance output sets the overall brightness by modulating the cathodes of all three color guns simultaneously.

Just after each horizontal sync pulse, the set looks for the reference burst and uses this reference in a phase

Fig. 19 Adding a color reference burst to the back porch of the horizontal sync pulses.



J3 Keyboard Connector (between U64 and U65)

Sol-PC, Rev. 2,E
10/18/76

pin no.	Signal name	pin no.	Signal name
1	ground	11	ground
2	+5v	12	+5v
3	Kbd Data Ready	13	Restart
4	Break	14	Local
5	Kbd Data Ø	15	KBd Data 4
6	Kbd Data 1	16	KBd Data 5
7	Kbd Data 2	17	KBD Data 6
8	Kbd Data 3	18	KBD Data 7
9	+5v	19	+5v
10	ground	20	ground

J4 Display Expansion Connector (between U28, 29)

pin no.	Signal name	pin no.	Signal name
1	ground	11	ground
2	N.C.	12	N.C.
3	Char. addr. 4	13	Dot Clock, 14.318MHz
4	Character clock	14	Composite sync. out
5	Char. addr. Ø	15	TTL Serial Data Out
6	Char. addr. 1	16	Composite blanking out
7	Char. addr. 2	17	Scan advance out
8	Char. addr. 3	18	Char. addr. 5
9	N.C.	19	N.C.
10	ground	20	ground

J5 Personality Module Edge Connector

pin no.	Signal name	pin no.	Signal name
B15	Ground	A15	Ground
B14	+5VDC	A14	+5VDC
B13	Addr. 9	A13	Addr. Ø
B12	Addr. 8	A12	Addr. 4
B11	Addr. 7	A11	Addr. 3
B10	INT Bus Ø	A10	Addr. 2
B9	INT Bus 1	A9	Addr. 1
B8	INT Bus 2	A8	Addr. 5
B7	INT Bus 3	A7	Addr. 6
B6	INT Bus 4	A6	C4
B5	INT Bus 5	A5	CØ
B4	Program Ø	A4	INT Bus 6
B3	Program 1	A3	INT Bus 7
B2	Program 2	A2	-12VDC
B1	Program 3	A1	+12VDC

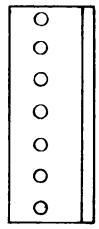
J6 Audio Out for CUTS Cassette Interface: Mini-phone jack at rear panel

J7 Audio In for CUTS Cassette Interface: Mini-phone jack at rear panel

J8 Tape Motor Control 1: (See output port FA, bit 7) Sub-mini jack at rear panel

J9 Tape Motor Control 2: (See output port FA, bit 6) Sub-mini jack at rear panel

J10 DC Power Connector, Sol-PC



S-100 Bus Definitions

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	+8V	+8 Volts	Unregulated voltage on bus, supplied to PC boards and regulated to 5V supplied by Sol-20 supply
2	-16V	-16 Volts	Positive unregulated voltage supplied by Sol-20 power supply
3	XRDY	EXTERNAL READY	External ready input to CPU ready circuitry
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt Line #7	
12	XRDY2	EXTERNAL READY #2	not used by Sol-PC
13 to 17	TO BE DEFINED		
18	$\overline{\text{STAT DSB}}$	STATUS DISABLE	-Allows the buffers for the 8 status lines to be tri-stated
19	$\overline{\text{C/C DSB}}$	COMMAND/CONTROL DISABLE	-Allows the buffers for the 6 output command/control lines to be tri-stated
20	UNPROT	UNPROTECT	-not used by Sol-PC electronics
21	$\overline{\text{SS}}$	SINGLE STEP	-not used by Sol-PC
22	$\overline{\text{ADD DSB}}$	ADDRESS DISABLE	-Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DSB}}$	DATA OUT DISABLE	-Allows the buffers for the 8 data output lines to be tri-stated
24	Ø2	PHASE 2 CLOCK	
25	Ø1	PHASE 1 CLOCK	
26	PHLDA	HOLD ACKNOWLEDGE	Processor command/control output signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle.

PIN NUMBER	SYMBOL	NAME	FUNCTION
27	PWAIT	WAIT	-Processor command/control signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle
28	PINTE	INTERRUPT ENABLE	-Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are inhibited.
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	(MSB)
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DI01	Data In/Out line #1	same as pin 94
36	DIOØ	Data In/Out line #0	same as pin 95
37	A10	Address Line #10	
38	DIO4	Data In/Out Line #4	same as pin 91
39	DIO5	Data In/Out Line #5	same as pin 92
40	DIO6	Data In/Out Line #6	same as pin 93
41	DIO2	Data In/Out Line #2	same as pin 88
42	DIO3	Data In/Out Line #3	same as pin 89
43	DIO7	Data In/Out Line #7	same as pin 90
44	SM1	MACHINE CYCLE 1	-Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUTPUT	-Status output signal that indicates the address bus contains the address of an output device and the data bus will cohtain the ouput data when PWR is active
46	SINP	INPUT	-Status output signal that indicates the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMORY READ	-Status output signal that indicates the data bus will be used to read memory data
48	SHLTA	HALT ACKNOWLEDGE	-Status output signal that acknowledges a HALT instruction
49	$\overline{\text{CLOCK}}$	$\overline{\text{CLOCK}}$	- Inverted output of the Ø2 CLOCK
50	GND	GROUND	
51	+8V	+8 Volts	Unregulated input to 5 volt regulators supplied by Sol-20 power supply
52	-16V	-16 Volts	Negative unregulated voltage supplied by Sol-20 power supply

PIN NUMBER	SYMBOL	NAME	FUNCTION
53	SSWI	SENSE SWITCH INPUT	not used by Sol
54	EXT CLR	EXTERNAL CLEAR	not used by Sol-PC electronics
55	RTC	REAL TIME CLOCK	not used by Sol-PC electronics
56	STSTB	STATUS STROBE	not used by Sol
57	DIGI	DATA INPUT GATE #1	When low forces PDBINS low and forces CPU input multiplexers to the DIO bus. During CPU DBIN cycle, disables CPU DIO bus drivers
58	FRDY	FRONT PANEL READY	-When low disables MWRITE driver
59 to 64	TO BE DEFINED		
65	MREQ	MEMORY REQUEST	- Z 80 signal not used by Sol-PC electronics
66	REF	REFRESH	- Z 80 signal not used by Sol-PC electronics
67	PHANTOM	PHANTOM DISABLE	-Output from CPU section used to disable RAM or ROM during power on initialization program execution
68	MWRITE	MEMORY WRITE	-Indicates that the data present on the Data Out Bus is to be written into the memory location currently on the address bus
69	PS	PROJECT STATUS	-not used by Sol-PC electronics
70	PROT	PROTECT	-not used by Sol-PC electronics
71	RUN	RUN	- not used by Sol-PC electronics
72	PRDY	PROCESSOR READY	- Memory and I/O input to the CPU Board wait circuitry
73	PINT	INTERRUPT REQUEST	- The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request.
74	PHOLD	HOLD	-Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle
75	PRESET	RESET	-Processor command/control input; while activated, the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	-Processor command/control output; provides a signal to indicate the beginning of each machine cycle
77	PWR	WRITE	-Processor command/control output; used for memory write or I/O output control. Data on the data bus is stable while the PWR is active
78	PDBIN	DATA BUS IN	-Processor command/control output; indicates to external circuits that the data bus is in the input mode

PIN NUMBER	SYMBOL	NAME	FUNCTION
79	A0	Address Line #0	(LSB)
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DI02	Data In/Out Line #2	same as pin 41
89	DI03	Data In/Out Line #3	same as pin 42
90	DI07	Data In/Out Line #7	same as pin 43
91	DI04	Data In/Out Line #4	same as pin 38
92	DI05	Data In/Out Line #5	same as pin 39
93	DI06	Data In/Out Line #6	same as pin 40
94	DI01	Data In/Out Line #1	same as pin 35
95	DIOØ	Data In/Out Line #0	same as pin 36
96	SINTA	INTERRUPT ACKNOWLEDGE	-Status output signal; acknowledges signal for INTERRUPT request
97	$\overline{SWO}$	WRITE OUT	-Status output signal; indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	-Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer
99	$\overline{POC}$	POWER-ON CLEAR	
100	GND	GROUND	

SWITCH FUNCTION DEFINITION -- Display Ctrl---Schematic Drawing #4

Switch No.	Mnemonic	Function ON	OFF
S1-1	RST	Restart to Zero	RUN (Dwg. #1)
S1-2	not used		
S1-3	BLANK	Blank Ctrl Characters	Display Ctrl Char.
S1-4	Polarity		
S1-5	BLINK	Blinking cursor	*Solid or NO cursor
S1-6	SOLID	Solid cursor	*Blinking or NO cursor

*NO cursor if S1-5 and S1-6 are off at same time.
Both switches should not be on at the same time.

Drawing #3 -- Sense Switch

Switch No.	Mnemonic	Function ON	OFF	
S2-1	SSWØ	LSB, data bit	Ø=LO	HI
S2-2thruS2-7		etc.	LO	HI
S2-8	SSW7	MSB data bit 7	LO	HI

SERIAL I/O BAUD RATE SWITCH -- Schematic Drawing #3

Switch No.	Mnemonic	Function ON	OFF
S3-1	75	75 BAUD	* Do not turn more than
S3-2	11	110 BAUD	one switch on at a time
S3-3	15	150 BAUD	
S3-4	30	300 BAUD	
S3-5	60	600 BAUD	
S3-6	12	1200 BAUD	
S3-7	24/48	2400 or 4800	(normally 2400 if not jumpered K to M)
S3-8	96	9600 BAUD	

SERIAL I/O CONTROL -- Schematic Drawing #3

Switch No.	Mnemonic	ON	OFF
S4-1	PS	Parity even	Parity odd (if S4-5 on)
S4-2	WLS 1	Data word length	8bits 7bits 6bits 5bits
S4-3	WLS 2		ON ON OFF OFF
			ON OFF ON OFF
S4-4	SBS	1 stop bit	2 stop bits (1.5 if 5bits/word)
S4-5	PI	Parity	No parity
S4-6	F/H	Half duplex	Full duplex

MEMORY ALLOCATION: ON CARD

Hexidecimal Address	Function
CØØØ - C7FF	Personality Module ROM or PROM (2048 words)
C8ØØ - CBFF	System RAM (1024 words)
CCØØ - CFFF	Display RAM Memory (1024 characters)

ON CARD INPUT PORT ALLOCATION

Hexidecimal Port Address	Function
F8	Status, Serial Comm. channel
F9	Serial Communication Channel Data
FA	Aux. Status. Cassette tape interface, parallel I/O, keyboard input
FB	Audio Cassette (CUTS) Data
FC	Keyboard Data (from J3)
FD	Parallel Port Data (from J2)
FE	Display Status
FF	Sense Switch (S2-1 thru S2-8)

OUTPUT PORTS

Hex Port Address	Function
F8	Control, Serial Comm. Channel
F9	Data, Serial Comm. Channel
FA	Control, Parallel I/O, CUTS Cassette I/O
FB	Data, CUTS audio cassette Interface
FC	Alarm (optional)
FD	Data, Parallel output Data channel
FE	Scroll control, Display Section
FF	not used in Sol-PC

STATUS PORT INPUT BIT ASSIGNMENTS

PORT F8 (STATUS, SERIAL COMM. CHANNEL)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	SCD	Serial Carrier Detect (EIA)	1 carrier
1	SDSR	Serial Data Set Ready (EIA)	Ø link ok
2	SPE	Serial Parity Error	1 error
3	SFE	Serial Framing Error	1 error
4	SOE	Serial Overrun Error	1 error
5	SCTS	Serial Clear to Send (EIA)	Ø clear
6	SDR	UART Serial Data Ready	1 ready
7	STBE	UART Serial Transmit Buffer Empty	1 empty

PORT FA (AUX. STATUS, CASSETTE TAPE INTERFACE, PARALLEL I/O, KEYBOARD INPUT)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	KDR	Keyboard Data Ready	Ø ready
1	PDR	Parallel Data Ready	Ø ready
2	PXDR	Parallel eXternal Device Ready	Ø ready
3	TFE	Tape Framing Error	1 error
4	TOE	Tape Overrun Error	1 error
5	not used		
6	TDR	Tape Data Ready	1 ready
7	TTBE	Tape Transmitter Buffer Empty	1 empty

PORT FE (DISPLAY STATUS)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	SOK	Scroll OK; ¼ sec timeout after scroll	Ø time complete

CONTROL PORT OUTPUT BIT ASSIGNMENTS

PORT F8 (CONTROL, SERIAL COMM. CHANNEL)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
4	SRTS	Serial Request to Send	1 request

PORT FA (CONTROL, PARALLEL I/O, CUTS CASSETTE I/O)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
3	PIE	Parallel Input Enable	1 pin 3 J2 low
4	PUS	Parallel Unit Select	0 pin 14 J2 low
5	TBR	Tape Baud Rate (300/1200)	0 1200 Baud
6	TT2	Tape Transport 2	0 run tape
7	TT1	Tape Transport 1	0 run tape

PORT FE (SCROLL CONTROL, DISPLAY SECTION)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø - 3	BDLA	Beginning Display Line Absolute address	4-bit data nybble
4 - 7	FDSP	First Displayed Line Screen Position	4-bit data nybble

CONNECTOR DESIGNATION

J1	Serial data	J6	Cassette Tape Audio Out
J2	Parallel Data	J7	Cassette Tape Audio In
J3	Keyboard	J8	Tape Motor 1
J4	Display Expansion	J9	Tape Motor 2
J5	ROM Personality Module	J10	PC Power
		J11	S-100 Bus Expansion

Processor Technology

The Sol Systems Manual is organized in a modular fashion. Purchasers of different Sol models will receive the appropriate sections of the manual. This mailing is to purchasers of Sol-PC, Sol-10 and Sol-20 units and includes Sections I, III, IV, IX and X, as well as numerous appendices. Please see the Table of Contents on pages i and ii. Sol-10 and S01-20 owners will also receive sections II and V through VIII.

We will soon be sending more sections to you as they are printed. At the same time we will ship the Sol System binder and Sol-BASIC5 cassette along with two computer games and further diagnostic software. Sol-PC purchasers will also receive section VIII and Appendix V.

PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080
CABLE ADDRESS "PROCTEC"

Sol-REG (DOES NOT APPLY TO REV B AND ABOVE)

Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #2

The Sol-REG PC board shipped with your kit contains an error that existed in our original art and a silk screen (legend) error. These errors relate specifically to the SCR1 installation portion of Step 10 and the Sol-20 DC cable installation instruction (Step 13) in Section II of the Sol Systems Manual.

Reference Section II, Step 10, SCR1 Installation

With your kit, use the following procedure to install SCR1 in place of the instructions provided on Page II-8 of the manual:

( ) Position SCR1 (IR106B2 or MCR106-2) on heat sink with component nomenclature up and observe how the left and center leads must be bent to install SCR1 as shown in Figure 1. Bend these two leads as required and install a ½" piece of spaghetti over the center lead. Place circular mica insulator between heat sink and SCR1, insert leads and fasten SCR1-insulator-sink to PC board with a 4-40 x 7/16 screw, lockwasher and nut. Insert screw from back (solder) side of board and drive nut finger tight.

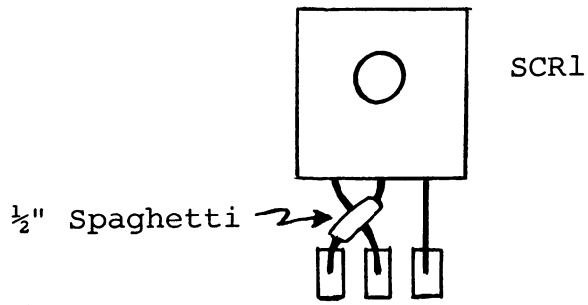


Figure 1. SCR1 installation.

Reference Section II, Step 13.

On the Sol-REG PC board you received, two pads are labeled X5. One is located in the upper right-hand area of the board above C4 and to the right of pad T3; the other is located between C5 and FWB2 just above pad T4.

IGNORE THE X5 PAD LOCATED ABOVE C4.

Connect the red-white lead of the Sol-20 DC cable to the X5 located between C5 and FWB2.

CN #2

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CABLE ADDRESS "PROCTEC"

Sol POWER SUPPLY

Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #4

Reference Section II, Page II-9

Add the following step to "Assembly-Test Procedure":

( ) Step 13. Test Sol-REG for short circuits. Check for continuity between FWB1 (MDA970-1) mounting screw and the following points. The resistance should be greater than 20 ohms in all cases.

X2
T2
T1
Q1, Emitter
Q1, Base
Q1, Collector
D1, right-hand lead
R1, left hand lead
D3, top lead
D4, top lead
*D3, bottom lead
*D4, bottom lead

*Resistance will be initially low due to C4 and C5, but it should increase to greater than 20 ohms after a few seconds.

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CABLE ADDRESS "PROCTEC"

Sol-BPB

REVISION LEVEL B BOARDS ONLY

Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #5

Reference Section VI, Step 4, Page VI-8

On some Rev B boards, the blue and two white leads on the cable are too large for the mounting holes. To overcome this problem, prepare these three leads as follows:

1. Cut off end of white and blue wires, about 1/8" back into insulation.

2. Cut off as many strands of each wire as needs in order to insert through mounting hole.

CN#5A

PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080
CABLE ADDRESS "PROCTEC"

SOL-REG Revision Level B

Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #6-2

A problem was detected in early Sol-Reg regulator boards in which the "crowbar" circuit would trigger without adequate reason and short-circuit the 5-volt output. A circuit change was made which will be reflected on revision level C and above.

Refer to the three Engineering Change Orders numbered ECO 10017, ECO 10018, and ECO 10019.

Reference Section 2.7.2, step 10;

Following visual inspection carry out the trace cuts shown on ECO 10017.

Reference Section 2.7.2, step 14;

Install the following components as shown in ECO 10019:

( )	R13	330	orange-orange-brown
( )	R14	100	brown-black-brown
( )	C8	.047uf	disc ceramic capacitor

Reference Schematic, Regulator

Attach ECO 10018 to the schematic or insert the new components as indicated in this ECO.

CN #6-2

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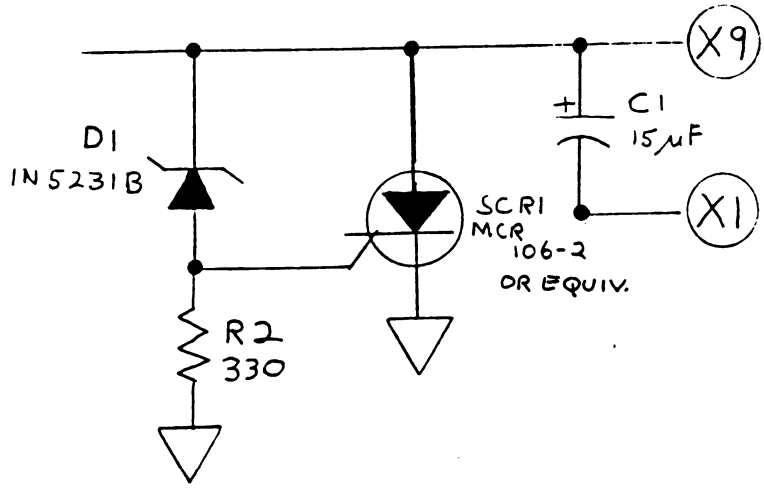
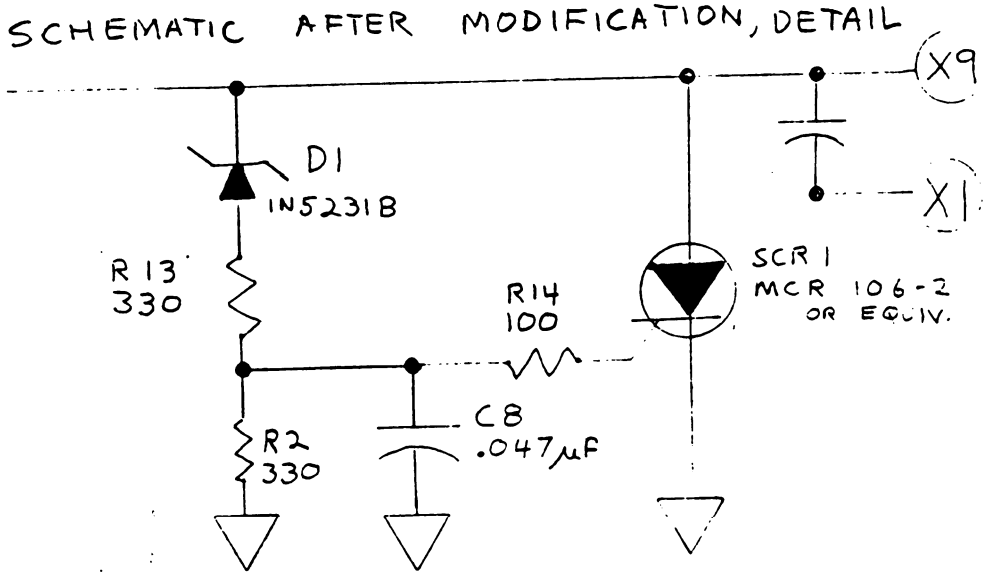
CABLE ADDRESS "PROCTEC"

ENGINEERING CHANGE ORDER



SCHEMATIC BEFORE MODIFICATION, DETAIL

SCHEMATIC AFTER MODIFICATION, DETAIL



REF. DES.	PART OR DWG. NO.	PART DESCRIPTION

NEXT ASSY.	USED ON
ECO 10017	105010

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

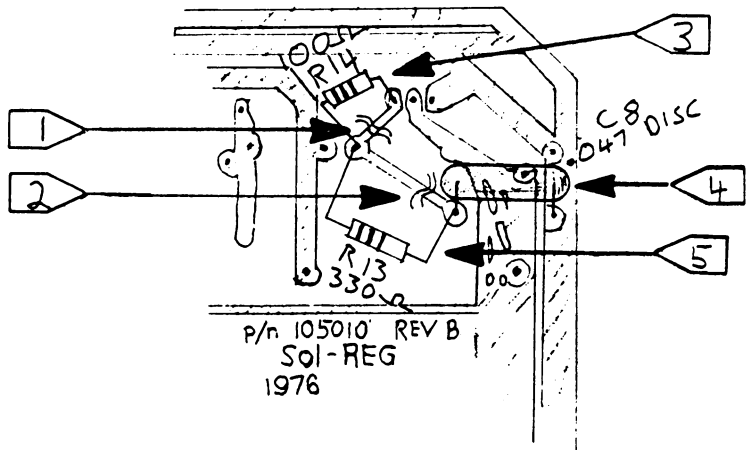
DRAWN: A. ATARIANI		ENGR: P. Mann	
DATE: 2/8/77		DATE: 2-1-77	
CHECKED: K. Jorgensen		RELEASED: P. Mann	
DATE: 2/9/77		DATE: 2-9-77	

MODIFICATION Schematic Sol Reg Crowbar

REF. DRAWING NO. 105009

REV.	E.C.O. DRAWING NO.	SCALE:	SIZE
B	10018	SHEET 1 OF 1	

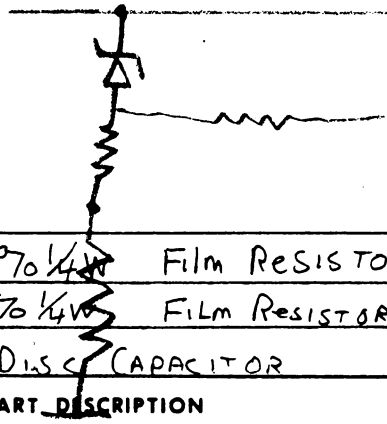
ENGINEERING CHANGE ORDER



BOTTOM VIEW
(Solder Side)

NOTES. UNLESS OTHERWISE SPECIFIED:

1) Cut trace connecting Anode of D1 with gate of SCR1.
2) Cut trace connecting R2 with D1.
3) Solder R14 (new) to pads of D1 anode & SCR1 gate.
4) Solder C8 (new) to pads of R2. (both ends).
5) Solder R13 (new) to pads of D1 (anode) & R2.



REF. DES.	PART OR DWG. NO.	PART DESCRIPTION		
R14	NEW	100Ω 5% 1/4W Film Resistor	1	
R13	NEW	330Ω 5% 1/4W Film Resistor	1	
C8	NEW	.047UF Disc Capacitor	1	

NEXT ASSY.	USED ON
ECO 10018	105009

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

DRAWN: A ATTARIAN II		ENGR: R. Mann	
DATE: 2/9/77		DATE: 2-10-77	
CHECKED: K. Jorgensen		RELEASED: R. Mann	
DATE: 2/9/77		DATE: 2-10-77	

MODIFICATION, PC BOARD, Sol Reg, Crowbar

REF. DRAWING NO. 100510

REV.	E.C.O. DRAWING NO.	SCALE:	SIZE
B	10017	—	
		SHEET 1 OF 1	

Processor Technology

The first few pages of this section of the Sol manual are revisions to other pages already in the manual. Please note the correct section and page that they refer to, and replace the appropriate page or pages as necessary. New pages are easily identified by the "Rev A" in the lower lefthand corner of the page.

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Sol-BPB REVISION LEVEL BOARDS

Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #5

Reference Section VI, Step 4, Page 5

When attaching the cable to the Sol-BPB, insert wires from solder (back) side of board and solder on component (front) side.

NOTE

Pad orientations given in Step 4 are as viewed from component side of board.

The blue and two white leads on the cable are too large for the mounting holes. To overcome this problem, prepare these three leads as follows:

1. Cut off end of white and blue wires, about 1/8" back into insulation.

2. Cut off as many strands of each wire as needed in order to insert through mounting hole.

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CABLE ADDRESS "PROCTEC"

Processor Technology

Sol MANUAL ERRATA SHEET #1

Reference Drawing No. 101007 in Section X (Page X-8)

The plastic tapped insert on the top edge of the left-hand masonite piece is incorrectly shown installed in the second hole from the back edge. This insert should be installed in the third hole from the back edge.

The second insert on the bottom edge is also shown incorrectly installed in the hole to the left of the center large hole. Install this insert in the hole to the immediate right of the large center hole.

ES #1

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CABLE ADDRESS "PROCTEC"

Sol-KBD MODIFICATIONS MOD 1

Applies to Revision Level A Boards
(Revision level not included on silk screen)

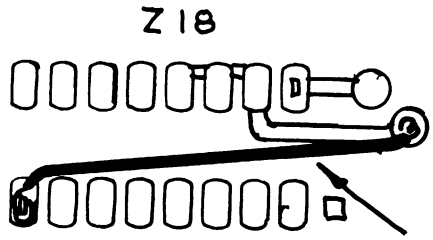
Processor Technology

Three layout errors exist on the Sol-KBD PC board you received. These errors must be corrected before you check the circuit board and start assembly. How these errors are corrected are described below:

1. Key Pad #55

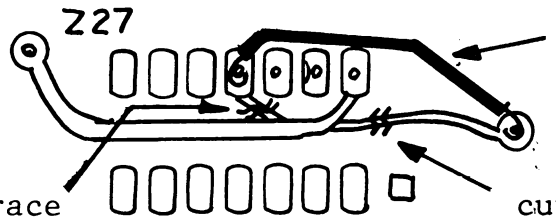
Using a sharp point, cut the bridge between the pad at 55 and the trace above (solder side).

2. U18, Pin 8



After installation of socket at U18 (Z18 on etch), install jumper wire from pin 8 to ground trace as shown. (Solder side.)

3. U27, Pin 11



After installation of socket at U27 (Z27 on etch) install jumper wire from pin 11 to pad as shown (solder side).

CN #3

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CABLE ADDRESS "PROCTEC"