# IBM SYSTEM/360 Model 44

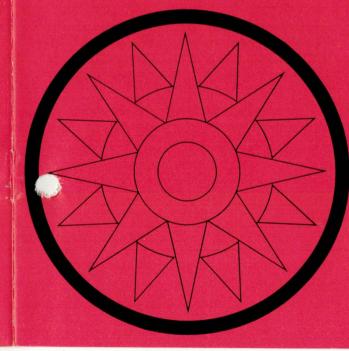
# **IBM**

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#### INSTRUCTION SET

The Model 44 executes the following instructions:

Instruction				
	Format	Format	Format	Format
Add	AR	A	_	- 1
Add Halfword	_	AH	_	- 11d
Add Logical	ALR	AL	_	_
AND	NR	N	_	NI
Branch and Link	BALR	BAL	-	_
Branch on Condition	BCR	BC	_	_
Branch on Count	BCTR	BCT	_	_
Compare	CR	C	_	_
Compare Halfword	_	CH	_	_
Compare Logical	CLR	CL	-	CLI
Divide	DR	D	_	_
Exclusive OR	XR	X	_	XI
Halt I/O	_	_	_	HIO
Insert Character	_	IC	_	_
Load	LR	L	_	_
Load Address	_	LA		
Load and Test	LTR	_	_	_
Load Complement	LCR	_	_	_
Load Halfword	Lak	LH	_	_
Load Negative	LNR	_	_	
Load Positive	LPR			
Load PSW	LIK			LPSW
Move				MVI
Multiply	MR	M		IVIVI
Multiply Halfword	WIK	MH		
OR	OR	O		OI
	SPM	_		OI
Set Program Mask Set System Mask	SPM -			SSM
Shift Left Double	_	_	SLDA	33111
		_	SLDA	The state of
Shift Left Double			SLDL	
Logical		_	SLDL	
Shift Left Single Shift Left Single	_	_	SLA	1
Logical	_	_	SLL	_
Shift Right Double	_	_	SRDA	_
Shift Right Double				
Logical	_	_	SRDL	_
Shift Right Single	_	_	SRA	_
Shift Right Single				

#### Introduction

System/360 Model 44 is the member of the System/360 family, oriented specifically toward scientific applications. Within the framework of System/360 architecture, the Model 44 emphasizes fast parallel binary operations, and short-, long-, and variable-ingth precision arithmetic, with a wide range of input/output equipment. The Model 44 may be interconnected to System/360 Models 30-75 via their channel-to-channel adapter and to IBM 1800 Data Acquisition and Control Systems via its System/360 adapter. This design has produced a low-cost, high-performance system tailored to the application areas of general scientific computation, data acquisition, and data reduction.

## System Highlights

- 32-bit word plus parity bits.
- One-microsecond-per-word memory cycle speed.
- Full 32-bit-word parallel arithmetic and data paths.
- 8K, 16K, 32K, 64K word memory options.
- Integrated single disk storage drive.
- Scientific System/360 instruction subset of the universal instruction set.
- Extended Instruction Set capability.\*
- Short and long precision Floating-Point Arithmetic feature, including variable-length long precision.
- 16 general purpose registers standard, with optional high-speed implementation of these registers.
- High Resolution Timer.
- Low- and high-speed multiplexer channels.
   Direct Data Channel.
- Direct Word.
- Priority Interrupt.
- Wide range of I/O equipment.
- Store and fetch protection.
- Extensive Checking.
- Comprehensive scientific programming support.
- \*Available upon request through IBM Marketing Representatives.

- Multiple linear regression
- Polynomial regression
- Canonical correlation
- Factor analysis
- Discriminant analysis
- Time series analysis
- Data screening and analysis
- Random number generation (uniform, normal)

## In matrix manipulation:

- Inversions
- Eigenvalues and vectors
- Simultaneous linear algebraic equations
- Transposition
- Matrix arithmetic (addition, product, etc.)
- Partitioning
- Tabulation and sorting of rows or columns
- Elementary operations on rows or columns

#### In other mathematical areas:

- Integration of given or tabulated functions
- Integration of up to six first-order differential equations
- Fourier analysis of given or tabulated functions
- Bessel and modified Bessel function evaluation
- Gamma function evaluation
- Legendre function evaluation
- Elliptic, exponential, sine, cosine, Fresnel integrals
- Finding real roots of a given function
- Finding real and complex roots of real polynomial equations
- Polynomial arithmetic (addition, division, etc.)
- Polynomial evaluation, integration, differentiation

#### PROCESSOR UNIT

The design of the processor unit is oriented toward the scientific user. The basic data unit is the 32-bit word. All arithmetic is binary. Processor storage is integrated with the processor unit.

# tegrated Single Disk Storage Drive

Utilizing a removable 2315 Single Disk Cartridge, a 292,800-word disk drive is integrated directly into the CPU, and is used both for system residence and for I/O. It has a transfer rate of 90,000 bytes per second with an average access time of 70 milliseconds. This forward-looking disk approach offers high performance at low cost. A second Single Disk Storage Drive is available as an optional feature.

## General Purpose Registers

The Model 44 employs 16 general purpose registers for use as index registers, base registers, accumulators for fixed-point arithmetic, and logical operations. General purpose registers 0-15 are either contained in nonaddressable storage or optionally implemented in Solid Logic Technology. This flexibility allows the user to choose his computing capability according to his specific needs. The SLT registers (250 nanoseconds circuitry) will offer faster program execution.

## Effective Addressing

An effective address is the sum of a 12-bit displacement field in the instruction, 24 bits of a general purpose register used as a base register, and 24 bits of a general purpose register used as an index register. This technique provides double indexing capability and facilitates relocation.

# igh Resolution Timer

This clock device periodically updates a location in main storage. It can be used for job accounting by measuring the duration of time for each job, for interrupt to prevent a runaway job from gaining control of the systems, for time recordings, and for polling a communication network on a regular basis. The timer has a 13 microsecond resolution.

statements to provide direct data organization in support of direct access storage devices.

- · Mixed-mode arithmetic.
- Ability to replace the H-FORMAT specification by enclosing quotation marks.
- The T-specification, permitting printed outpr to begin at any print position.
- P-scale factors in FORMAT statements.
- IMPLICIT statement allowing extended implicit classifications by first character of a name.
- An extended type statement, including length specification.
- G-conversion, extended to cover all numeric and logical data types.
- Multiple entry points to subprograms, and nonstandard returns from subroutines.
- Arrays of up to seven dimensions.
- Call by name for functions and arrays; call by value or name for other arguments.
- PAUSE statement extended to permit output of messages.
- NAMELIST statement permitting input/output and conversion without an explicit I/O list and FORMAT statement.

Variables and constants may be either fixed- or floating-point values in single or double precision. In addition to the capabilities of the FORTRAN IV language itself, there is a library of subroutines for performing common mathematical procedures such as finding square roots, trigonometic functions, logarithmic values, etc. The compiler recognizes the subroutine requirements and supplies automatically the linkages to the subroutine.

## PROGRAM COMPATIBILITY

Source programs written using the Assembler and FORTRAN languages provided in the Model 44 support are upward-compatible with the languages of Operating System/360.

The Trap and Simulate capability available for System/360 Models 44F, G, and H will permit the Model 44 user to have complete instruction set compatibility with System/360 Models 30-75.

oriented toward parallel binary operation, is provided. Basic byte manipulation capability is also retained.

## Extended Instruction Set Capability

The Model 44 utilizes a subset of the System/360 instruction set. With the Trap and Simulate capability, the system is able to accept the full System/360 instruction set. These additional instructions are simulated in nonaddressable 1-microsecond memory. This feature permits compatibility between System/360 Models 30-75 and the Model 44, provided that the configurations are comparable and programs are not time-dependent.

#### PROCESSOR STORAGE

Cycle time: 1 microsecond

Width: One word (32 data plus 4 parity bits)

Sizes:

Bytes
32,768
65,536
131,072
262,144

## Addressing

Byte locations in storage are consecutively addressed (24-bit binary addresses) starting with 0. The maximum valid effective address depends upon the particular size of the main storage unit. Any attempt to address main storage with an address greater than the particular maximum results in a program error interruption.

## Checking

All transfers are checked by the parity bit assigned each eight-bit byte. Should an error occur in an anput/output device, communication channel, or memory, an interrupt takes place and information pertinent to the error is recorded.

#### **CHANNELS**

## Overlap Operation

Data flows concurrently between processor storage and channel devices while CPU processing continues.

## 1856 Analog Output Terminal

Provides controls, power supply, and housing for digital-to-analog converters and their associated precision voltage references. DAC's provide conversion of either 10-bit or 13-bit digital values to an analog signal for use in operating strip chart recorders, oscilloscopes, or as input to hybrid systems. A capabilit of up to 128 analog output points can be housed in combinations of the Model 1 and 2 1828 enclosures.

#### COMMUNICATIONS

## 2701 Data Adapter Unit

- Provides for attachment of remote and local I/O devices operating through various customer or common-carrier facilities.
- Provides for attachment of 4 communication lines or up to two synchronous communication lines.

#### 2702 Transmission Control

 Provides for attachment of up to 15 half-duplex communication lines.

#### DISPLAY UNITS

## 2250 Display Unit

- Displays up to 3848 characters—52 lines each, with 72 alphameric characters.
- · Keyboard input.
- Point/vector plots.
- Model 1 includes its own control unit.
- Model 2 requires 2840 Display Control.

# 2260 Display Station (requires 2848 Display Control)

- Displays from 240 to 960 characters.
- Displays 36 alphamerics, 25 special characters.
- · Keyboard input.

## **Programming Systems**

Programming support of the new IBM System/360 Model 44 will be provided in two categories:

# SYSTEM/360 MODEL 44 BASIC PROGRAMMING SUPPORT (44 BPS)

This interim support consists of three independent programs for card and tape configurations. The pro-

parts of core storage from being destroyed by overwriting or unpredictable programming errors.

## Input/Output Devices

Model 44 can accommodate an extremely broad selection of I/O devices. It incorporates a standard uterface concept that provides a data format and a gnal sequence common to System/360 I/O devices. The following devices may be used with, or added to, the Model 44:

## CONSOLE PRINTER-KEYBOARD (standard)

• Print speed 14.8 cps.

#### READER-PUNCHES

#### 1442 Card Read Punch

- Model N1 and N2: Reads 400 cards/minute.
- Punches 160 columns/second.

#### 2501 Card Reader

 Model B1, B2: Reads 80-column cards 600 to 1000/minute.

#### 2520 Card Read Punch

- Model B1: Reads and punches 500 cards/minute.
- Model B2: Punches 500 cards/minute.
- Model B3: Punches 300 cards/minute.

## 2540 Card Read Punch

- Reads 1000 cards/minute.
- Punches 300 cards/minute.

## PRINTERS

## 1403 Printer

- Model 2: Prints 600 lines/minute—
   132 print positions.
- Model 3: Prints 1100 lines/minute— 132 print positions.
- Model 7: Prints 600 lines/minute— 120 print positions.
- Model N1: Prints 1100 lines/minute— 132 print positions.

# 1443 Printer

 Model N1: Prints up to 240 lines/minute up to 120 print positions.

#### MAGNETIC TAPES

## 2401 Magnetic Tape Unit

Single tape drive.

## 2402 Magnetic Tape Unit

 Two independently operating drives in a single unit.

## 2403 Magnetic Tape Unit and Control

 A single-channel, read or write tape control and one tape drive.

## 2404 Magnetic Tape Unit and Control

- A two-channel, simultaneous read-while-write tape control, and one tape drive.
- The following characteristics apply to the 2401, 2402, 2403, and the 2404.

800 bpi	Model 1	Model 2	Model 3	
Bytes/second	30,000	60,000	90,000	
Density (bytes/inch)	800	800	800	
Tape Speed (inches/second)	37.5	75.0	112.5	
Nominal Interrecord Gap (inches)	.6	.6	.6	
Nominal IRG Time (milliseconds)	16.0	8.0	5.3	
Rewind Time (minutes)—incldg reload	3.0	1.4	1.0	
Rewind and Unload	2.2	1.5	1.1	
1600 bpi	Model 4	Model 5	Model 6	
Bytes / second	60,00	120,000	180,000	
Density (bytes/inch)	1,600	1,600	1,600	
Tape Speed (inches/second)	37.5	75.0	112.5	
Nominal Interrecord Gap (inches)	.6	.6	.6	
Nominal IRG Time (milliseconds)	16.0	8.0	5.3	
Rewind Time (minutes)—incldg reload Rewind and Unload	3.0	1.4	1.0	

#### DIRECT ACCESS STORAGE DEVICES

Single Disk Storage Drive (First Standard)

- Utilizes removable 2315 Single Disk Cartridge.
- Cartridge capacity 292,800 words.
- Average access time, 70 milliseconds.
- Transfer rate, 90,000 bytes per second.

## 2311 Disk Storage Drive

- Utilizes removable 1316 Disk Cartridge.
- Cartridge capacity, 7.25 million bytes.
- Average access time, 85 milliseconds.
- Transfer rate, 156,000 bytes per second.

#### PAPER TAPE

## 2671 Paper Tape Reader

- Reads 5-, 6-, 7- or 8-track tape.
- Reads up to 1000 cps.

## DATA ACQUISITION

1826 Data Adapter Unit

For expansion of digital input features and digital output features on the 1827 Data Control Unit. Also permits the attachment of an alternate analog-to-digital converter. Will accommodate up to 576 digital rocess termination points.

Model 1 is a free-standing unit, externally cabled, which may be located up to 100 feet from the 1827.

Model 2 is directly attached and internally cabled.

#### 1827 Data Control Unit

A modular unit which extends the capabilities of a System/360 to handle a broad range of control applications from high-speed data acquisition to supervisory control of industrial processes.

Accommodates basic features which permit the attachment of an analog-to-digital converter, relay analog input multiplexing (up to 1024 points), solid-state analog input multiplexing (up to 256 points), hardware limit checking for analog inputs, analog input terminals including matching and filtering components, high-speed analog outputs (digital-to-analog converters, up to 128 points), digital input up to 1024 bits, high-speed pulse counters (up to 128), latching or pulse outputs (up to 2048), digital register output (up to 2048 bits).

The 1827 provides for up to five addresses which are allocated to available subchannels. With either a standard or high-speed multiplexer channel, concurrent device operation is permitted, provided each device has a separate subchannel.

## 1851 Multiplexer Terminal

Provides termination for analog input signals and mounting for multiplexer groups, signal conditioning dements, and time-shared amplifiers.

Model 1—a standard terminal for all non-thermocouple analog input signals—can terminate up to 64 differential inputs.

Model 2—thermocouple terminal for both thermocouple and non-thermocouples input signals—can terminate up to 62 inputs. Up to six 1851s can be mounted in one 1828 Model 2 enclosure.

Storage accesses to service I/O devices (depending on I/O requirements) produce minimal interference with CPU operations.

## Standard Interface

Data format and channel control functions are standard System/360.

#### Channel Characteristics

Two types of channels are provided with the Model 44. One channel of either type is required.

## Multiplexer

To service low-speed devices, one per system is provided to accommodate:

- Up to 64 subchannels.
- One to eight control units per channel.
- 50,000 bytes per second, interleaved data rate.
- 200,000 bytes per second, burst data rate.

# High-Speed Multiplexer Option

For higher-speed devices, up to two per system are provided to accommodate:

- One to four subchannels per channel.
- Two control units per subchannel.
- Up to 16 devices per control unit.
- 200,000 bytes per second, interleaved data rate per channel.
- 500,000 bytes per second, burst rate for onechannel operation.
- 800,000 bytes per second, total burst rate for two-channel operations.

## Direct Data Channel

Provides a half duplex 32-bits wide data path between a foreign device and main processor storag Up to eight external devices can be attached.

## Direct Word

Provides for the transfer of 32 bits (full word) of information between an external device and main processor storage on a per-instruction basis.

## Store and Fetch Protection

Provides read/write protection and protects selected

grams included with Model 44 Basic Programming Support are:

- Card Assembler—a card assembly system which employs Model 44 Instruction Set mnemonics and pseudo instructions.
- Card Utilities—a package of utility programs that provide device-to-device capabilities for the supported devices.
- Tape FORTRAN—language compiler—compatible with and encompassing the proposed ASA Basic FORTRAN. It requires three tape drives for compilation, with a fourth tape drive necessary for Load and Go compatibility. The compiler requires the Floating-Point Option for both compilation and execution.
- Device-supporting programs—for 1442 and 2540 Card Read Punch, 1403 and 1443 Printer.
   All 2400 series magnetic tape units are supported excepting those recorded at 1600-bytesper-inch density.

## SYSTEM/360 MODEL 44 PROGRAMMING SYSTEM (44 PS)

Model 44 Programming System is designed for residence on one single disk storage drive, which is standard on 2044, and requires the 2315 Disk Cartridge.

Disk-Resident Monitor with I/O Capabilities—a batch-processing monitor with I/O capabilities, interrupt-handling facilities with exits for user's options, and utility programs. All customer and IBM processing programs can utilize the functions provided by the 44 PS Monitor.

Disk-Resident Assembler—permits the use of Model 44 Instruction Set Mnemonics, including instructions rovided by the announced features, pseudo instructions, and literals.

Disk-Resident FORTRAN IV (44 PS)—compatible with and encompassing the proposed ASA FORTRAN language. It will accept programs written in DOS/360 and TOS/360 FORTRAN and OS/360 FORTRAN and will provide:

- Double-precision arithmetic.
- Compatible extensions to READ and WRITE

## Interrupt System

The powerful System/360 interrupt system provides for quick and efficient handling of the following classes of interruption:

- Machine Checks
- Program Interrupt
- Supervisor Call
- External Interrupt
- Input/Output

# Priority Interrupt

Provides for quick response to external conditions and provides 32 independent levels of priority interrupt. Has 256 uniquely identifiable interrupts per main level, for a total capability of 8,192 lines.

# Floating-Point Registers

Four floating-point registers, each 64 bits in length, are provided. The first 32 bits of each register are implemented in Solid Logic Technology, and the low-order 32 bits are implemented in nonaddressable storage.

## Arithmetic

#### Fixed-Point

Fixed-point binary operations are performed in any general purpose register, using fullword or halfword data.

## Floating Point

Floating-point operations are performed in any floating-point register.

- Range:  $10^{-78}$  to 10 + 75
- Precision:

Short word > 6 + decimal digits Long word > 15 + decimal digits

# Variable-Length Long Precision Floating-Point

In addition to the above two ranges of precisic arithmetic, the Model 44 has a variable-length floating-point feature. This feature allows the user to suppress arithmetic operation on low-order bytes of the long precision fraction. This ability permits faster instruction execution at shorter fractional lengths.

## Scientific Instruction Set

A subset of the System/360 universal instruction set,

## MODEL 44 PROGRAMMING SUPPORT MONITOR AND INPUT/OUTPUT FACILITIES

Units Supported	Residence*	Reader	Input	Output	List	Operator Communication
Console Printer-						
Keyboard					**	X
1403-2, 3, 7, N1		**	**	**	X	
1442 N1		X	X	X		
1442 N2				X		
1443 N1					X	
2501 B1, B2		X	X			
2520 B1		X	X	X		
2520 B2, B3				X		
2540		X	X	X		
2311			X	X		
2400		X	X	X	X	
Single Disk						
Storage Drive	X		X	X		
Second Single Disk						
Storage Drive	X		X	X		
O .						

<sup>\*</sup>System Residence can only be on one storage drive.

## **Application Support**

The Scientific Subroutine package is a collection of over 130 FORTRAN subroutines divided into three groups: statistics, matrix manipulation, and mathematics. They are a collection of input/output-free, computational building blocks that can be combined with a user's input, output or computational routines to meet his individual needs. The package can applied to the solution of many problems in industry, science, and engineering.

Individual subroutines, or a combination of them, can be used to carry out the following functions:

#### In statistics:

- Analysis of variance (factorial design)
- Correlation analysis

#### **General Characteristics**

The Model 44 utilizes the same advanced Solid Logic Technology circuitry as the other models of System/ 360. The miniaturized circuit modules result in:

- Faster circuitry because of high-density packaging.
- Lower cost and greater design flexibility, made possible by simplified batch-fabrication processes.
- 3. Less maintenance because of ruggedized components.
- 4. Easier maintainability because of increased checking.
- 5. Improved physical access to circuit elements.

Automated testing allows components to be thoroughly checked in a comprehensive quality control program. The result is a degree of reliability not previously available in data processing systems.

## DATA AND INSTRUCTION FORMAT

#### Data

CPU register, arithmetic operations, and storage data paths are word-oriented. A word is 36 bits wide; 32 bits represent the data field and 4 bits indicate parity (one parity bit for each 8 bits of the data field). Halfword (16 data bits, 2 parity bits) and byte (8 data bits, 1 parity bit) operations are provided to augment the scope and power of the instruction set. Floating-point operands are short precision (32-bit word, 4 parity bits), or long precision (64-bit doubleword, 8 parity bits). The first 8 bits contain the sign and the hexadecimal characteristic The remaining 24 or 56 bits contain the hexadecimal fraction.

### Instruction

All instructions occupy either a word or a halfword. Approximately half of the instruction set does not reference processor storage, thus providing high-performance operations.

## Appendix

# COMPONENTS FOR MODEL 44

Console Printer-Keyboard (Standard) Reader-Punches

- 1442-N1, N2 Card Read Punch
- 2501-B1, B2 Card Reader
  - 2520-B1, B2, B3, Card Read Punch
  - 2540 Card Read Punch

#### Printers

- 1403-2, 3, 7, N1 Printer
- 1443-N1 Printer
- 1416 Interchangeable Train Cartridge (for 1403-3 and N1)

# Magnetic Tapes

- 2401-1, 2, 3 Magnetic Tape Unit
- 2402-1, 2, 3 Magnetic Tape Unit
- 2403-1, 2, 3, 4, 5, 6 Magnetic Tape Unit and Control
- 2404-1, 2, 3 Magnetic Tape Unit and Control

## Direct Access Storage Devices

- Single Disk Storage Drive (First Standard)
- 2311 Disk Storage Drive

## Paper Tape

2671-1 Paper Tape Reader

## Data Acquisition

- 1826-1, 2 Data Adapter Unit
- 1827-1 Data Control Unit
- 1851-1, 2 Multiplexer Terminal
- 1856 Analog Output Terminal

## Communications

- 2701 Data Adapter Unit
- 2702 Transmission Control

## Graphics

- 2250-1, 2 Display Unit
- 2260-1 Display Station

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RR Forma	RX at Forma	RS at Forma	SI at Format
_	_	_	SIO
_	ST	_	_
_	STC	_	_
_	STH	_	_
SR	S	_	
_	SH	_	_
SLR	SL	_	_
SVC	_	_	_
_	_	_	TS
_	_	_	TCH
_		_	TIO
_	_	_	TM
	Forma	Format Forma  -	Format Format Format  -

An optional feature provides the full complement of floating-point instructions for both long and short operands and the RR and RX formats:

Instruction	RRF	ormat	RX Format	
	Long	Short	Long	Short
Add Normalized	ADR	AER	AD	AE
Add Unnormalized	AWR	AUR	AW	AU
Compare	CDR	CER	CD	CE
Divide	DDR	DER	DD	DE
Halve	HDR	HER	_	_
Load	LDR	LER	LD	LE
Load and Test	LTDR	LTER	_	-
Load Complement	LCDR	LCER	_	_
Load Negative	LNDR	LNER	_	_
Load Positive	LPDR	LPER	_	-
Multiply	MDR	MER	MD	ME
Store	_	_	STD	STE
Subtract Normalized	SDR	SER	SD	SE
Unnormalized	SWR	SUR	SW	SU