μ-COMP DDP-516 General Purpose I/C Digital Computer

Honeywell

COMPUTER CONTROL
DIVISION

FEATURES

All silicon monolithic integrated circuits; proven production capability

- Fully parallel machine organization
- 16-bit word, two's complement
- Two full-word arithmetic registers
- 0.96 μsec memory cycle time
- 4096 μ-STORE ICM-40 magnetic core memory
- Memory expansion to 32,768 words; 16,384 in standard cabinet
- Hardware index register
- Multi-level indirect addressing; pre- or post-indexing
- Large sector size for maximum memory efficiency
- Direct addressing of full memory with desectorizing software
- Simple command format; comprehensive instruction repertoire
- Most instructions executed in 1.92 μsecs or less
- Commands include 3-way compare, increment memory and skip, interchange memory and accumulator
- Powerful set of shift commands; extensive skip-branch conditions
- Byte manipulation commands
- 5.28 μsec multiply
- Hardware double precision capability
- Memory lockout option for program protection
- Memory parity option
- Real-time clock option
- I/O designed for real-time systems interface
- Priority interrupt standard
- Power failure interrupt standard
- Individually buffered I/O devices
- Two-cycle I/O commands select device, test status, and transfer data
- No I/O hold-off
- Flexible priority scheme with program settable masks
- DMC option for economical time-shared I/O
- Direct memory access option for mc I/O rates
- ASR-33 or ASR-35 option
- Program compatible with DDP-116
- Software package field-proven in over 100 installations
- Selectable one- or two-pass assembler
- Desectorizing loader
- Bootstrap loader protected in read-only memory
- Fixed and floating point subroutine library
- Real-time monitor program (RTM)
- ASA FORTRAN IV
- Compact mechanical packaging
- Movable control console
- Front access for ease of maintenance
- Modular plug-in options for easy expansion
- Full line of compatible I/C modules and accessories available for systems designer
- First delivery: September '66
- Price: upon request
- Liberal OEM terms available

INTRODUCTION

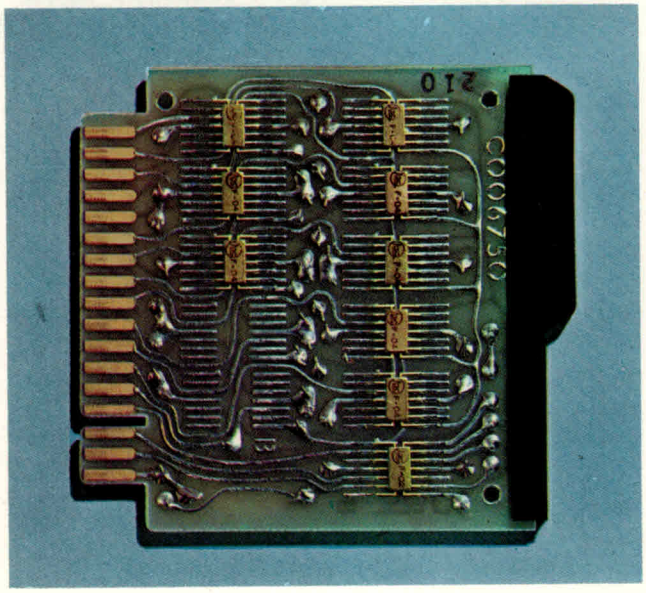
A new 16-bit I/C general purpose computer

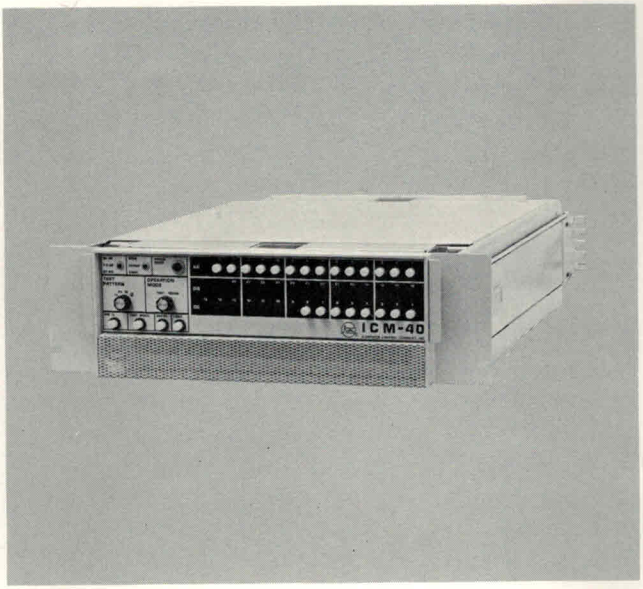
The μ-COMP DDP-516 is a third generation general purpose digital computer — a natural product of 3C's complete digital systems capability . . . a new computer system at once new in terms of speed, high-performance I/C hardware and reliability, yet with immediately deliverable field proven software.

The DDP-516 customer receives a system backed by a dozen successful years in the digital electronics industry, by programming and maintenance courses conducted by 3C experts, by a continuous exchange of information and ideas as a member of our computer users' group and by the resources, integrity and continuing support of Honeywell.

BACKGROUND

From the house that built the first 16-bit compact and the first commercial I/C computer





Computer Control has, for more than twelve years, set the pace in the digital computer/digital systems industry as a leading manufacturer of digital modules, core memories, and general purpose computers. 3C was among the first to recognize integrated circuit technology as the key to future growth: the first to offer a complete I/C digital logic line after two years of in-house funded research and development. And the first to offer a commercial I/C computer. This technological strength, coupled with 3C's 16-bit hardware and software development experience and Honeywell corporate resources, gives the μ-COMP DDP-516 user more computer for the money than any other machine on the market.

μ-PAC I/C Digital Logic Modules — As a result of in-house Advanced Techniques Laboratory research, 3C has attained a position of leadership in the design, development, and application of silicon monolithic integrated circuits. High reliability, low cost per logic function, and ease of maintenance are proven features built into the DDP-516 with μ-PACS.

3C has drawn on more than twelve years of reliability experience with digital logic modules to develop the μ-COMP DDP-516. Computer design engineers contribute strongly in defining logical capability and configuration parameters for μ-PACS. To achieve optimum system reliability, extensive consideration is given to circuit design approaches, component values and tolerances, margins, heat transfer, and performance specifications. DDP-516 MTBF: over 4000 hours normal operation.

Inherent advantages contributing to μ-PAC reliability over discrete component circuits are:

1. Greatly reduced number of thermal compression bonds required on a typical digital integrated circuit.
2. Fewer component interconnections.
3. Fewer sealed packages per circuit.
4. Less variation between individual integrated circuits.
5. Easier detection of defective circuits.

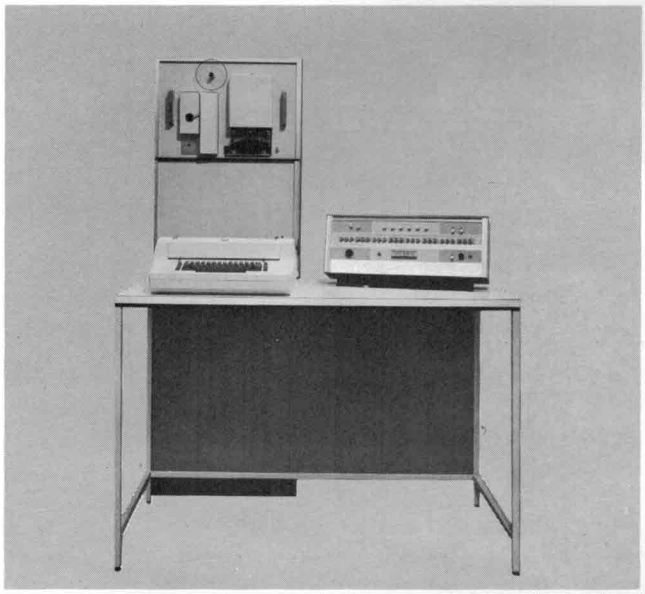
All hybrid circuits used in the DDP-516 are standard μ-PAC modules which employ high quality, high stability discrete components. All semiconductor components are silicon.

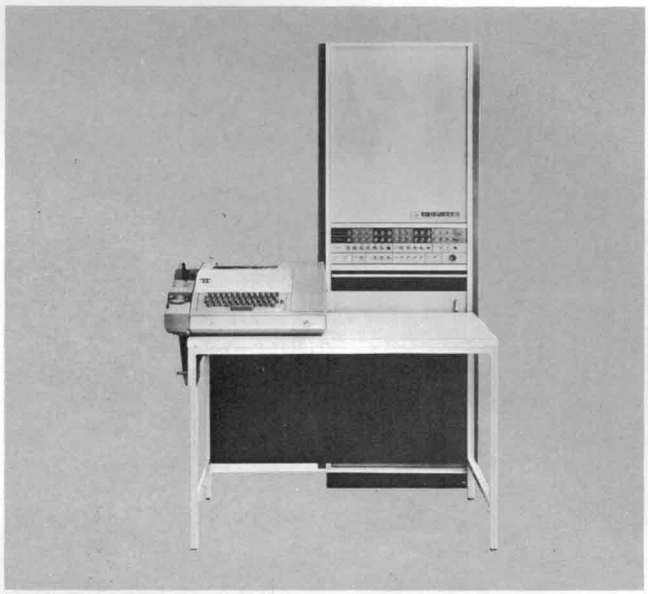
In addition to circuit reliability, the μ-COMP DDP-516 is engineered for highly reliable operation. Parallel machine organization permits use of moderate speed circuitry and wide performance margins.

Rigid inspection, test, and over all quality assurance programs are an integral part of both the μ-PAC and DDP-516 manufacturing processes.

μ-STORE ICM-40 Core Memory — The μ-STORE ICM-40 I/C Core Memory system is the heart of the DDP-516. This compact, high speed system has been field-proven in a variety of installations including the DDP-124 I/C general purpose computer. μ-PAC I/C modules are used throughout. In addition to using this memory in its I/C computers, 3C markets the ICM-40 as a standard product.

DDP-124 — Introduced in 1965, the μ-COMP DDP-124 general purpose computer was the first truly





I/C computer. The experience gained with this widely used 24-bit computer provides a demonstrated capability in installation and maintenance of I/C systems in a variety of applications, as well as advanced packaging concepts and ready production facilities.

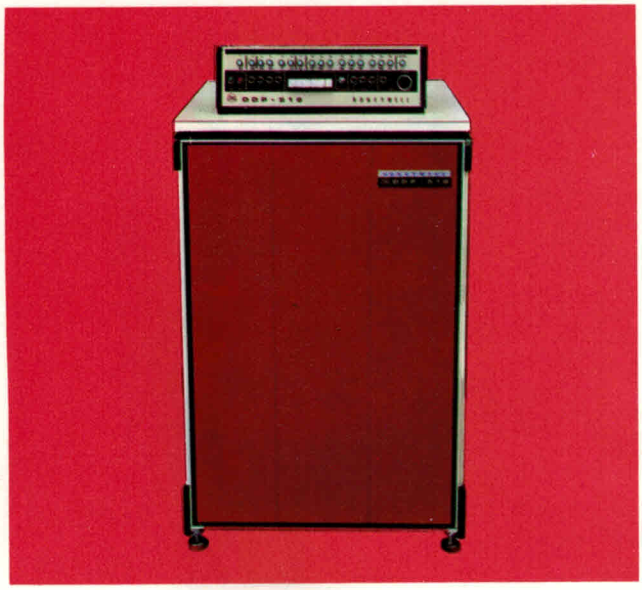
The DDP-516 uses the same general physical configuration as the DDP-124 — automatically wired back planes mounted vertically in a swing-out drawer for front access to both PACS and wiring, built-in cooling fans, cable PAC connectors for easy interface and expansion, the same μ-PAC logic and the same ICM-40 type memory. Proven production capabilities insure quick delivery and reliable performance of the DDP-516.

DDP-116 — 3C demonstrated its leadership in the compact computer market by designing the first 16-bit real-time computer . . . the DDP-116. First to be announced, first to be delivered, the DDP-116 has gained a wealth of operating experience in well over 100 installations in industry, in the military, in research, and in numerous other real-time environments. Bugs have long since been shaken out of the software. Applications and user organization (CAP) software libraries continue to grow. Quality control procedures have been implemented to insure that users receive reliable, accurate software packages for their configuration. Reliable operation of both hardware and software is a proven fact.

DDP-516 is program compatible with DDP-116, thus 516 software is checked out and deliverable today — no waiting, no field test. Plus, you get immediate access to an established users' group library.

GENERAL DESCRIPTION

Designed for real-time on-line applications



μ-COMP DDP-516 is a compact, low cost, high performance 16-bit binary general purpose digital computer. Standard memory capacity is 4096 words (expandable to 32,768) with 0.96 μsec cycle time. Extremely high computation and I/O speeds make the DDP-516 ideal in real-time on-line systems applications.

Modular design, flexible I/O structure and powerful command repertoire enable the DDP-516 to meet a broad variety of applications wherever real-time performance characteristics are the major criteria.

General characteristics include fully parallel organization, indexing, multi-level indirect addressing, powerful I/O system, comprehensive 72-command instruction repertoire, and straightforward logic for easy system interface and field expansion. Selected optional capabilities are designed with plug-in modularity to permit custom tailoring at minimum expense.

Desectorizing, an important software feature, allows the programmer to directly address all of core memory without considering sector boundaries. Standard DDP-516 hardware provides direct addressing to 1024 words of core memory with a single command. This capability is extended by desectorizing software which generates indirect address linkages when it is necessary to cross sector boundaries. Redundant linkages are never generated. Thus, a program written in assembly language will, in general, be more efficient than a program written by a programmer who must be concerned with indirect address linkages.

The DDP-516 software package includes such DDP-116 proven programs as utility routines, arithmetic subroutine library, I/O library, and COP (DDP-516 debugging aid). DAP-16 (DDP-516 assembly program), is unique in that it allows the operator to specify a one- or two-pass assembly for the same source program; one-pass being preferable for the basic system, two-pass for systems with high speed input devices where more detailed listings are desired. The one- and two-pass options both allow the programmer to directly address all of memory in his source program through the use of desectorizing software.

FORTRAN is DDP-116 proven ASA FORTRAN IV, immediately deliverable for systems with 8K memory. These programs can be run concurrently with real-time operations under control of RTM, the DDP-516 Real-Time Monitor. This program, in conjunction with the memory lockout option, allows real-time processes to be protected from undebugged off-line programs while operating under interrupt control.

The DDP-516 features compact mechanical packaging — fits into standard rack width cabinet, stands 38 inches high from floor to table top. Movable control console is designed to allow complete operator freedom. Three vertical leaves house the system power supply, central processor (with ample space for optional additions) and 3C μ-STORE ICM-40 core memory (with space for up to 16,384 words). The entire mainframe can be rack mounted in less than 36 inches of vertical rack space for implementation into complex systems configurations. Tilt-out construction provides front access to both modules and interwiring.

SPECIFICATIONS

Engineered for maximum performance at lowest cost

Type

16-bit parallel binary
Two's complement arithmetic
Coincident-current random-access ferrite core memory, 4K to 32K
Single address with multi-level indirect addressing and indexing

Speed

Memory cycle time	0.96 μsec
Add	1.92 μsec
Subtract	1.92 μsec
Multiply	5.28 μsec*
Divide	10.56 μsec*
Double precision add	2.88 μsec*
Single word I/O transfer	1.92 μsec

Time multiplex I/O transfer: 260 kc with DMC*
Over 1 mc with DMA*

Power

1 kw at 115 vac ±10%, 60 ±2 cps single phase
Power failure interrupt is standard feature

Weight

250 lbs.

Temperature

0° to 45°C (32° to 113°F)
(Central processor less any I/O devices)

Dimensions (without console)

24″ x 24″ x 38″

Cooling

Filtered, forced air cooling provided within central processor cabinet

Signal Levels

Logic ZERO: 0 V dc
Logic ONE: +6 V dc

Standard Input/Output Lines

10-bit address bus
16-bit input bus
16-bit output bus
Priority interrupt
External control and sense lines

I/O Teletype Unit (ASR-33 or ASR-35)

Print	10 cps
Keyboard input	10 cps
Read paper tape	10 cps
Punch paper tape	10 cps

Off-line paper tape reproduction, preparation and listing

Central Processor Options

High speed arithmetic package (includes multiply, divide, normalize and double precision load, store, add and subtract)
Memory parity
Real-time clock
Memory lockout (includes sector zero relocation)

I/O Options

Additional priority interrupts
Direct multiplex control (DMC)
Direct memory access (DMA)
Parallel input or output channels
Parallel buffered I/O channels

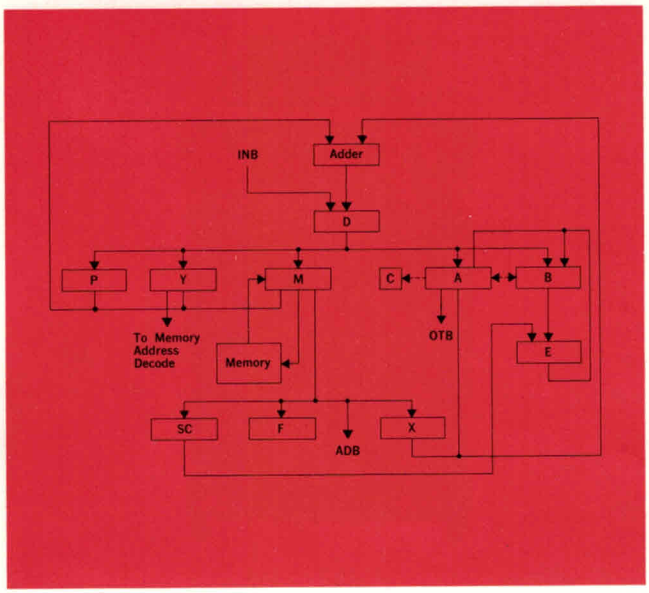
Peripheral Options

Magnetic tape transports — 36-80 ips
Mass storage system — 100K-600K words
Line printer — 120 col, 300 lpm
Paper tape reader — 300 cps
Paper tape punch — 110 cps
Card reader — 200 cpm

*With optional hardware

INTERNAL ORGANIZATION

Dual arithmetic register and flexible I/O



A Register (A) — The A register is a 16-bit register used as the primary arithmetic and logic register of the computer. The A register can be displayed and manually controlled on the computer control panel.

B Register (B) — The B register is a 16-bit secondary arithmetic register used with the A register to hold arithmetic operands which exceed one word in length. The B register can be displayed and manually controlled on the computer control panel.

Program Counter (P) — The program counter contains the location of the next instruction to be performed. Its content is incremented by one each time an instruction is performed and may be incremented additional times during the execution of certain commands. The P counter contains 16 bits, and can be manually controlled on the computer control panel.

Y Register (Y) — The Y register is a 16-bit memory address register. The Y register can be displayed and manually controlled on the computer control panel.

E Register (E) — The E register is a 16-bit register used when shifting the B register.

D Register (D) — The D register is a 16-bit register used as a distribution register.

Adder — Performs the basic arithmetic processes of addition and subtraction. It is also used as a transfer path.

F Register (F) — The F register is a four-bit register that contains the operation code.

Output Bus (OTB) — Output bus contains 16 lines that transmit data from the computer to an I/O device.

M Register (M) — The M register is a 16-bit memory information register. The M register can be displayed and manually controlled on the computer control panel.

Input Bus (INB) — Input bus contains 16 lines that transmit data from an I/O device to the computer.

Address Bus (ADB) — Address bus contains 10 lines that transmit address information to an I/O device. Bits 7-10 define the function to be performed by the I/O command. Bits 11-16 designate the I/O device to be used.

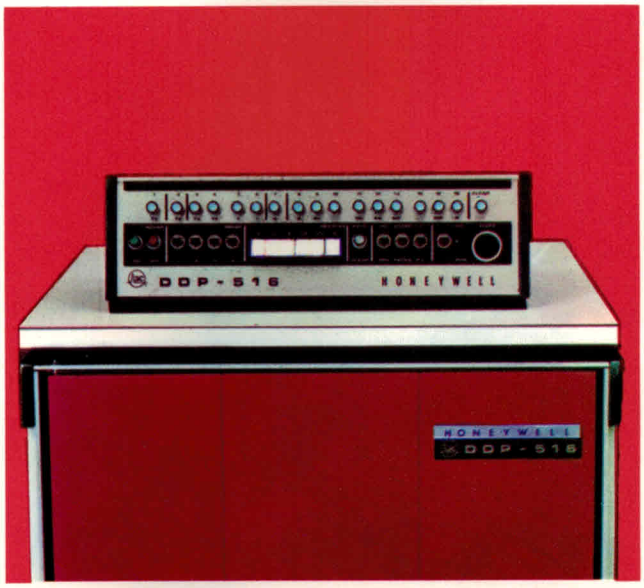
Shift Counter (SC) — The shift counter is a six-bit counter used to control the timing of certain instructions such as the shift and normalize instructions.

Index Register (X) — 16-bit register used for address modification. Any memory reference instruction that addresses location zero also accesses the X register.

C Bit (C) — Flip-flop used to indicate overflow on arithmetic instructions. Also used in shift instructions.

OPERATION

Flexible control with simplified communication



The DDP-516 console is cable-connected to the central computer and can be positioned anywhere on the top of the cabinet to suit operator convenience. Or it can be moved to an adjacent table if preferred.

μ-COMP DDP-516 is designed to provide high performance and simple, direct operation characteristics. Operator control specifications have been engineered for flexibility and are augmented by extensive information display. Built-in power failure protection and ease of maintenance are design features.

Control Console Functions — Standard remote console contains binary displays in octal representation, run status displays, and all operator controls. By depressing the appropriate select switch, the operator can display contents of the A register, B register, index register, program counter, and memory information register as well as internal counters and flip-flop status. Registers may be cleared and/or altered from the console and memory locations can be displayed or written into. (Memory locations 1-15 can be loaded manually only, and contain program load instructions.)

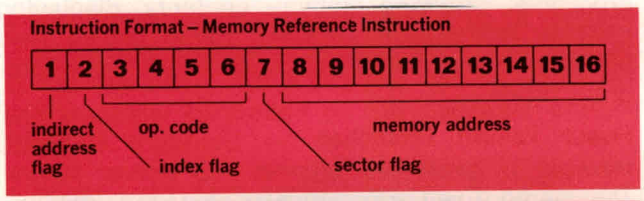
Console control functions include selection of operation mode, memory accesses, single instruction, continuous run, four sense switches for control of programs, and a power failure interrupt inhibit switch.

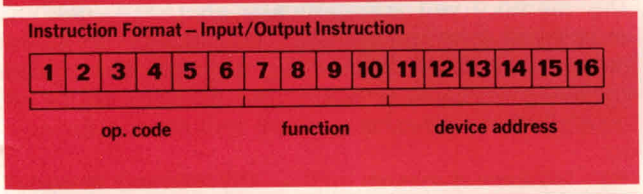
In addition to the console control, the DDP-516 utilizes a teletype keyboard unit with paper tape reader and punch. Either a Model ASR-33 or ASR-35 is offered. When used in conjunction with software checkout functions, this I/O medium becomes the primary control for breakpointing programs, changing memory contents, displaying memory, and related functions. It may also be used off-line for preparation, duplication, or listing program tapes.

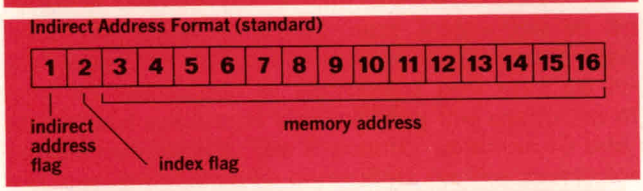
Power Failure Protection — Standard DDP-516 memory is protected against AC power failure. The memory will automatically shut down without destroying information. Also, an interrupt on power failure will occur permitting storage of register contents in memory before the memory shuts off.

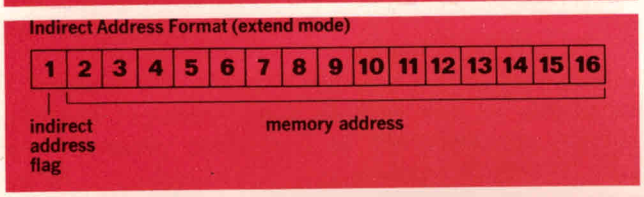
WORD FORMATS

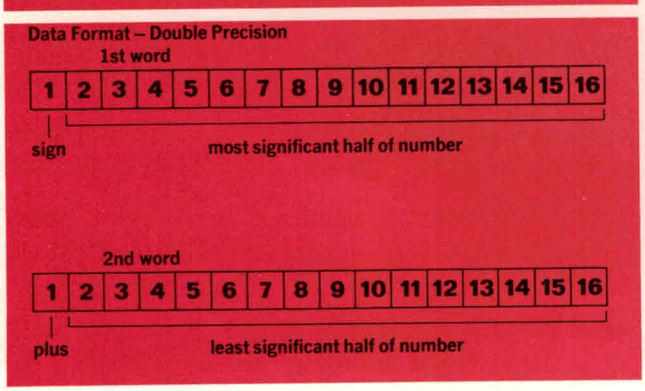
Sixteen-bit data and address word diagrams

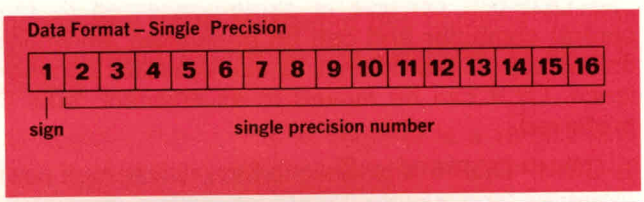


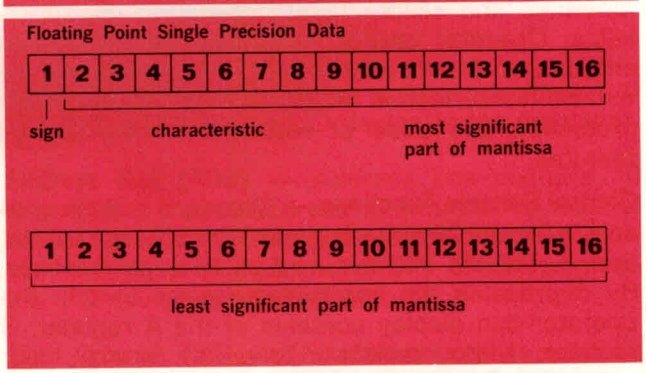


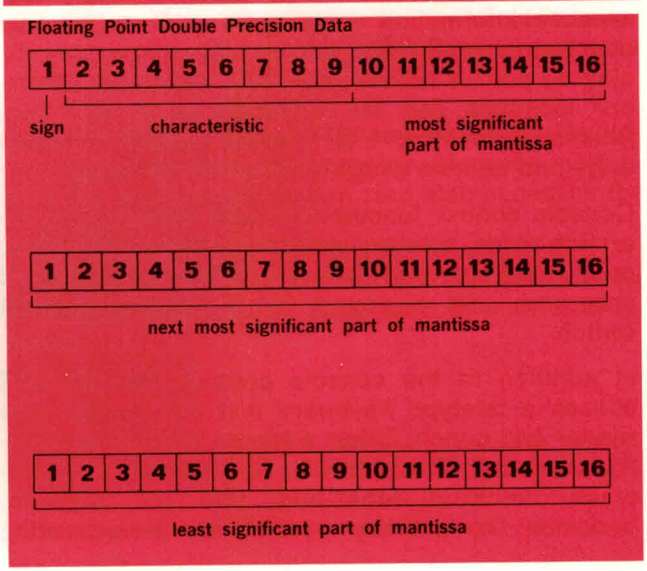












DATA REPRESENTATION AND ADDRESSING MODES

Fixed and floating point, single and double precision; memory is divided into sectors of 512 words each

Sector Addressing (one word per instruction) — When the sector flag is a one, the address portion of the instruction refers to the same sector as that addressed by the program counter.
When the sector flag is a zero, the address portion of the instruction refers to sector zero. (Note: memory lockout option includes sector zero relocation register. When sector flag is zero, instruction refers to sector whose address is in relocation register.)

Indirect Addressing — When indirect addressing is required, the effective address is assumed to be in the location specified by the address portion of the instruction and the selected sector address. However, if the location specified by the address portion of the instruction and the selected sector address also calls for indirect addressing, another cycle of indirect addressing is initiated. This chaining of indirect addresses can continue indefinitely for all instructions which permit indirect addressing. Each indirect address cycle requires an additional 0.96 microseconds for instruction execution.

Indexing — When the index bit is set, the contents of the index register are added to the effective address of the instruction to produce a new effective address. If indexing is specified in a given instruction, it occurs before any indirect addressing occurs. If indexing is specified in an indirect address, it occurs before any further indirect addressing occurs. When indexing is used, no additional time is required for instruction execution.

Extend Mode — Systems with 24K or 32K word memories will be equipped with bank-switching logic whereby an extend mode is included. When in the extend mode, the indirect address format includes 15 address bits in order to access 32K; indexing is specified in the instruction and is applied after indirect addressing.

Fixed Point — Data is represented in two's complement form, with the sign in the most significant bit position followed by 15 magnitude bits. Single precision fixed point values thus range from −32,768 to +32,767. While this is adequate for most applications, the DDP-516 offers both hardware and software double precision capabilities for users who require 30-bit accuracy. Typical double precision times:

Add (hardware)	2.88 μsec
Add (subroutine)	36. μsec

All arithmetic operations in the DDP-516 automatically keep track of the sign. Overflow results in the setting of the C bit indicator.

Floating Point — Used in conjunction with numerous floating point routines in the DDP-516 program library, floating point capabilities include both single and double precision accuracies. Convenient and fast, these routines offer the flexibility of either 7 or 12 digit precision for number ranges of $10^{\pm 38}$.

INSTRUCTION REPERTOIRE

Wide selection of arithmetic, shift, and byte manipulation steps

Type	Mnemonic	Time (μsecs)	Description
Load and Store	LDA	1.92	Load A
	LDX	2.88	Load Index
	IMA	2.88	Interchange Memory and A
	IAB	0.96	Interchange A and B
	CRA	0.96	Clear A
	STA	1.92	Store A
	STX	1.92	Store Index
Arithmetic	ADD	1.92	Add
	SUB	1.92	Subtract
	IRS	2.88	Increment, Replace and Skip
	AOA	0.96	Add One to A
Control	SSP	0.96	Set Sign Plus
	SSM	0.96	Set Sign Minus
	SMK	1.92	Set Mask
	CMA	0.96	Complement A
	CSA	0.96	Copy Sign and Set Sign Plus
	ACA	0.96	Add C to A
	SCB	0.96	Set C
	RCB	0.96	Reset C
	HLT	0.96	Halt
	NOP	0.96	No Operation
	ENB	0.96	Enable Program Interrupt
	INH	0.96	Inhibit Program Interrupt
	TCA	1.44	Two's Complement A
	CHS	0.96	Complement A Sign
Input-Output	OCP	1.92	Output Control Pulse
	SKS	1.92	Skip if Ready Line Set
	INA	1.92	Input to A
	INK	0.96	Input Keys
	OTA	1.92	Output from A
	OTK	1.92	Output Keys
Byte Manipulation	ICA	0.96	Interchange Halves in A
	ICL	0.96	Interchange/Clear Left Half of A
	ICR	0.96	Interchange/Clear Right Half of A
	CAL	0.96	Clear Left Half
	CAR	0.96	Clear Right Half

Type	Mnemonic	Time (μsecs)	Description
Logical	ANA	1.92	Logic AND
	ERA	1.92	Exclusive OR
Shift	LGL	0.96 + .48n	Logical Left Shift
	LGR	0.96 + .48n	Logical Right Shift
	ALR	0.96 + .48n	Logical Left Rotate
	ARR	0.96 + .48n	Logical Right Rotate
	ALS	0.96 + .48n	Arithmetic Left Shift
	ARS	0.96 + .48n	Arithmetic Right Shift
	LLL	0.96 + .48n	Long Left Logical Shift
	LRL	0.96 + .48n	Long Right Logical Shift
	LLR	0.96 + .48n	Long Left Rotate
	LRR	0.96 + .48n	Long Right Rotate
	LLS	0.96 + .48n	Long Arithmetic Left Shift
	LRS	0.96 + .48n	Long Arithmetic Right Shift
Transfer Control	JMP	0.96	Unconditional Jump
	JST	2.88	Jump and Store Location
	CAS	2.88	Compare
	SKP	0.96	Unconditional Skip
	SPL	0.96	Skip if A Plus
	SMI	0.96	Skip if A Minus
	SZE	0.96	Skip if A Zero
	SNZ	0.96	Skip if A Not Zero
	SLZ	0.96	Skip if (A_{16}) Zero
	SLN	0.96	Skip if (A_{16}) One
	SSC	0.96	Skip if C Set
	SRC	0.96	Skip if C Reset
	SS1	0.96	Skip if Sense Switch #1 Set
	SS2	0.96	Skip if Sense Switch #2 Set
	SS3	0.96	Skip if Sense Switch #3 Set
	SS4	0.96	Skip if Sense Switch #4 Set
	SR1	0.96	Skip if Sense Switch #1 Reset
	SR2	0.96	Skip if Sense Switch #2 Reset
	SR3	0.96	Skip if Sense Switch #3 Reset
	SR4	0.96	Skip if Sense Switch #4 Reset
	SSR	0.96	Skip if No Sense Switch Set
	SSS	0.96	Skip if Any Sense Switch Set

OPTIONS

Optional features for expanded capability

High Speed Arithmetic Package — Enhances the arithmetic capability of the DDP-516 by providing hardware implementation of multiply, divide, and normalize. It also provides double-precision load, store, add and subtract capabilities operating on a pair of words in memory and the A and B registers. Instructions include:

MPY	5.28	Multiply
DIV	10.56	Divide
NRM	0.96 +.48n	Normalize
SCA	0.96	Shift count to A
DBL	0.96	Enter double precision mode
SGL	0.96	Enter single precision mode
DLD	2.88	Double load
DST	2.88	Double store
DAD	2.88	Double add
DSB	2.88	Double subtract

Memory Parity — Provides facilities for generating parity on all memory write cycles and checking parity on all memory read cycles. The computer's memory parity error flip-flop can be tested under program control and reset under program control. The setting of the parity error flip-flop generates an interrupt on the standard interrupt line. This interrupt can be inhibited under program control by resetting the interrupt mask. Instructions:

RMP	0.96	Reset memory parity indicator
SPS	0.96	Skip on memory parity error
SPN	0.96	Skip on no memory parity error

Memory Lockout — Facilitates the time-shared execution of undebugged programs concurrently with on-line operation. To this end, the memory sectors containing the on-line program and its data, etc., are protected from accidental alteration. Peripheral equipment is similarly protected to maximize system integrity.

In the restricted mode of operation, no protected location can be altered, and the operations OCP, SKS, OTA, SMK, OTK, INA, HLT, and INH are considered illegal. No instruction is permitted more than eight levels of indirect addressing in this mode. Any instruction attempting to violate these restrictions is aborted and causes an interrupt.

Normal operation is free of all restrictions; the program can execute any instruction in the repertoire. Selection of those memory sectors which are to be protected is controlled by a lockout mask register. It is a 64-bit register, each bit of which is associated with one 512-word memory sector, and contains a zero if the corresponding sector is protected. The setting of LMR is accomplished by SMK instructions. In addition, sector zero may be relocated for those programs not having access to the true sector zero. The relocated sector zero is that sector whose address is in the 6-bit relocation register.

Instructions provided with the memory lockout option include:

ERM	0.96	Enter restricted mode
SMK	1.92	Set relocation register
SMK	1.92	Set lockout mask

Once entered, operation continues in the restricted mode until an interrupt, whether caused by a protection violation or not, occurs.

Real-Time Clock — Permits the computer to keep track of real time by means of a memory location which is incremented by one every 16.67 milliseconds. This location is usually preset by program to a minus value; when it reaches zero, an interrupt occurs.

INPUT/OUTPUT

Unique real-time oriented capabilities

The basic I/O system of the DDP-516 consists of an input/output bus used to transfer full words in and out of the computer. In addition it contains lines which provide timing signals and commands to peripheral devices. Each peripheral device which is tied to the I/O bus has its own buffer and control logic. This feature permits a high degree of flexibility in using multiple devices concurrently and in handling multiple devices through priority interrupt. Devices are addressed by means of the six least significant bits in an I/O instruction. These, plus four function bits, are transmitted via the 10 ADB (address bus) lines to the device where they are decoded.

Priority Interrupt — The standard interrupt system consists of a single interrupt line to which multiple interrupt sources can be connected. When an interrupt occurs the program counter is stored and control is transferred to a standard location. A software routine then sorts out the source of the interrupt and transfers to the correct subroutine. Interrupt sources can be enabled and inhibited individually under program control. Thus the system permits multiple priority interrupt levels with the stacking of interrupts upon interrupts. Assignment of the priority level of a particular source is also under program control.

I/O Modes — There are four basic modes in which data can be transferred back and forth between peripheral devices of the DDP-516.

a. single word transfer
b. single word transfer with interrupt
c. direct multiplexed control (DMC)
d. direct memory access (DMA)

Single Word Transfer Mode — The basic input/output mode of the standard computer is single word transfers under program control. In this mode, words can be read from external devices into the accumulator utilizing INA instructions, and full words can be transferred from the accumulator to the output device using OTA instructions. During input in this mode, the programmer has the option of clearing or not clearing the accumulator before each input (INA) instruction. This allows input characters to be packed into words as part of a basic input routine. In order to make the DDP-516 extremely flexible in real-time applications, the ability to test and skip on the ready status of an I/O device has been included in the basic input and output instructions. Thus the computer is not required to hold off, waiting for a ready signal. Using the single word transfer mode, blocks of input or output data may be transferred to/from memory at word rates up to 130 kc.

Single Word Data Transfer with Interrupt Mode — The interrupt system can also be utilized with the basic input/output commands to provide a powerful input/output mode for real-time processing. In this mode frequent testing of a device for readiness is eliminated. The device ready signal causes a program interrupt. The I/O functions are then performed whereupon the program continues in its normal fashion.

Additional priority interrupt lines, up to a total of 48, may be added to a DDP-516 system.

Direct Multiplexed Control (DMC) — A direct multiplexed control mode is available which permits data transfer between peripheral devices and the memory concurrent with computation. In this mode the starting location to which the block of information is to be transferred and the final location at

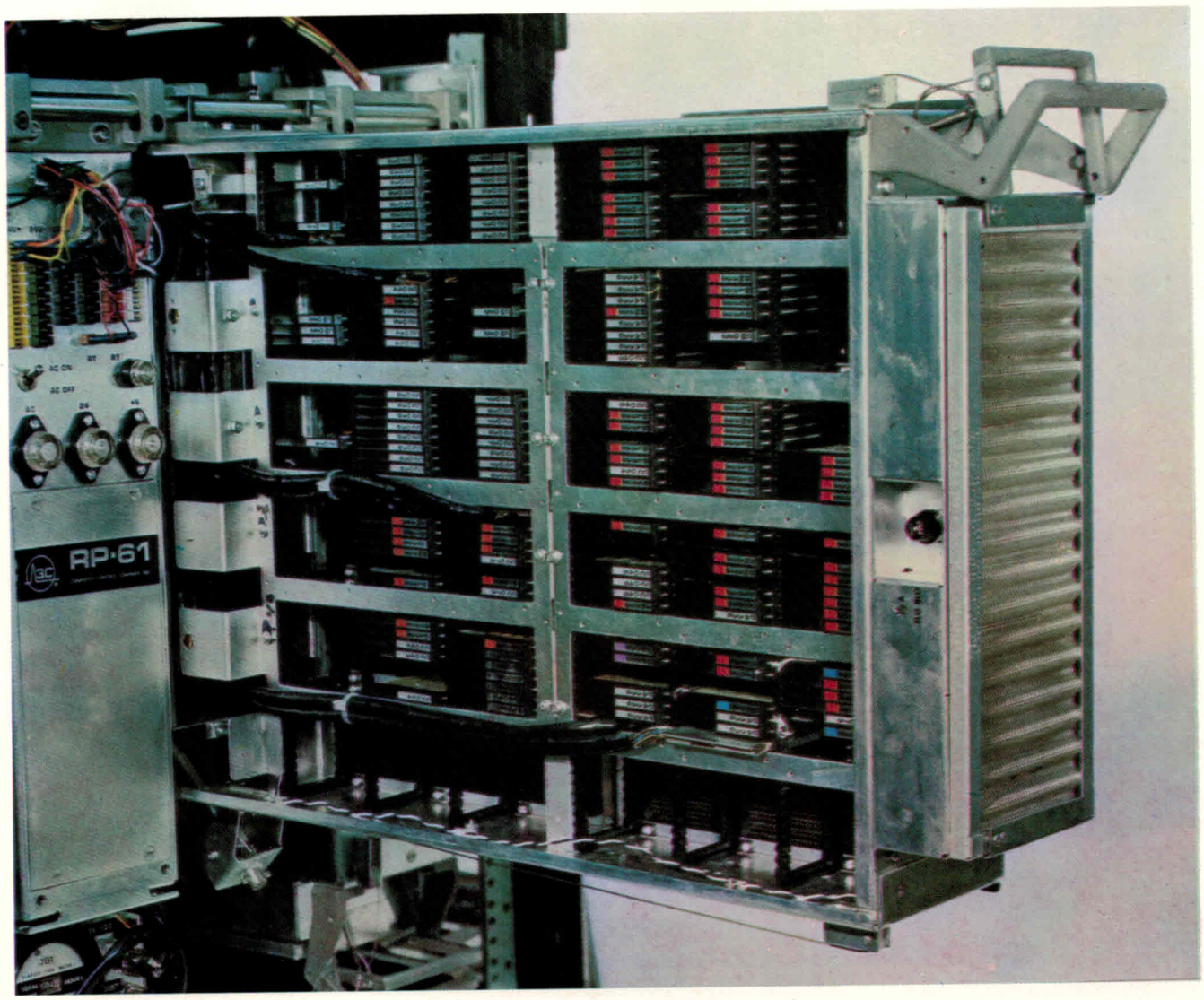
which the block transfer is to be terminated are set up under program control. The data transfer is then initiated by the program. Once this has been done, transfers occur independent of program control until the specified block of memory has been filled.

Since the 15-bit starting and final addresses of the block of memory are stored in standard locations in memory, this is an extremely economical mode of I/O. Up to 16 devices can be connected to the DMC system simultaneously, independently transferring data between each device and a specified block in memory. Because this mode requires only 3.84 microseconds of computer time for each word transfer, a maximum word rate of over 260 kc can be obtained if computation is effectively halted. For slower word rates, any time not needed by the DMC is used by the computer for computation. End of range interrupt (maskable) is a standard feature for each DMC sub-channel. An added option is DMC automatic switching, whereby end of range causes alternate blocks of memory to be used.

Direct Memory Access (DMA) — This channel provides an alternate path to memory via the L register by means of which I/O transfers may be processed on a cycle stealing basis. Up to four sub-channels, each with its own address and range registers, may be multiplexed into the DMA channel. In the time-shared mode, DMA interrupts processing for 1.2 μsecs per word. Maximum response time from data request until transfer complete is 1.92 μsecs on input, 2.64 on output. In the block transfer mode, with program processing suspended, DMA I/O rates exceed one million 16-bit words per second.

MAINTENANCE AND SUPPORT

Designed for easy maintenance; backed by continuing service



MAINTENANCE AND SUPPORT

Designed for easy maintenance; backed by continuing service

It is 3C's philosophy to act as a digital partner to the systems designer and user, supplying digital computers, digital building blocks, and advanced engineering capabilities; and to support these customers in the areas of programming, hardware maintenance, training, and application engineering assistance.

Services included with the DDP-516 are designed to provide the user with continuing support and flow of information before and after delivery.

Maintenance and field expansion have been greatly simplified. Unique front access packaging provides convenient access to all circuits. Central processor and memory swing out individually to expose both circuit modules and interwiring.

Maintenance Training Course — Includes instruction in operation, logic design, diagnostic procedures, diagnostic routines, and preventive maintenance. A logistic support program for personnel with previous digital logic design knowledge is included. This two-week course is provided at no cost.

Programmer Training Course — Includes instructions for programming in machine language, an introduction to DDP-516 programming systems, and instruction in DDP-516 operation. A one-week course is provided at no cost.

Logistic Support Program — Provides after-delivery service and information to DDP-516 users.

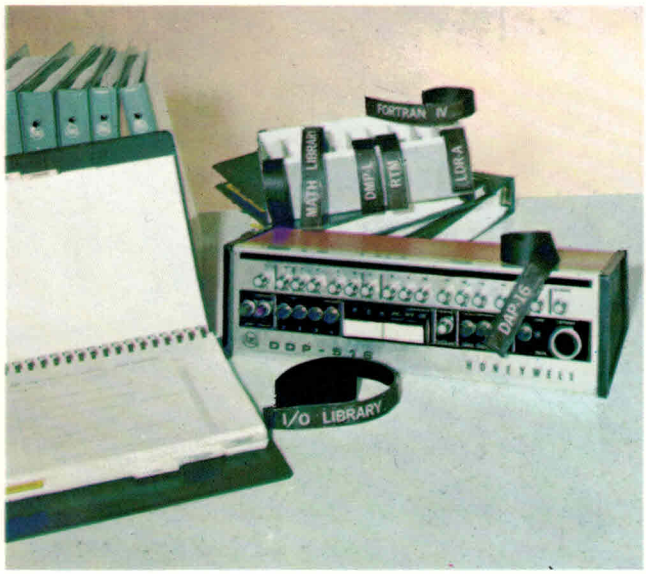
DDP-516 Users' Group (CAP) — Actively exchanges user information and programming sub-routines as developed. Incorporates users of the DDP-116, which is program compatible.

PROGRAMMING SOFTWARE

Comprehensive package is fully field proven

PROGRAMMING SOFTWARE

Comprehensive package is fully field proven



FORTRAN IV — This compiler is available as standard software for the DDP-516. FORTRAN IV is a one pass compiler that will operate in a minimum system consisting of a DDP-516 with 8192 words of core memory. This compiler provides all of the power and flexibility of FORTRAN as defined by the American Standards Association. It features the use of type statements, external statements, block data, double precision, complex, logical and octal constants. From a programmer's point of view it can be said that FORTRAN IV retains all of the ease of programming and the clarity of FORTRAN II while adding the advantages of generality and flexibility.

Assembly Program (DAP-16) — DAP-16 is a symbolic language assembly program. The purpose of DAP-16 is to translate from a symbolic language convenient to the programmer to binary code intelligent to the DDP-516. Translation is optionally made in a two-pass or one-pass process and is generally on a one-for-one basis, that is, for each source statement written by the programmer, one machine instruction is generated by DAP-16. DAP-16 produces either relocatable or absolute object code, and the source language includes the capability of using symbolic addressing, mnemonic machine codes, double-precision operations (optional hardware required) index register instructions, and compound address expressions. In addition, DAP-16 provides octal, decimal and ASCII literals plus a wide variety of pseudo-operations which serve to control the assembly process, define data, allocate core memory or generate linkage to subroutines. The CALL and SUBR pseudo-operations produce FORTRAN IV compatible subroutine linkages.

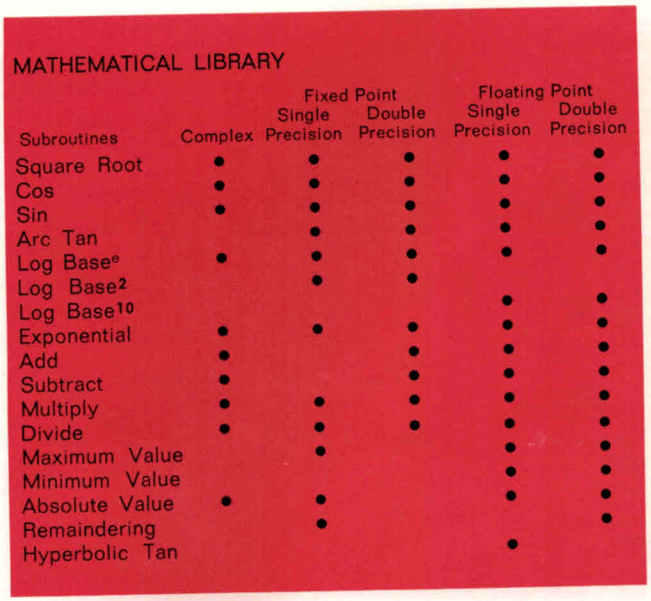
An important feature of DAP-16 is the generation of an extended object code. The extended object code, in conjunction with the desectorizing loader, *permits the programmer to address the DDP-516 as if the entire memory was directly addressable* rather than concerning himself with sector addressing and the indirect address linkage necessary to cross from sector to sector.

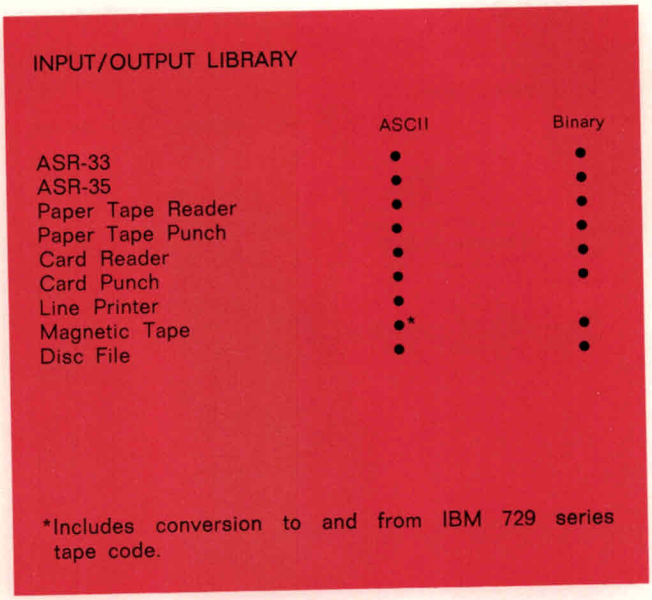
Real-Time Monitor (RTM) — The Real-Time Monitor program increases efficiency of real-time computer systems by automatically time sharing the capabilities of the computer between a combination of real-time and free-time programs. With the RTM program, engineering calculations, debugging, DAP assemblies, FORTRAN IV compilations, or scientific calculations can be performed without interfering with the primary job of the computer; namely, the real-time applications.

RTM is composed of a set of integrated programs which perform the following functions: (1) exercise the required scheduling and control functions necessary to assure the coordinated execution of the several programs sharing the computer's capabilities, (2) recognize and record all interrupts so that they may be appropriately processed, and (3) control and execute all input-output operations.

The minimum hardware system in which the RTM can operate includes 8192 words of core memory, a teletype, real-time clock, eight priority interrupts, high speed I/O such as paper tape or cards, and memory lockout.

Input/Output Selector (IOS) — This program is used in conjunction with major programs supplied with the DDP-516 to establish the input/output communication link with the input/output equipment. Users with varying complements of peri-





pheral equipment are readily accommodated by the modular design of IOS.

Desectorizing Loader — A relocatable program which loads the memory with octal information in absolute or relocatable format. This program is capable of loading the main program and subroutines called by it or called by other subroutines, and completes the transfer vector linkage between the main program and external subroutines. Also included is the capability to generate special indirect address links in sector zero based on addressing information generated by the assembly program or compiler.

Subroutine Library — The standard software package includes an extensive assortment of subroutines to aid the programmer in performing mathematical operations and functions, conversion, and input-output operations.

Mathematical routines are available for single and double precision, fixed and floating point, and complex calculations as indicated in the accompanying chart.

Conversion routines are available for ASCII to fixed point, floating point, and complex; fixed point, floating point, and complex to ASCII; fixed point to floating point; floating point to fixed point; and complex to floating point.

DEBUG Program (COP-516) —A compact relocatable program capable of:

a. Type memory in octal
b. Type corrections into memory
c. Enter a breakpoint into memory and start at a specified location
d. Return to breakpoint and continue with program being debugged
e. Clear memory to zero within limits
f. Search memory for an address within specified limits
g. Start at a location and print the contents of any or all of the following: A register, B register, index register, and C bit, when one of several dynamic options is chosen.

DUMP — A compact relocatable program which enables the user to obtain memory dumps in octal or mnemonic instruction format. The program is completely modular. Each function available is provided in subroutine format, i.e., if the user desires only an octal memory dump, he need only carry the coding necessary to perform this function. The DUMP can communicate with any output equipment available in the system through the input/output selector program.

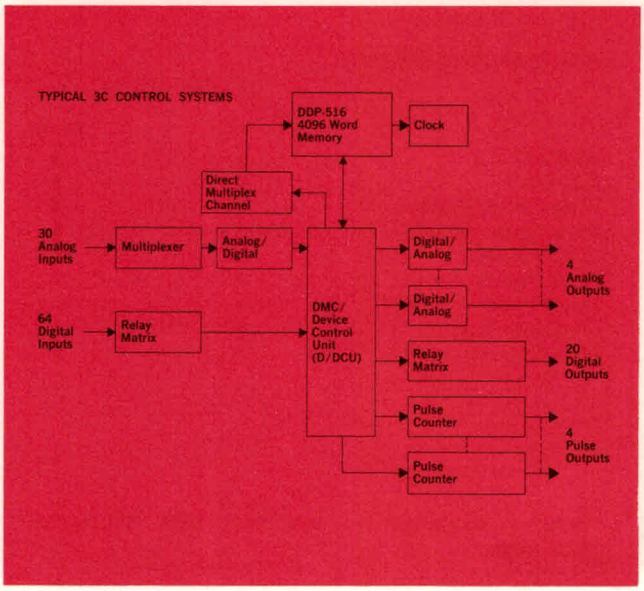
Update — A program which facilitates the deletion, insertion or replacement of source program statements located on paper tape, and whose output is on either paper or magnetic tape. A listing of the modified tape is optionally available as an output.

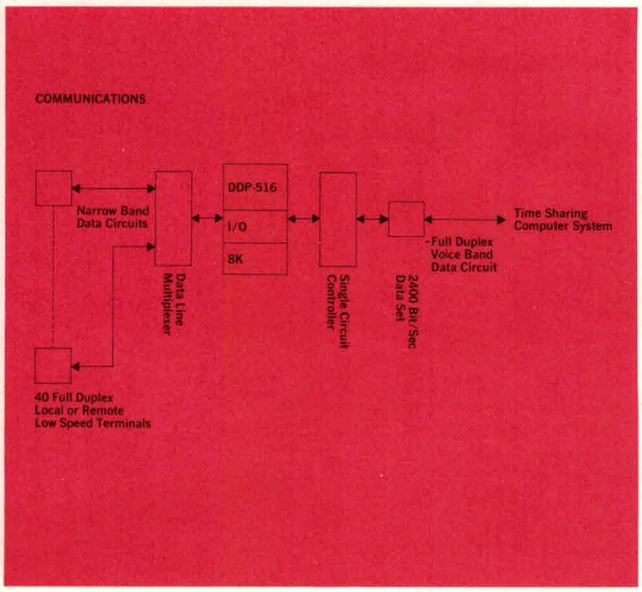
Input/Output Library — Made up of a set of subroutines for each I/O device, offered with the DDP-516. Each I/O routine permits the user to specify the data format most convenient for his application. Any necessary code conversion is handled by the I/O routine. Complete error checking and, where possible, recovery procedures are included.

Verification and Test Programs — An extensive package of verification and test programs is provided with the DDP-516, which includes routines for verifying the operation of the control unit, arithmetic unit, core memory, and the available input/output devices. These routines generate indicative information reflecting the operational status of the equipment being verified.

APPLICATIONS

Wherever real-time capabilities are required





3C, with more than twelve years of digital systems development experience incorporating time tested digital logic modules, has delivered a wide variety of computer systems. These range in design and complexity from multi-loop process control, computerized analysis of speech patterns, to real-time digital flight simulation.

In the medical research field, a computer is being used to study the control of artificial limbs (remote manipulators and orthotic structures). The system is developing control algorithms over prescribed or optimized multi-axis control paths.

Boiler control of an advanced power plant is a typical industrial control application. The computer system is providing the control for start-up and shut-down sequences of a 12 burner boiler as well as continuous monitoring of the boiler operating system.

A numerical control system uses a 3C computer interfaced with an automatic line tracer which digitizes non-dimensioned drawings of sheet metal parts. The system output is a finished N/C punched tape representing the outlines of the parts to be produced on a numerical control milling machine.

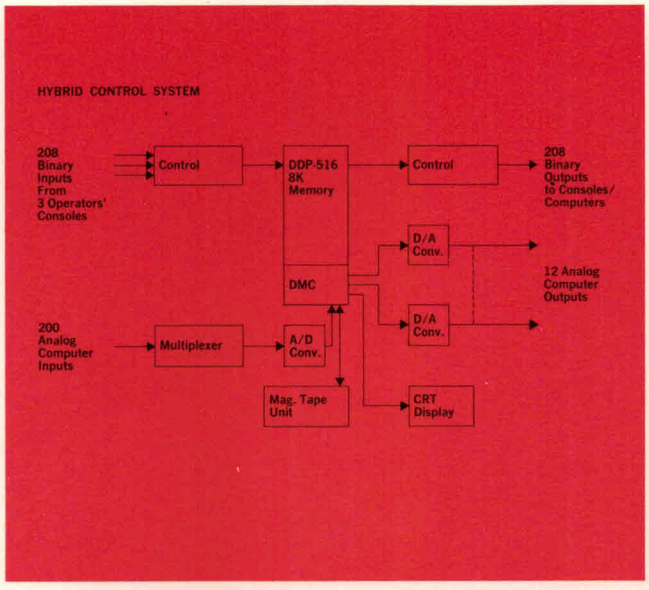
In the rapidly expanding field of radio astronomy, a 3C computer system maps temperature regions on celestial bodies. The computer measures the phase difference between three interferometer antennas and performs an auto-correlation of frequency and phase.

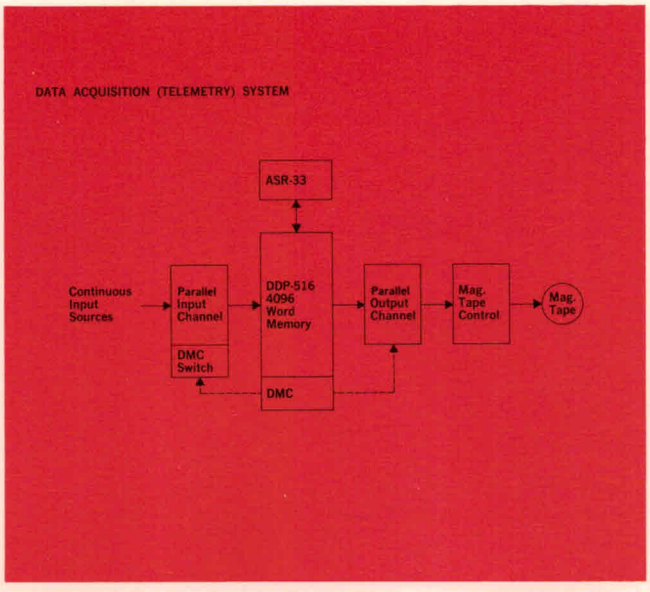
An airline uses a 3C computer system to process real time information concerning flight status and reservation availability. The system employs dual central processors, each time sharing disc and magnetic tape units through programmed electronic switches. Sixteen low and medium speed data communications circuits are switchable between either central processor.

The following illustrations are more detailed explanations of typical 3C computer applications:

Process Control System — This system provides direct dynamic control and optimization over a multi-loop system. The DMC/Device Control Unit (D/DCU) serves as the control interface and is recognized as a single unique address by the computer. Upon computer command, the D/DCU controls block or word transfer, decodes, and scans the input/output channel group desired. Scan intervals are provided by a real-time clock with supplementary interrupts. By using a direct multiplexed channel (DMC), the I/O utilization efficiency is very high, allowing the bulk of the scan interval to be used for computation.

Communications Systems — A large time sharing utility uses multiple 3C computer systems to extend the power of the central processor to remote subscribers. Communications circuit lease cost can rapidly defeat the economies of time sharing when narrow band data circuits must be extended for long distances. The 3C data concentrator system multiplexes 40 full duplex low speed data circuits onto a single medium speed voice band line. In addition to data concentration, the 3C computer detects significant characters, inserts control functions and performs several translations thereby freeing the time sharing processor for its fundamental purpose.





Hybrid Control System — Control of three analog computers and the digitizing, storage, and display of computation data is performed by this system.

The data channels of each analog computer are scanned under computer control by a high speed multiplexer and A/D converter.

A direct multiplexed channel (DMC) enters the data into memory where operations are performed. The modified data is transferred by another DMC to a magnetic tape unit. The data may also be displayed for plotting and analysis on the CRT with full point, character, and vector generation capability.

Commands and control of the analog computers are provided by three operator consoles interfacing to the digital computer through binary input and output lines.

Data Acquisition (Telemetry) — Continuous high speed data is accessed by the DDP-516, formatted, and written on IBM compatible tape for later processing. Input and output are both under control of the DMC for simultaneous I/O. Input utilizes the DMC automatic switching option to allow hardware switching of block limits during a word time; program has a frame time to switch buffer addresses and to control the tape unit. Magnetic tape interface automatically converts words to characters, and assigns parity (BCD or binary) to each.

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