A = A register (16 bits)
ADB = Address bus
B = B register (16 bits)
C = Carry bit (C-bit)
D = Input/output device code
DP = Double precision mode bit
EA = Effective address
F = Input/output function code
G = Generic instruction
INB = Input bus
IO = Input/output and test instruction
MR = Memory reference instruction (Index bit, indirect address bit, and sector bit applicable)
OTB = Output bus
P = Program counter register (16 bits)
PI = Program interrupt enable indicator
PMI = Previous mode indicator (extended addressing option)
SC = Shift count

SH = Shift instruction
X = Index register (16 bits)
( ) = Contents of a hardware register
[ ] = Contents of core memory location
∧ = Logical AND
∨ = Logical OR
⊻ = Exclusive OR
¯ = Logical NOT
+ = Algebraic addition
→ = Replaces
⇄ = is exchanged with
¬ = Discarded
* = Optional instruction
@ = CPU must be in double precision mode
** = Instructions STX and LDX have the same operation code (15). STX has an index bit of 0; LDX has an index bit of 1.
*** = Instructions OTA and SMK have the same operations code (74). SMK has device address D=20 or 24; OTA has D≠20 or 24.

DDP-516 PERIPHERAL DEVICE CODES

CHARACTER	ASCII CODE	HOLLERITH CARD CODE	MAG TAPE CODE
0	260	0	12
1	261	1	01
2	262	2	02
3	263	3	03
4	264	4	04
5	265	5	05
6	266	6	06
7	267	7	07
8	270	8	10
9	271	9	11
A	301	12-1	61
B	302	12-2	62
C	303	12-3	63
D	304	12-4	64
E	305	12-5	65
F	306	12-6	66
G	307	12-7	67
H	310	12-8	70
I	311	12-9	71
J	312	11-1	41
K	313	11-2	42
L	314	11-3	43
M	315	11-4	44
N	316	11-5	45
O	317	11-6	46
P	320	11-7	47
Q	321	11-8	50
R	322	11-9	51
S	323	0-2	22
T	324	0-3	23
U	325	0-4	24
V	326	0-5	25
W	327	0-6	26
X	330	0-7	27
Y	331	0-8	30
Z	332	0-9	31
Space	240	Blank	20
!	241^2	8-6	16
"	242^2	0-8-7	37
#	243^2		
$	244^2	11-8-3	53
%	245^2	12-8-5	75
&	246^2		
'	247^2	8-4	14
(	250^2	0-8-4	34
)	251^2	12-8-4	74
*	252^2	11-8-4	54
+	253^2	12	60
,	254	0-8-3	33
–	255	11	40
.	256	12-8-3	73
/	257	0-1	21
:	272	8-5	15
;	273	11-8-2	52
<	274^2	11-8-7	57
=	275^2	8-3	13
>	276^2	8-7	17
?	277^2		
@	300^2		
[	333^3	11-8-5	55
\	334^4	12-8-6	76
]	335^5	0-8-6	36
↑	336^6	12-8-2	72
←	337	12-8-7	77

NOTES:
1. When writing magnetic tapes in even parity (BCD) mode, 00_8 is written as 12_8; conversely when reading in even parity, 12_8 is read as 00_8.
2. Upper case characters on ASR-33/35
3. Upper case VT on ASR-33/35
4. Upper case FORM on ASR-33/35
5. Upper case M on ASR-33/35
6. Upper case N on ASR-33/35

CONTROL AND SENSING CODES FOR ASR-33/35 AND HIGH SPEED PAPER TAPE READER/PUNCH

		ASR 33/35
OCP	'0004	Enable ASR-33/35 in input mode
OCP	'0104	Enable ASR-33/35 in output mode
SKS	'0004	Skip if ready
SKS	'0104	Skip if not busy
SKS	'0504	Skip if input not stop code
INA	'0004	Input ASCII code if ready
INA	'0204	Input binary code if ready
INA	'1004	Clear A and input ASCII code if ready
INA	'1204	Clear A and input binary code if ready
OTA	'0004	Output ASCII code if ready
OTA	'0204	Output binary code if ready
		Paper Tape Reader
OCP	'0001	Start paper tape reader
OCP	'0101	Stop paper tape reader
SKS	'0001	Skip if paper tape reader is ready
INA	'0001	Input if paper tape reader ready
INA	'1001	Clear A and input if paper tape reader ready
		Paper Tape Punch
OCP	'0002	Enable paper tape punch
OCP	'0102	Paper tape punch power off
SKS	'0002	Skip if paper tape punch is ready
SKS	'0102	Skip if paper tape punch is enabled
OTA	'0002	Output to paper tape if ready

SUMMARY OF DAP--16 PSEUDO-OPERATIONS

OPERATION MNEMONIC	MEANING
***	Op code set by program
ABS	Absolute Mode
BCI	Binary coded information
BES	Block ending with symbol
BSS	Block starting with symbol
BSZ	Block storage of ZEROs
CF1	Configuration DDP-116
CF4	Configuration DDP-416
CF5	Configuration DDP-516
CALL	Call Subroutine
COMN	Put in common storage
DAC	Define Address Constant
DBP	Double Precision decimal to binary
DEC	Decimal to binary
EJCT	Eject
END	End of source program
EQU	Equals
EXD	Enter extended desectoring
FIN	Finish; punch out literals
LIST	Generate listing
LOAD	Load Mode
LXD	Leave extended desectoring
MOR	More
NLST	No listing
OCT	Octal to binary
ORG	Origin
PZE	Plus Zero
REL	Relocatable mode
SETB	Set base sector
SUBR	Subroutine entry point
XAC	Define External Address Constant

ASR-33/35 FUNCTION CONTROLS

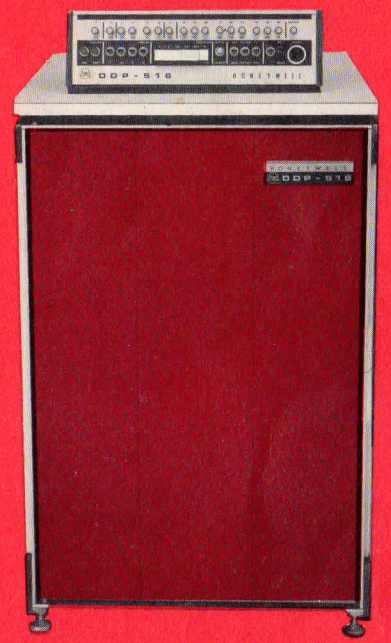
FUNCTION	OCTAL CODE
Bell	207
Line Feed	212
Return	215
X on	221
X off	223
Rub out	377

OP CODE OCTAL	MNEMONIC	INSTRUCTION	TYPE	EXECUTION TIME (μSEC)
01	JMP	Unconditional Jump	MR	0.96
02	LDA	Load A	MR	1.92
02	DLD*@	Double Load	MR	2.88
03	ANA	AND to A	MR	1.92
04	STA	Store A	MR	1.92
04	DST*@	Double Store	MR	2.88
05	ERA	Exclusive OR to A	MR	1.92
06	ADD	Add	MR	1.92
06	DAD*@	Double Add	MR	2.88
07	SUB	Subtract	MR	1.92
07	DSB*@	Double Subtract	MR	2.88
10	JST	Jump and Store Location	MR	2.88
11	CAS	Compare	MR	2.88
12	IRS	Increment, Replace and Skip	MR	2.88
13	IMA	Interchange Memory and A	MR	2.88
14	OCP	Output Control Pulse	IO	1.92
15	LDX**	Load X	MR	2.88
15	STX**	Store X	MR	1.92
16	MPY*	Multiply	MR	5.28
17	DIV*	Divide	MR	10.56 (max)
34	SKS	Skip if Ready Line Set	IO	1.92
54	INA	Input to A	IO	1.92
74	OTA***	Output from A	IO	1.92
74	SMK***	Set Mask	IO	1.92
0400	LRL	Long Right Logical Shift	SH	0.96 + 0.48N
0401	LRS	Long Arithmetic Right Shift	SH	0.96 + 0.48N
0402	LRR	Long Right Rotate	SH	0.96 + 0.48N
0404	LGR	Logical Right Shift	SH	0.96 + 0.48N
0405	ARS	Arithmetic Right Shift	SH	0.96 + 0.48N
0406	ARR	Logical Right Rotate	SH	0.96 + 0.48N
0410	LLL	Long Left Logical Shift	SH	0.96 + 0.48N
0411	LLS	Long Arithmetic Left Shift	SH	0.96 + 0.48N
0412	LLR	Long Left Rotate	SH	0.96 + 0.48N
0414	LGL	Logical Left Shift	SH	0.96 + 0.48N
0415	ALS	Arithmetic Left Shift	SH	0.96 + 0.48N
0416	ALR	Logical Left Rotate	SH	0.96 + 0.48N
000000	HLT	Halt	G	1.44
000005	SGL*	Enter Single Precision Mode	G	0.96
000007	DBL*	Enter Double Precision Mode	G	0.96
000011	DXA*	Disable Extended Addressing	G	0.96
000013	EXA*	Enable Extended Addressing	G	0.96
000021	RMP*	Reset Memory Parity Error	G	0.96
000041	SCA*	Shift Count to A	G	0.96
000043	INK	Input Keys	G	0.96
000101	NRM*	Normalize	G	0.96 + 0.48N
000201	IAB	Interchange A and B	G	0.96
000401	ENB	Enable Program Interrupt	G	0.96
001001	INH	Inhibit Program Interrupt	G	0.96
001401	ERM*	Enter Restricted Mode	G	0.96
100000	SKP	Unconditional Skip	G	0.96
100001	SRC	Skip if C Reset	G	0.96
100002	SR4	Skip if Sense Switch No. 4 Reset	G	0.96
100004	SR3	Skip if Sense Switch No. 3 Reset	G	0.96
100010	SR2	Skip if Sense Switch No. 2 Reset	G	0.96
100020	SR1	Skip if Sense Switch No. 1 Reset	G	0.96
100036	SSR	Skip if No Sense Switch Set	G	0.96
100040	SZE	Skip if A Zero	G	0.96
100100	SLZ	Skip if (A_{16}) is Zero	G	0.96
100200	SPN*	Skip on No Memory Parity Error	G	0.96
100400	SPL	Skip if A Sign Plus	G	0.96
101000	NOP	No Operation	G	0.96
101001	SSC	Skip if C Bit Set	G	0.96
101002	SS4	Skip if Sense Switch No. 4 Set	G	0.96
101004	SS3	Skip if Sense Switch No. 3 Set	G	0.96
101010	SS2	Skip if Sense Switch No. 2 Set	G	0.96
101020	SS1	Skip if Sense Switch No. 1 Set	G	0.96
101036	SSS	Skip if Any Sense Switch Set	G	0.96
101040	SNZ	Skip if A Non-Zero	G	0.96
101100	SLN	Skip if (A_{16}) Is One	G	0.96
101200	SPS*	Skip on Memory Parity Error	G	0.96
101400	SMI	Skip if A Sign Minus	G	0.96
140024	CHS	Complement A Sign	G	0.96
140040	CRA	Clear A	G	0.96
140100	SSP	Set A Sign Plus	G	0.96
140200	RCB	Reset C Bit	G	0.96
140320	CSA	Copy Sign And Set Sign Plus	G	0.96
140401	CMA	Complement A	G	0.96
140407	TCA	2's Complement A	G	1.44
140500	SSM	Set A Sign Minus	G	0.96
140600	SCB	Set C Bit	G	0.96
141044	CAR	Clear A, Right Half	G	0.96
141050	CAL	Clear A, Left Half	G	0.96
141140	ICL	Interchange and Clear Left Half of A	G	0.96
141206	AOA	Add One to A	G	0.96
141216	ACA	Add C to A	G	0.96
141240	ICR	Interchange and Clear Right Half of A	G	0.96
141340	ICA	Interchange Characters In A	G	0.96
171020	OTK	Output Keys	G	1.92

@ CPU must be in double precision mode
* Optional instruction. N = Number of shifts
** Instructions STX and LDX have the same operation code (15). STX has an index bit of 0; LDX has an index bit of 1.
*** Instructions OTA and SMK have the same operations code (74). SMK has device address D=20 or 24; OTA has D≠20 or 24.

Honeywell, Computer Control Division, Framingham, Mass. 01701

PROGRAMMERS REFERENCE CARD

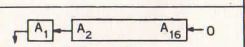
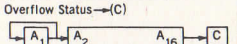
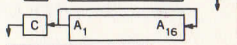
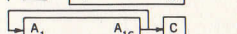
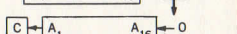
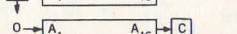


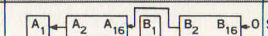
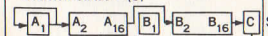
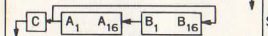
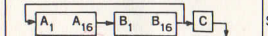
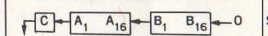
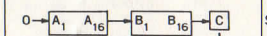
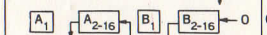
MICRO M COMP

DDP-516

Honeywell

COMPUTER CONTROL DIVISION

CATEGORY	OP-CODE MNEMONIC	OP-CODE OCTAL	FUNCTION	TYPE
Load and Store	CRA	140040	0 → (A)	G
	LDA	02	[EA] → (A)	MR
	DLD*@	02	[EA] → (A) [EA+1] → (B)	MR
	STA	04	(A) → [EA]	MR
	DST*@	04	(A) → [EA] (B) → [EA+1]	MR
	LDX**	35 ~~15~~	[EA] → (X) [EA] → [00000]	MR
	STX**	15	(X) → [EA]	MR
	IAB	000201	(A) ⇄ (B)	G
	SCA*	000041	(SC) → (A_{12-16}) 0 → (A_{1-11})	G
	IMA	13	(A) ⇄ [EA]	MR
Half Word	CAL	141050	0 → (A_{1-8}) (A_{9-16}) are unchanged	G
	CAR	141044	0 → (A_{9-16}) (A_{1-8}) are unchanged	G
	ICA	141340	(A_{1-8}) ⇄ (A_{9-16}) (A_1) is interchanged with (A_9) (A_2) is interchanged with (A_{10}), etc.	G
	ICL	141140	(A_{1-8}) → (A_{9-16}) 0 → (A_{1-8})	G
	ICR	141240	(A_{9-16}) → (A_{1-8}) 0 → (A_{9-16})	G
Arithmetic	ADD	06	(A) + [EA] → (A) Overflow Status → (C)	MR
	DAD*@	06	(A,B) + [EA,EA+1] → (A_{1-16}), (B_{2-16}) 0 → (B_1) Overflow Status → (C)	MR
	SUB	07	(A) − [EA] → (A) Overflow Status → (C),	MR
	DSB*@	07	(A,B) − [EA,EA+1] → (A_{1-16}), (B_{2-16}) 0 → (B_1) Overflow Status → (C)	MR
	MPY*	16	(A) × [EA] → (A,B), (C) is unchanged	MR
	DIV*	17	(A,B) ÷ [EA] → (A) Remainder → (B) Improper Divide Status → (C)	MR
	ACA	141216	(A) + (C) → (A) Overflow Status → (C)	G
	AOA	141206	(A) + 1 → (A) Overflow Status → (C)	G
	TCA	140407	Two's complement (A) → (A) (C) is unchanged	G
Logical	ANA	03	(A) ∧ [EA] → (A)	MR
	ERA	05	(A) ⊻ [EA] → (A)	MR
	CMA	140401	($\bar{A}$) → (A)	G
	CSA	140320	(A_1) → (C), 0 → (A_1) Bits 2 through 16 of A are not changed.	G
	SSM	140500	1 → (A_1) Bits 2 through 16 of A are not changed.	G
	SSP	140100	0 → (A_1) Bits 2 through 16 of A are not changed.	G
	CHS	140024	($\bar{A}_1$) → (A_1) Bits 2 through 16 of A are not changed.	G
Shift	ALS	0415		SH
	ARS	0405		SH
	ALR	0416		SH
	ARR	0406		SH
	LGL	0414		SH
	LGR	0404		SH

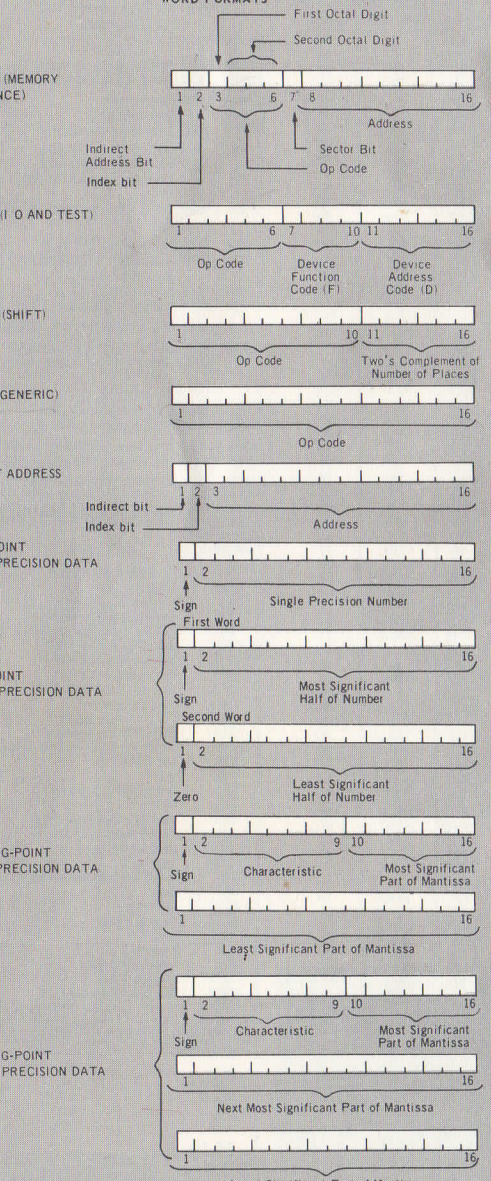
CATEGORY	OP-CODE MNEMONIC	OP-CODE OCTAL	FUNCTION	TYPE
Shift (cont)	LLS	0411	 Overflow Status→(C)	SH
	LRS	0401		SH
	LLR	0412		SH
	LRR	0402		SH
	LLL	0410		SH
	LRL	0400		SH
	NRM*	000101	 Until (A_1) ≠ (A_2) number of shifts → (SC)	G

Control	CAS	11	If (A) > [EA], execute next instruction
			If (A) = [EA], skip next instruction
			If (A) < [EA], skip next two instructions
				MR

	JMP	01	EA → (P) Next instruction to be executed is at location EA	MR
	JST	10	(P_{3-16}) → [EA_{3-16}]; [$EA_{1,2}$] not changed EA + 1 → (P) Next instruction to be executed is at EA+1	MR
	IRS	12	[EA] + 1 → [EA] ; if original [EA] + 1 = 0, skip next instruction	MR
	SKP	100000	Skip next instruction	G
	SPL	100400	Skip next instruction if (A_1) = 0	G
	SMI	101400	Skip next instruction if (A_1) = 1	G
	SZE	100040	Skip next instruction if (A) = 0	G
	SNZ	101040	Skip next instruction if (A) ≠ 0	G
	SLZ	100100	Skip next instruction if (A_{16}) = 0	G
	SLN	101100	Skip next instruction if (A_{16}) = 1	G
	SRC	100001	Skip next instruction if (C) = 0	G
	SSC	101001	Skip next instruction if (C) = 1	G
	SR1	100020	Skip next instruction if SS1 is off.	G
	SR2	100010	Skip next instruction if SS2 is off.	G
	SR3	100004	Skip next instruction if SS3 is off.	G
	SR4	100002	Skip next instruction if SS4 is off.	G
	SSR	100036	Skip next instruction if all sense switches are off.	G
	SS1	101020	Skip next instruction if SS1 is on.	G
	SS2	101010	Skip next instruction if SS2 is on.	G
	SS3	101004	Skip next instruction if SS3 is on.	G
	SS4	101002	Skip next instruction if SS4 is on.	G
	SSS	101036	Skip next instruction if any sense switch is on.	G
	SPN*	100200	Skip on no memory parity error	G
	SPS*	101200	Skip on memory parity error	G
	HLT	000000	Stop computer operation.	G
	NOP	101000	No operation.	G
	RCB	140200	0 → (C)	G
	SCB	140600	1 → (C)	G
	ENB	000401	Enable interrupt. (PI indicator lights)	G
	INH	001001	Inhibit Interrupt. (PI indicator extinguished)	G
	INK	000043	(C) → (A_1) (DP Mode) → (A_2) (PMI) → (A_3) 0 → (A_{4-11}) (SC) → (A_{12-16})	G
	OTK	171020	(A_1) → (C) (A_2) → (DP Mode) (A_3) → (PMI) (A_{12-16}) → (SC)	G
	SGL*	000005	Enter Single Precision Mode	G
	DBL*	000007	Enter Double Precision Mode	G
	EXA*	000013	Enable Extended Addressing	G
	DXA*	000011	Disable Extended Addressing	G
	ERM*	001401	Enter Restricted Mode	G
	RMP*	000021	Reset Memory Parity Error	G

CATEGORY	OP-CODE MNEMONIC	OP-CODE OCTAL	FUNCTION	TYPE
Input/Output	OCP	14	(FD_{7-16}) → (ADB_{7-16}) Direct Control Pulse (F) to I/O Device (D)	IO
	INA	54	If not ready, no input, execute next instruction. If ready, and (F_7) = 1, (INB) → (A) and skip next instruction. If ready, and (F_7) = 0, (INB) ∨ (A) → (A) and skip next instruction.	IO
	OTA***	74	If not ready, no output, execute next instruction. If ready, (A) → (OTB), skip next instruction.	IO
	SMK***	74	(A) → (OTB)	IO
	SKS	34	Skip or execute next instruction depending on sense condition.	IO

WORD FORMATS



***Instructions OTA and SMK have the same operation code (74). SMK has device address D = 20 or 24; OTA has D ≠ 20 nor 24.