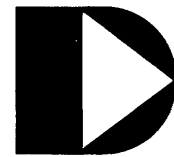


# Datapoint 3300/Maintenance

DATAPOINT CORPORATION



The leader in dispersed data processing™

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## INTRODUCTION

This manual is for use by persons with the responsibility to repair and maintain the Datapoint 3300.

The manual is arranged to provide a detailed explanation of the Theory of Operation in a logical sequence.

The theory of operation details all functions within the Datapoint 3300. Review of this section in conjunction with the associated diagrams should thoroughly acquaint the technician with the designed operational characteristics of the equipment.

Extreme caution must be used in replacing a component on any of the printed circuit cards. Recommended tools and techniques to preclude serious damage to the cards are provided in the maintenance section of this manual.

## DESCRIPTION

The Datapoint 3300 is a data terminal, incorporating the most advanced electronic engineering, modern design and compatibility with all time sharing services.

To become familiar with the functions of the Datapoint 3300, refer to the Operators Instruction Manual supplied with the equipment.

Table 1-1 provides a listing of dimensions, electrical and interface specifications for the Datapoint 3300.

**Table 1-1. Specifications**

## DIMENSIONS

Width	18 inches
Height	13 inches
Depth	18 inches
Weight	48 pounds

## ELECTRICAL

Power Input	200 Watts, 115 VAC, Single Phase, 60 HZ
Heat Dissipation	683 BTU/hr.
Operating Temperature Range	40°F to 100°F
Humidity Limits	0% to 95%
Display Size	10 1/8" to 7 5/8"
Active Display Size	8" x 6"
Spot Diameter	0.01 inches
Repeatability	±0.001 inches
Characters per Line	72
Number of Lines	25
Number of Characters Displayable	1800
Intensity	Adjustable
Brightness	75 ft. Lamberts/Min.
Contrast Ratio	12:1
Types of Phosphor	P31
Character Size	0.11" x 0.18"
Character Generation	
Method 5 x 7	Dotmatrix
Deflection Type	Magnetic
Deflection Method	Modulated Scan
Character Generator	Read Only Memory
Type of Memories	MOS
Memory Size:	
ROM	2240 Bits
Circulating	10,800 Bits
	1800 Characters
Display Refresh Rate	60 Times/Sec.
Character Set	Upper Case ASC II
Cursor	Non-Destructive, Blinking

**Table 1-1. Specifications (Cont)**

## INTERFACE

Serial (Input and Output)	EIA RS-232-B
Bit Rates	110, 220, 440, 880, 1760 150, 300, 600, 1200, 2400
Parallel (Input Only)	Logic Level

## SIGNAL CHARACTERISTICS:

### (EIA RS-232-B Code)

1. RECEIVE
  - a. MARK -3 TO -25 VOLTS
  - b. SPACE +3 TO +25 VOLTS
2. TRANSMIT
  - a. MARK -10 VOLTS WITH 3K LOAD
  - b. SPACE +6 VOLTS WITH 3K LOAD

MAXIMUM SHORT CIRCUIT CURRENT 500 MA

TERMINATING IMPEDANCE 3K to 7K

CONNECTOR TYPE 17-10250-1  
Amphenol  
(or equivalent)

## PIN ASSIGNMENTS

<u>PIN NO.</u>	<u>FUNCTION</u>
1	Protective Ground
2	Transmitted Data
3	Receive Data
4	Request to Send
7	Signal Ground
8	Data Carrier Detector
11	Reverse Channel Transmitted Data
12	Reverse Channel Receive Data
18	Read Only Data (See Note)
20	Data Terminal Ready
25	Use for Computer Terminal Test

## NOTE

This data may be used to drive a read only copy device and has the same signal characteristics as the normal transmitted data.

Table 1-2 provides the ASC II code assignments for all of the characters and functions used in the Datapoint 3300.

Table 1-2. ASC II Code Assignments

BIT #				7	0	0	0	0	1	1	1	1
				6	0	0	1	1	0	0	1	1
4	3	2	1	5	0	1	0	1	0	1	0	1
0	0	0	0				SP	Ø	@	P		
0	0	0	1			X on	!	1	A	Q		
0	0	1	0				"	2	B	R		
0	0	1	1			X off	#	3	C	S		
0	1	0	0				\$	4	D	T		
0	1	0	1		WRU		%	5	E	U		
0	1	1	0				&	6	F	V		
0	1	1	1		BELL		'	7	G	W		
1	0	0	0			c →	(	8	H	X		
1	0	0	1			c ←	)	9	I	Y		
1	0	1	0		LINE FEED	c ↑	*	:	J	Z		
1	0	1	1		c ↓	ESC	+	;	K	[		
1	1	0	0			HOME DOWN	,	<	L	\		
1	1	0	1		RE-TURN	HOME UP	-	=	M	]		
1	1	1	0		SPOW LATCH	ERASE EOL	.	>	N	↑		
1	1	1	1		SPOW UN LATCH	ERASE EOF	/	?	O	←		RUB OUT

c Cursor

# DIAGRAM SYMBOLISM

## SCHEMATIC AND LOGIC DIAGRAMS

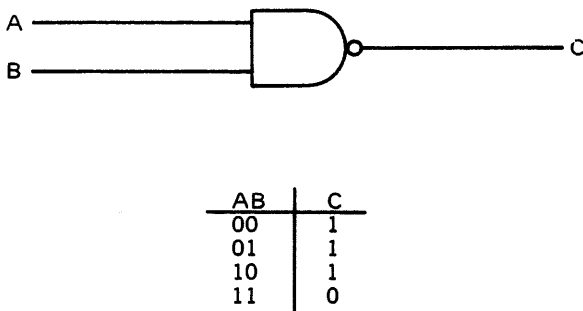
Symbols used on schematic and logic diagrams are generally Military Specification symbols. However, no attempt has been made to conform to Military standards.

The 7400 series, TTL logic family is used. A "one" is high (+5v); a "zero" is low (0v).

Only two types of gates, NAND and NOR are employed.

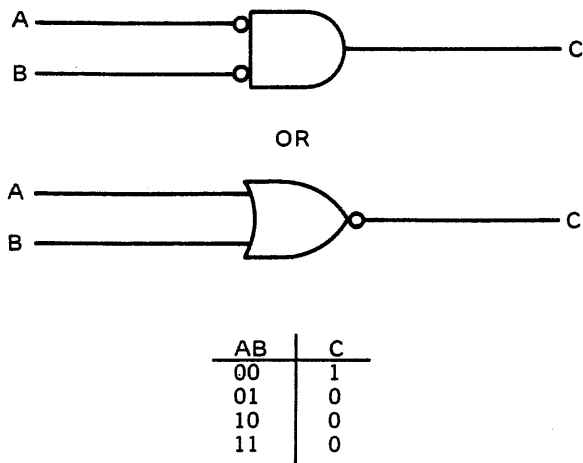
The small circle used at the input or output of the symbols indicates that the active level is a low.

The NAND gate is used in two, three, four, and eight input configurations. The symbol and truth table for the NAND gate are shown in figure 1-1.



**Figure 1-1. NAND Gate**

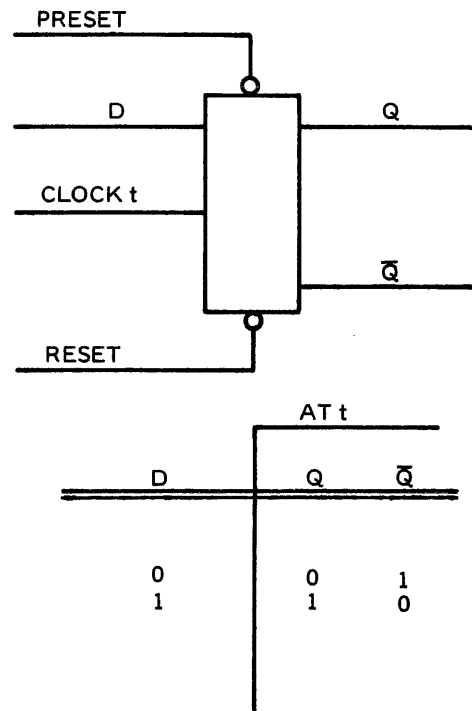
The NOR gate is used only in the two input configuration. The symbols and truth table for NOR gates are shown in figure 1-2.



**Figure 1-2. NOR Gates**

D and JK are the only two types of flip flops used.

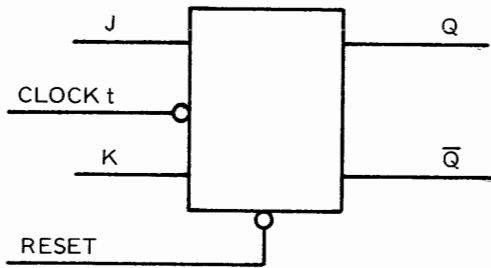
The symbol and truth table for the D flip-flops are shown in figure 1-3. The input at D determines which state the Q output will go on the ascending edge of the next clock. The preset and reset lines are not related to clock time and will override any D input at clock time. A low going pulse on the preset will result in a high output at Q. A low going pulse on the reset will result in a high output at  $\bar{Q}$ .



**Figure 1-3. D Flip-Flop**

The symbol and truth table for the JK flip-flops are shown in figure 1-4. The JK flip-flop utilizes the descending edge of the clock to provide two inputs for control. The J input controls the next state of the Q output and the K input controls the next state of the  $\bar{Q}$  output. The J and K inputs are usually complements of each other, however, this is not a requirement. When the J and K inputs are both low, no change will occur at the outputs at clock time. When the J and K inputs are both high, the outputs will complement at clock time. Two variations are used for

inputs to the JK flip-flops. The first provides for one J input and one K input while the second variation provides for three J inputs and three K inputs. The three inputs function as an AND gate and all three J inputs or all three K inputs must be high to reflect a high on the output being controlled.



AT t (DESCENDING EDGE OF CLOCK)

JK	Q	Q̄
01	0	1
10	1	0
11	Q̄	Q
00	Q	Q̄

**Figure 1-4. JK Flip-Flop**

Other special circuits used, such as dividers, counters and one-shots are symbolized by a rectangle with all of the inputs and outputs marked.

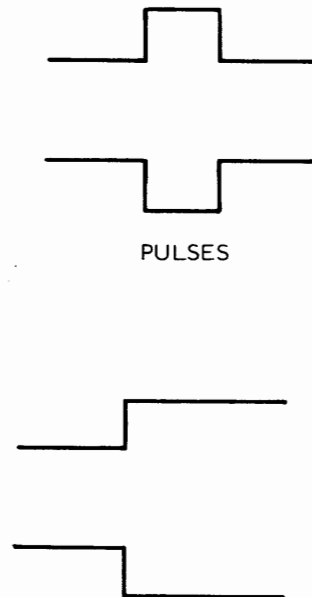
**BLOCK DIAGRAMS**

The functional block diagrams are composed of circuit elements connected by lines to indicate

the direction of information flow. The elements are represented by rectangles with no significance to size. Each rectangle contains a letter designator which represents the general type of circuit. The letter designators are:

- G ..... Gate
- L ..... Latch
- D ..... D flip-flop
- JK ..... JK flip-flop

The most significant waveforms are shown adjacent to appropriate pins. Figure 1-5 is typical of pulses and levels generally shown in waveforms.

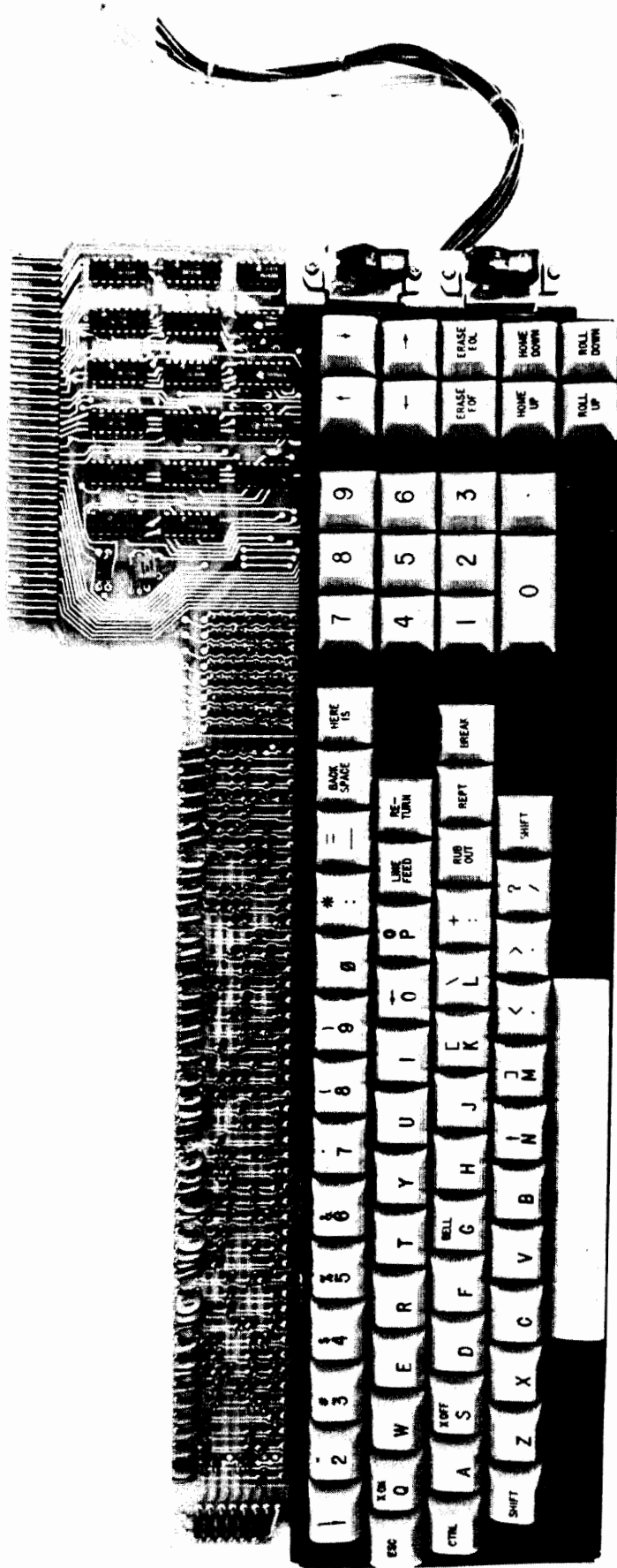


LEVELS, TRANSITION SHOWS DIRECTION OF INITIAL MOVEMENT. LEVEL REMAINS UNTIL OTHER ACTION IS TAKEN.

**Figure 1-5. Typical Waveforms**

**ILLUSTRATIONS**

Figures 1-6 through 1-9 show the printed circuit cards used in the Datapoint 3300.



KEYBOARD

ANSWERBACK

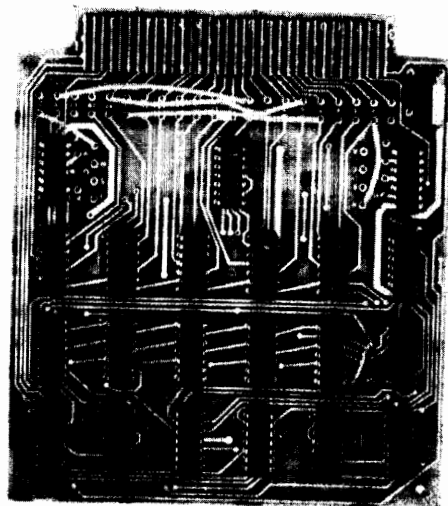
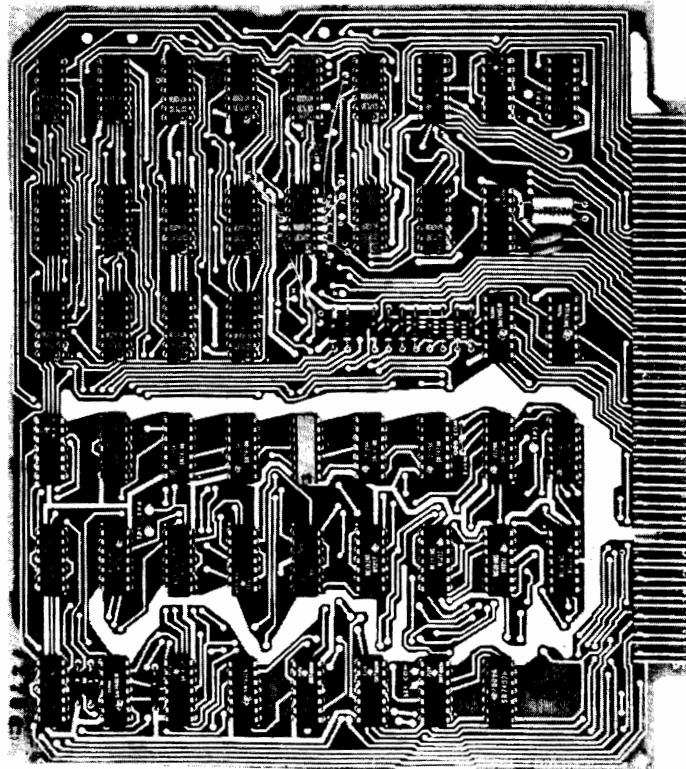
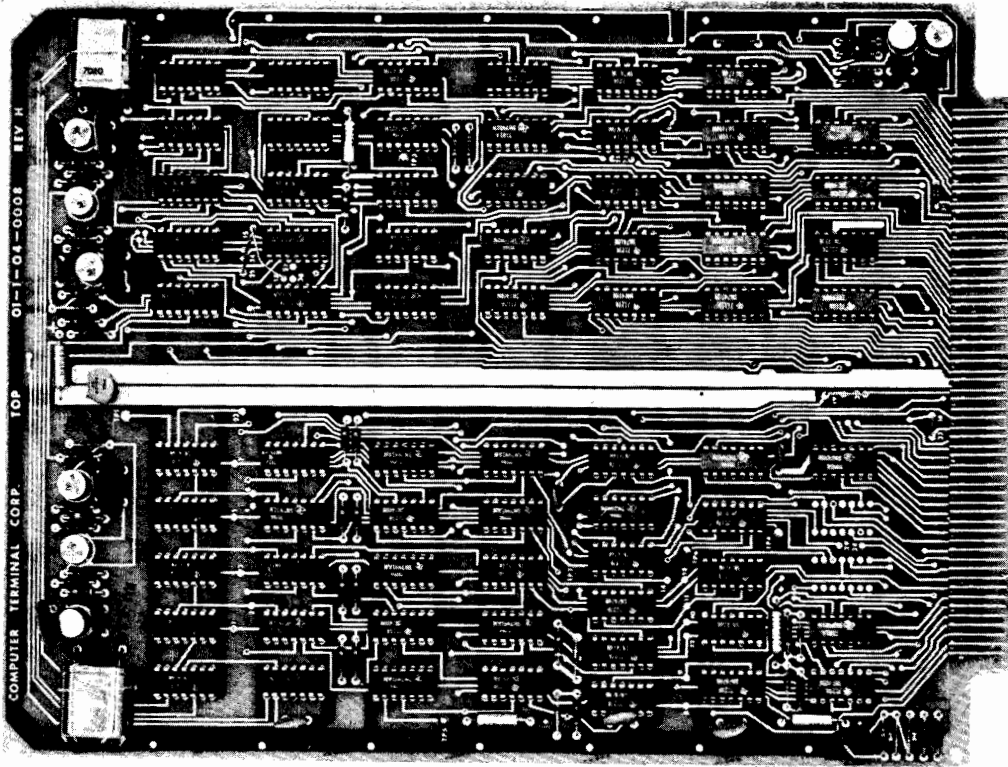


Figure 1-6. Keyboard and Answer-Back Cards

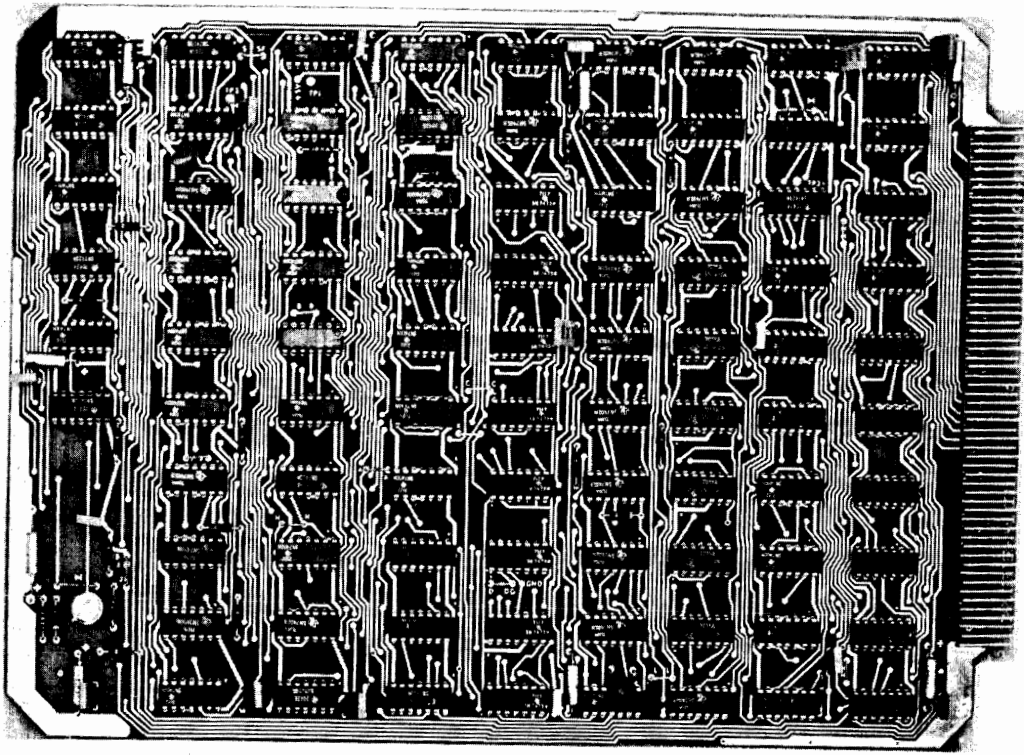
INTERFACE 2



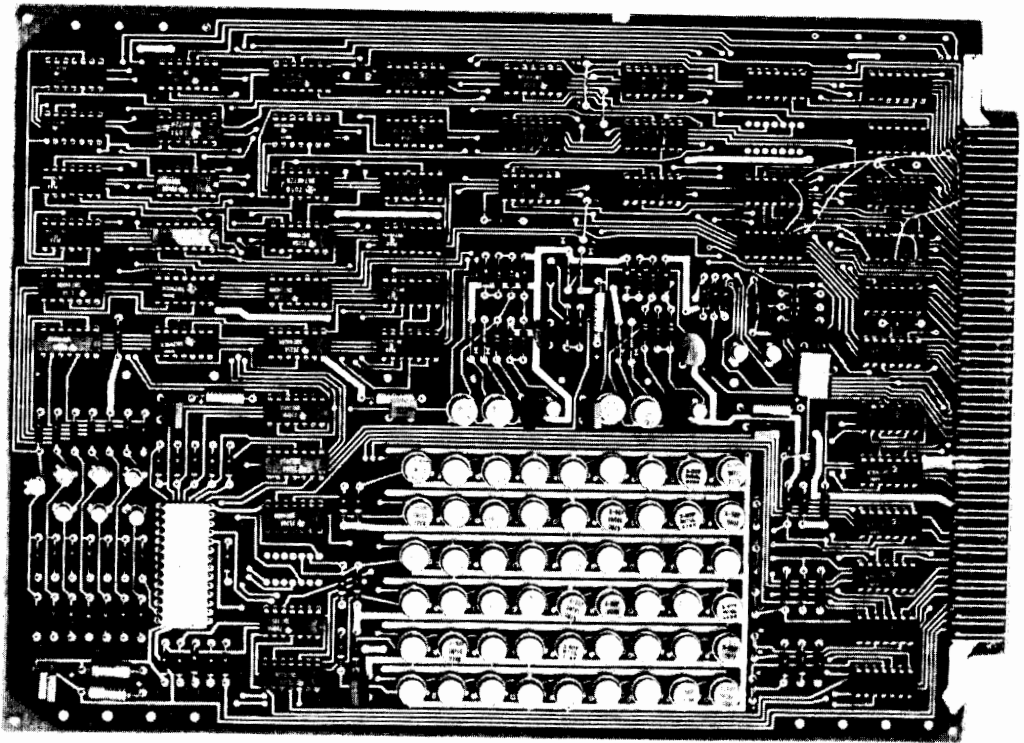
INTERFACE 1

Figure 1-7. Interface 1 and Interface 2 Cards





CONTROL LOGIC



MOS

Figure 1-8. Control Logic and MOS Cards

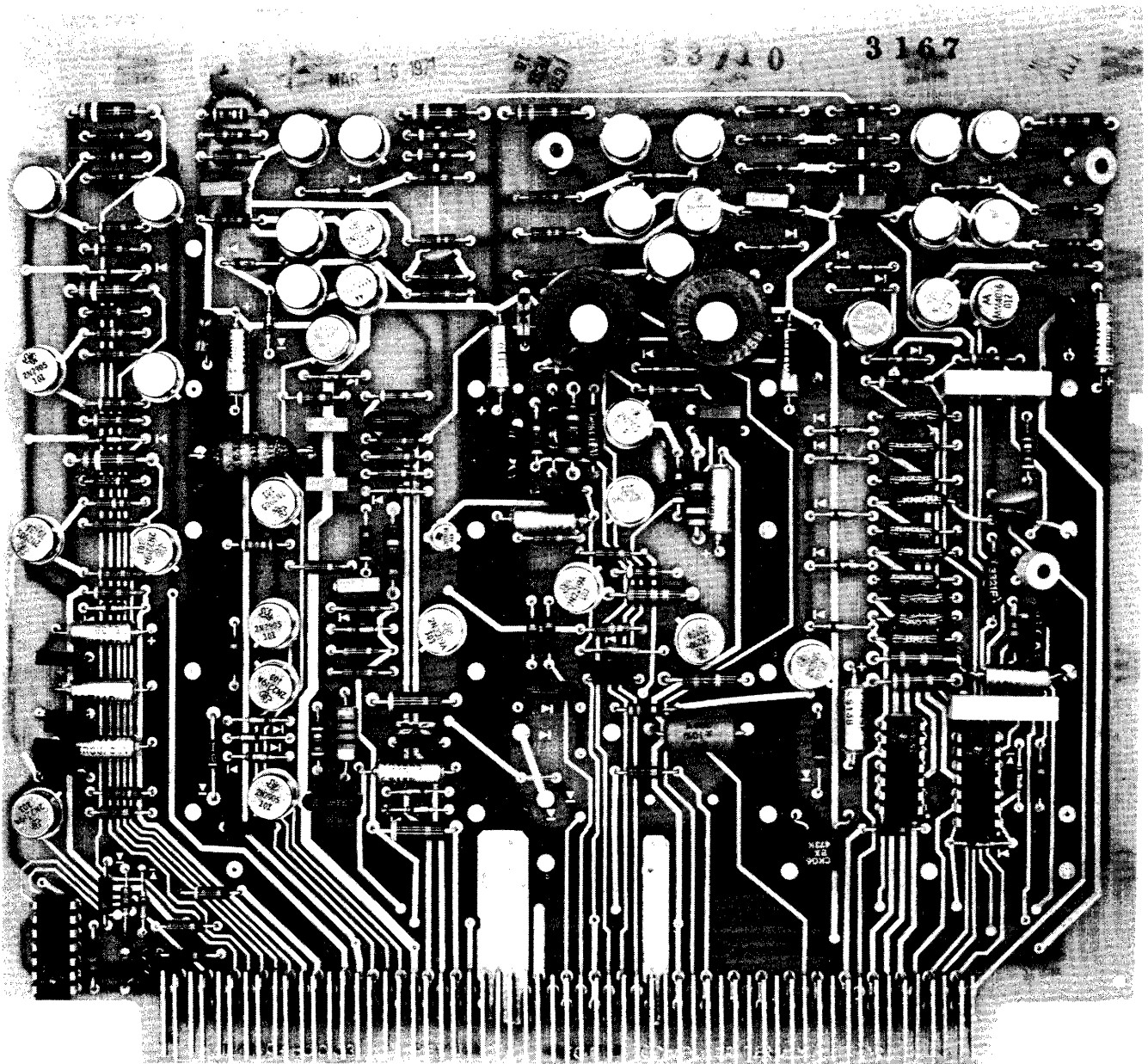


Figure 1-9. Deflection Amplifier Card



# THEORY OF OPERATION

## SECTION II

### General

The Theory of Operation presented in this section is provided to acquaint the technician with the overall functions and then explain, in detail, functions contained on each card of the terminal. References to particular block diagrams, logic diagrams or schematics should further aid in understanding the operation being explained.

The Data Logic portion will primarily deal with those circuits used in processing data. The Control Logic portion will primarily deal with all of the control functions. References to other sections are noted where inter-relation with another function is explained.

### DATA LOGIC

#### General

The Datapoint 3300 as a complete operational unit consists of two main sections (transmit and receive), power supplies and interface timing. The transmit and receive functions will be covered as separate functions to familiarize the technician with the overall operation of the data terminal. Interface timing and power supplies will be explained in the detailed explanations of the various circuits and printed circuit cards. Reference to figure 2-1 will assist in better understanding the transmit and receive functions.

### TRANSMIT FUNCTION

The keyboard is normally considered the source of data to be transmitted, however, provisions have been incorporated to permit parallel data entry from any other auxiliary source, e.g. the Datapoint 3300T. The keyboard or auxiliary source provides seven parallel data bits and a strobe pulse. The strobe occurs after the data bits are stable on the output lines, typically about 600 micro-seconds. The strobe pulse starts the output clock generator that counts down the 8 times selected rate clock provided by the interface oscillator. The output of the clock

generator, loads the start space and data into the output shift register, clocks the shift register each bit time and clocks the parity generator during each bit time. During the eighth bit time, the proper parity bit is inserted to produce an even parity followed by either one or two stop marks, depending upon the speed selected. The data is fed serially to the line buffer, located on the deflection card. This circuit converts the digital data signal into the bipolar signal defined in EIA RS-232-B. (See Table 1-1)

Digital data is tapped off the Output Buffer input and connected to the LOCAL/REMOTE and DUPLEX switches. When in Local or Half Duplex mode, digital data is sent to the Receive section and ORed with the data, if any, from the Input Buffer. Transmitted data appears on pin 2 of connector J9.

The Answer-Back optional feature is considered a part of the transmit function. Answer-Back consists of an eleven bit shift register that cycles two times when triggered by receipt of a control "E" or by depressing the HERE IS key on the keyboard. The output of the Answer-Back card is wired to the keyboard matrix to produce a sequential output the same as if the keys were depressed in that sequence.

Depressing the BREAK key generates a space condition on the output line. On early models, the space condition was maintained on the output line as long as the BREAK key was held depressed, however the later models will only provide approximately a 200 milli-second break on the output line for each time the BREAK key is depressed.

In order to repeat a character, the REPEAT key and any other alpha or numeric key must be depressed. This action starts the Repeat Generator which creates keyboard strobes at 7.5 PPS. These repeat pulses are ORed through the same path as the normal keyboard strobe pulses.

## RECEIVE FUNCTION

The bipolar EIA RS-232-B signal enters the Datapoint 3300 at Pin 3 of connector J9. The Input Buffer converts this bipolar data to standard logic levels. (1 = high or +5V, 0 = low or 0 volts).

The negative going transition of the start space causes the input bit chopper to start shifting the data into the input shift register. When a full character has been shifted into the register, a flag is raised to the comparator and the data is passed in parallel through the Speed Buffer, if available, into the input hold register.

The Speed Buffer is a circulating memory to provide temporary storage for characters while the trace is returning to the compare or cursor position. The Speed Buffer is only necessary when the input character time is less than the frame time or 16.6 milli-seconds. The Speed Buffer would be required for all data rates above 60 char/sec.

When the compare does occur, the contents of the input hold register is loaded into the circulating memory. When a compare is generated in response to a flag from the input shift register, the circulating data is inhibited at the OR gate to the memory and replaced by the new data.

The circulating memory is driven by a two phase clock at a 135 KHz rate. The two clocks are derived from the cycle generator and converted to MOS compatible levels by the MOS clock drivers. The period between clocks is 7.5 micro-seconds; therefore, the six parallel bits in the circulating memory are present for this period at the address input to the Read Only Memory (ROM). The six bit character actually defines a block address in the memory or a starting address from which five sequential addresses will be read. The cycle generator provides five sequential pulses to the ROM which causes the five 7 bit words to be read out. Each word represents one column of the 5 x 7 character matrix. While each 7 bit word is present at the ROM output, the dot generator scans each bit position and produces a digital pulse for each "one" present in the word. This pulse is applied to the

video amplifier and becomes a visible dot on the cathode ray tube (CRT).

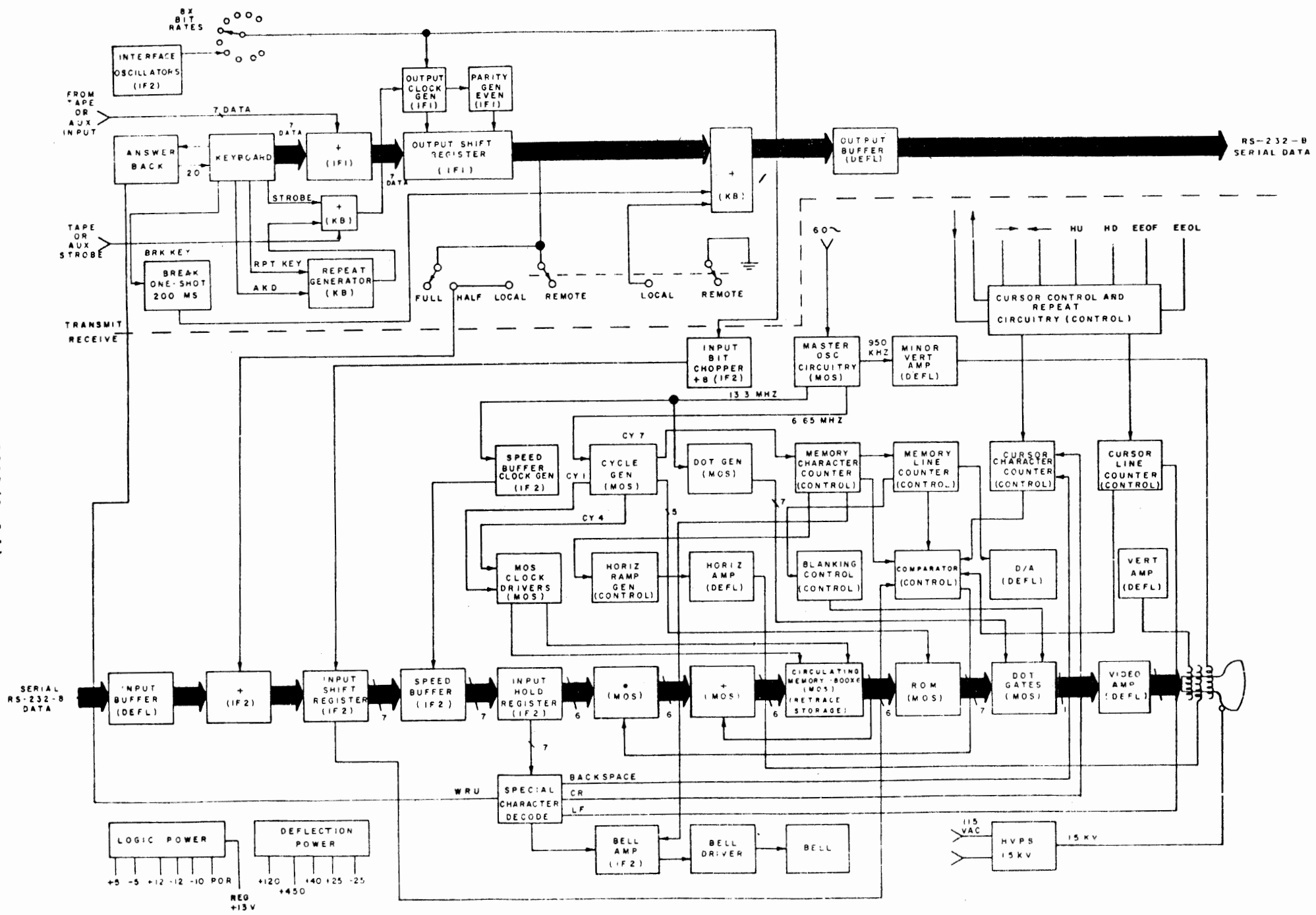
The dots are positioned on the CRT by three yoke windings. The horizontal winding controls the lateral position of the character and is modulated by the minor vertical sweep which controls the individual dot positions. The vertical sweep controls the line position on the CRT. Digital pulses from the memory character counter supply the input for the horizontal ramp generator. The horizontal ramp is generated on the control logic board and passed to the horizontal amplifier on the deflection card. The actual power drivers for each deflection winding are located on heat sinks on the rear panel assembly. A 950 KHz digital signal is the source of the minor vertical deflection which is sometimes referred to as the WRITE deflection. The output of the vertical amplifier for any given line is a constant current level. The current level is controlled by the Digital-to-Analog (D/A) converter which receives its digital input from the memory line counter on the control logic card.

The source for all timing is the master oscillator located on the MOS card. The circuit is a crystal controlled 26.6 MHz oscillator. The output of the oscillator is burst synched to the line e.g. the output is shut off at the end of the frame and is not started again until the power line passes through zero volts going in the positive direction. This technique eliminates any apparent flicker in the display due to a beat between the refresh 60 Hz and the room lighting.

The special character decode monitors the input data for special control characters. The output of this gate array causes various functions to occur, such as CARRIAGE RETURN, LINE FEED, BACKSPACE, BELL, etc.

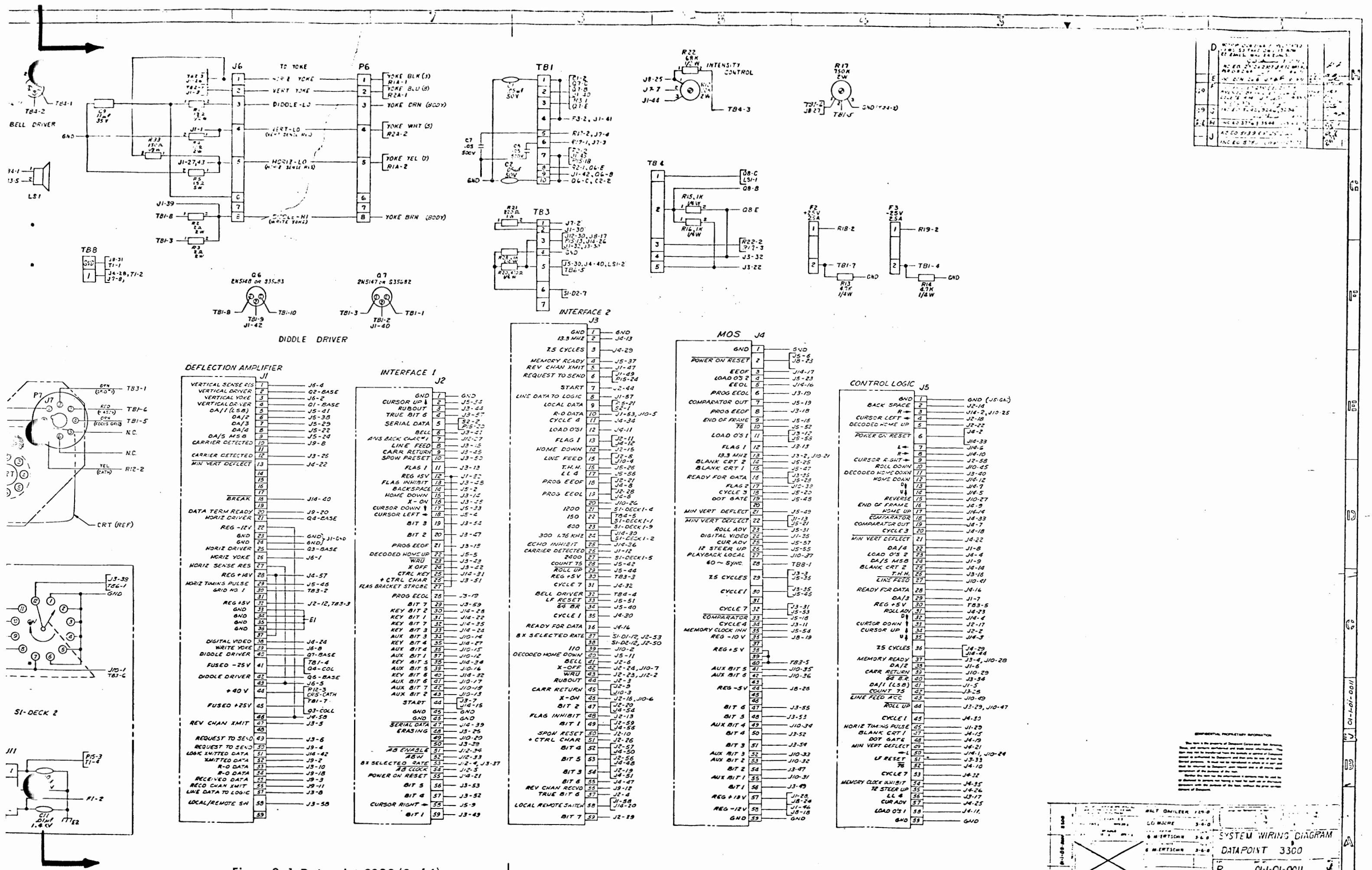
The cursor control and repeat circuitry located on the control logic card receives the inputs from the various cursor control keys located on the keyboard. This circuitry controls the cursor line and character counters.

Figure 2-1. Datapoint 3300 (1 of 4)



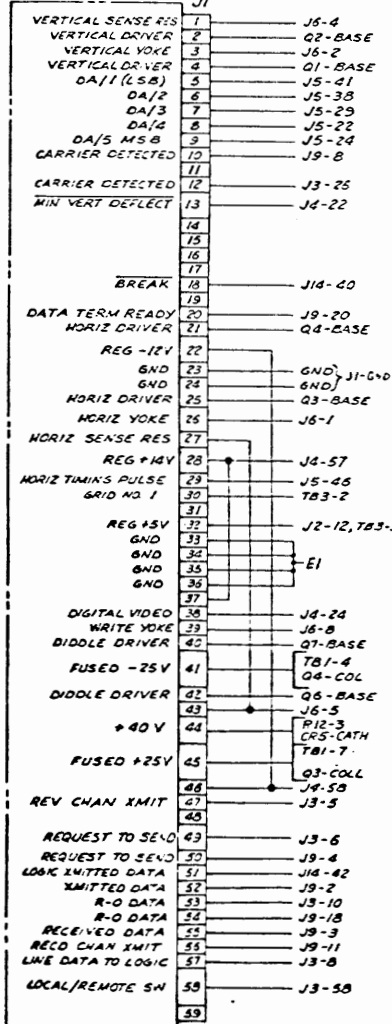




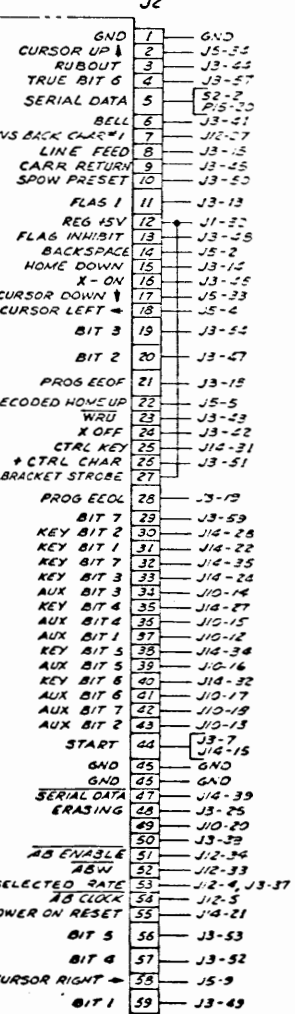


D	1	2	3	4	5	6	7	8	9	10
E	11	12	13	14	15	16	17	18	19	20
F	21	22	23	24	25	26	27	28	29	30
G	31	32	33	34	35	36	37	38	39	40
H	41	42	43	44	45	46	47	48	49	50
I	51	52	53	54	55	56	57	58	59	60
J	61	62	63	64	65	66	67	68	69	70

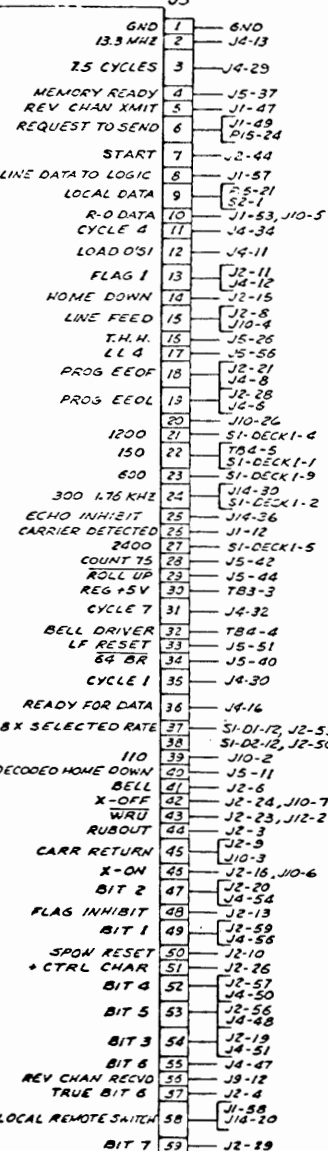
**DEFLECTION AMPLIFIER**



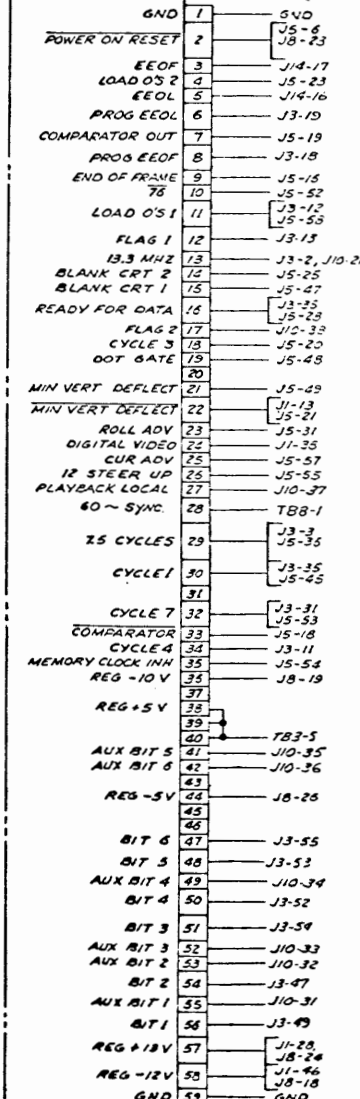
**INTERFACE 1**



**INTERFACE 2**



**MOS**



**CONTROL LOGIC**

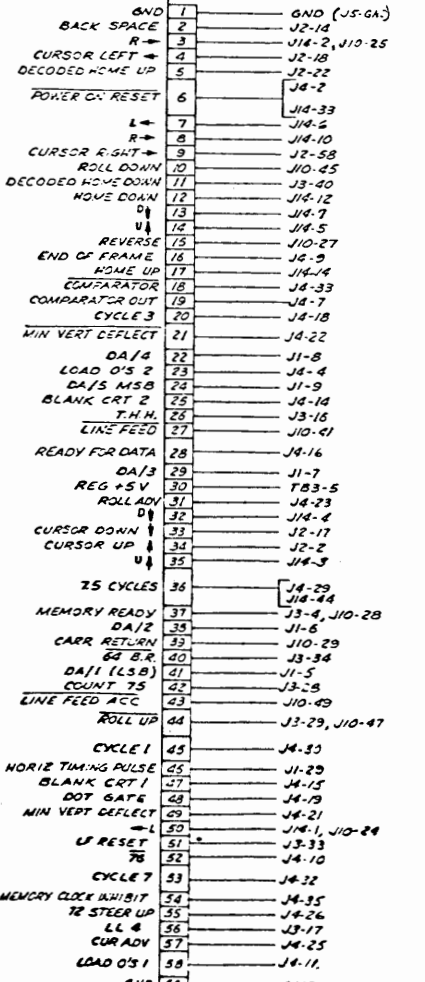


Figure 2-1. Datapoint 3300 (2 of 4)

WALT DANILEWICZ 125-0  
 LO MOCRE 3-4-0  
 MIENTSCH 3-6-0  
 MIENTSCH 3-6-0  
 J. C. STEW 74-0

**SYSTEM WIRING DIAGRAM**  
 DATAPoint 3300  
 R 01-01-001



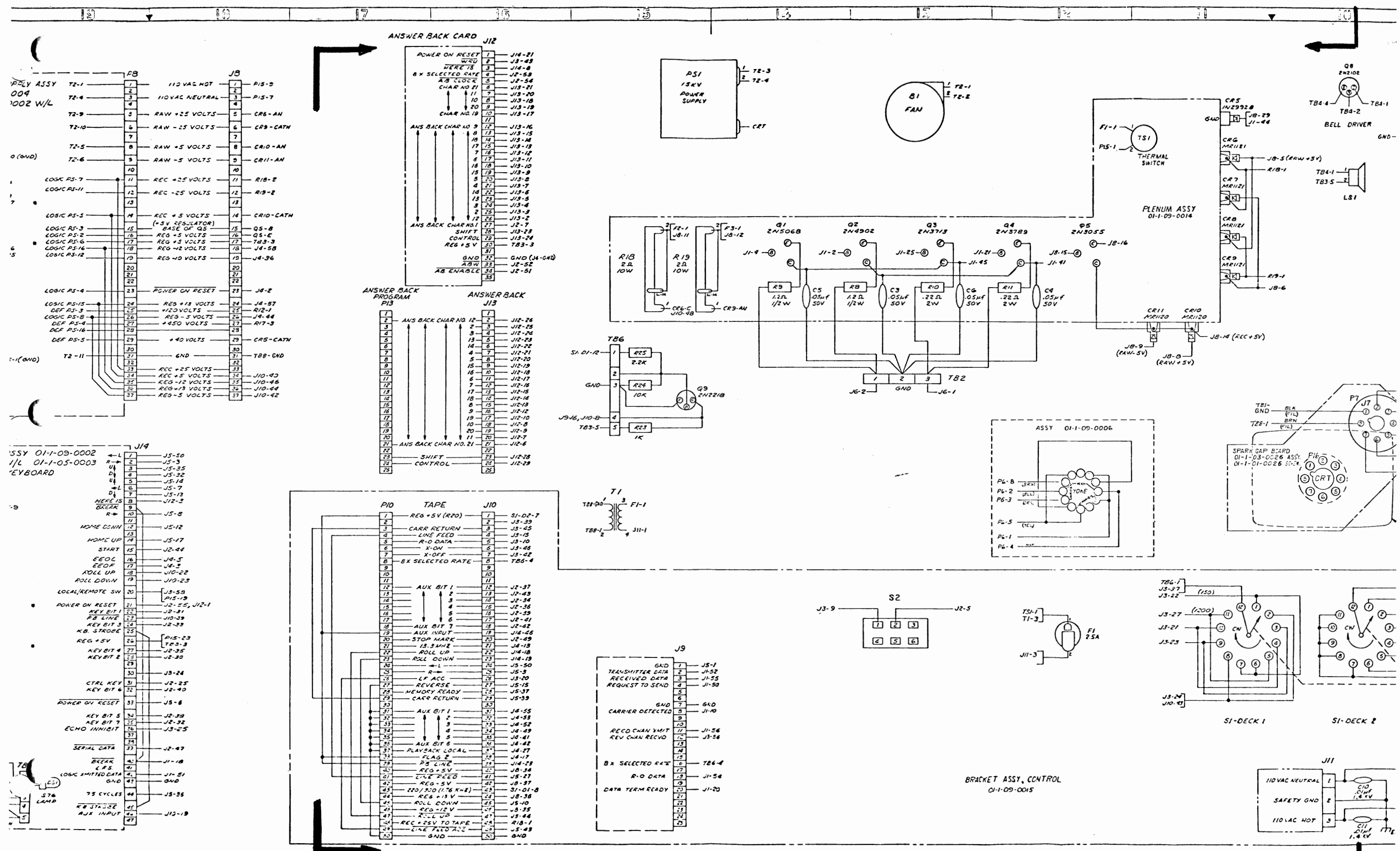


Figure 2-1 Diagram 2200 (2 of 4)

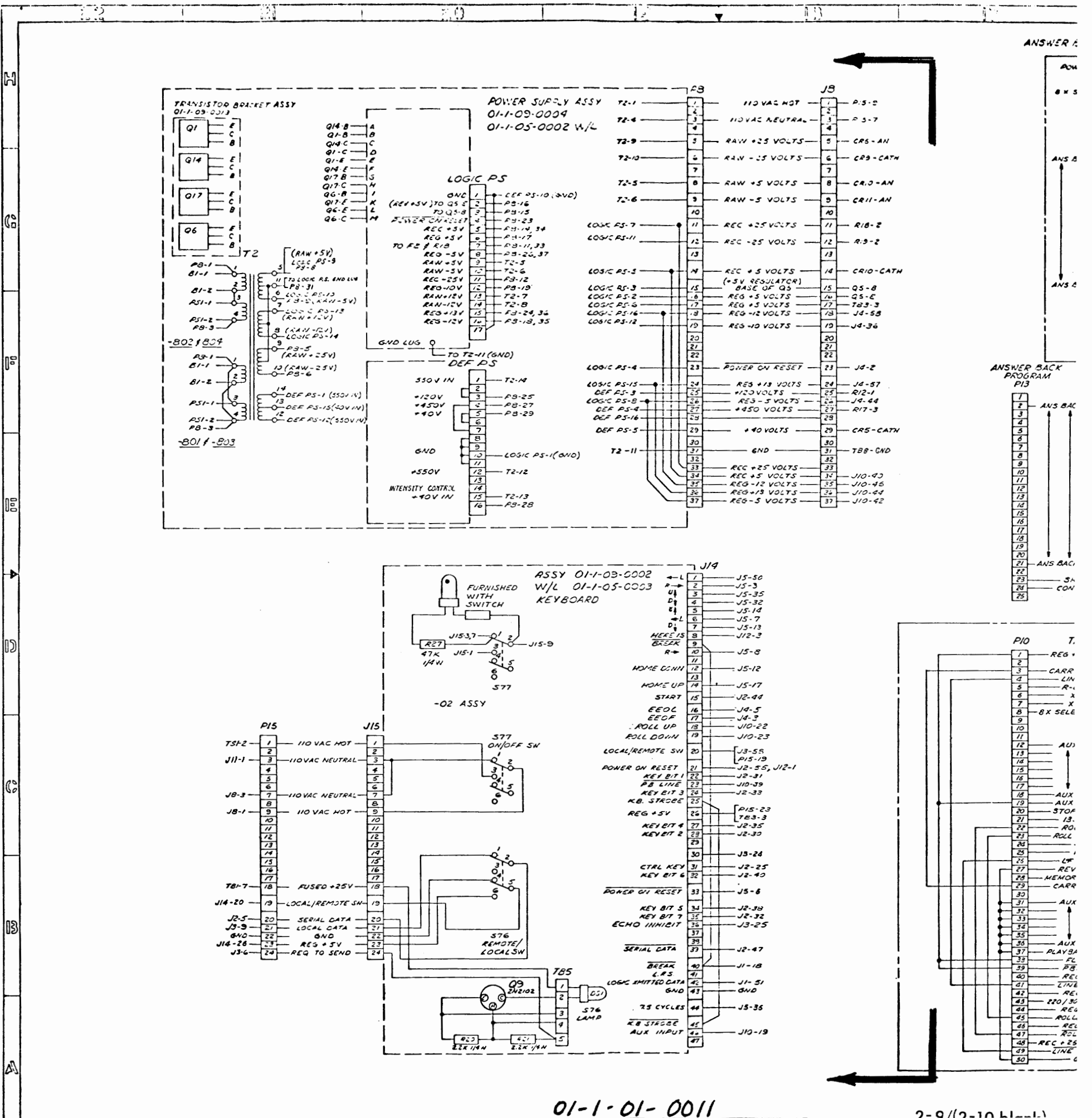


Figure 2-1. Datapoint 3300 (4 of 4)

01-1-01-0011

2-9(2-10) (1-1)

## KEYBOARD

The keyboard consists of 75 hermetically sealed magnetic reed switches that initiate the generation of numbers, letters or control function signals. The magnetic reed switches, the diode matrix and the other associated circuitry are mounted on the Keyboard printed circuit card.

The unique roll-over feature, which allows characters to be printed on the downward movement of the key is accomplished by capacitively coupling the switch closure into the diode matrix. A typical switch circuit is shown in figure 2-2.

When the key is depressed, the voltage on the capacitor at the key side is changed from 5V to 0V; therefore, there is a 5V change on the matrix side of the capacitor. The two diodes in series ensure that the 5V change will drive the resulting pulse below ground. This will compensate for the diode drop in the matrix.

Refer to the Keyboard Block Diagram figure 2-3 to follow the keyboard theory of operation. Figure 2-4, Keyboard Schematic Diagram, is provided for details of the keyboard circuit.

There are seven data bit lines coming out of matrix. The pulses on the bit lines are negative going pulses when the line is active or when the bit is a "one". The pulse duration is approximately 400 micro-seconds. These bit lines are applied to a latching register. The purpose of

this register is to eliminate the effects of switch contact bounce. At the same time that the bounce register is latching, Z13 is starting the timing generator, Z16.

The timing generator is driven by the 1.76 KHz clock and produces two sequential pulses that are spaced approximately 570 micro-seconds apart. The first pulse, created by Z7 and inverted and driven by Z14, loads the contents of the bounce register into the holding register. The hold register is loaded on the rising leading edge of the first pulse. The second pulse occurs approximately 570 micro-seconds later and is gated through Z15, Z17 and Z14 to become the output strobe pulse. This pulse goes to the interface circuitry indicating that new data is available in the hold register. The OR gate, Z17 is used to combine possible strobes from the keyboard, tape cassette unit or the repeat generator, Z12. The repeat generator (Z12) generates continuous strobes at 7.5 PPS whenever it is enabled by Z6 which is the NAND of the Repeat key and the AKD signal from Z7.

The second pulse occurs a minimum of 570 micro-seconds after the first pulse (long after the switch bounce has decayed) and resets the bounce register. This is accomplished by Z15. The timing generator is now in its static condition awaiting the depression of another key to restart the operation.

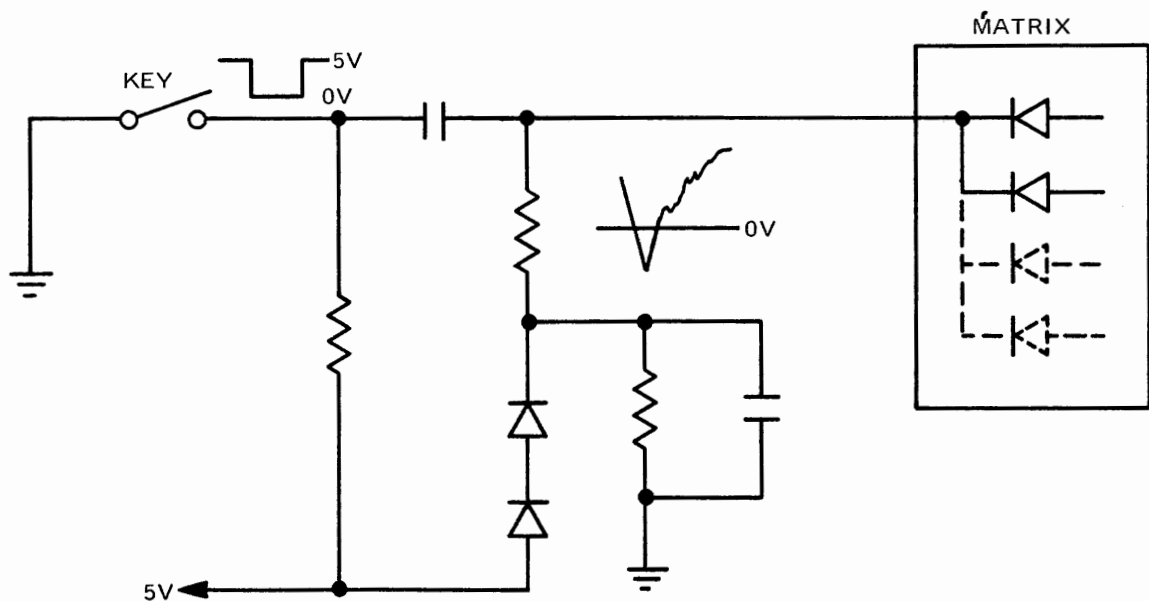


Figure 2-2. Typical Switch Circuit

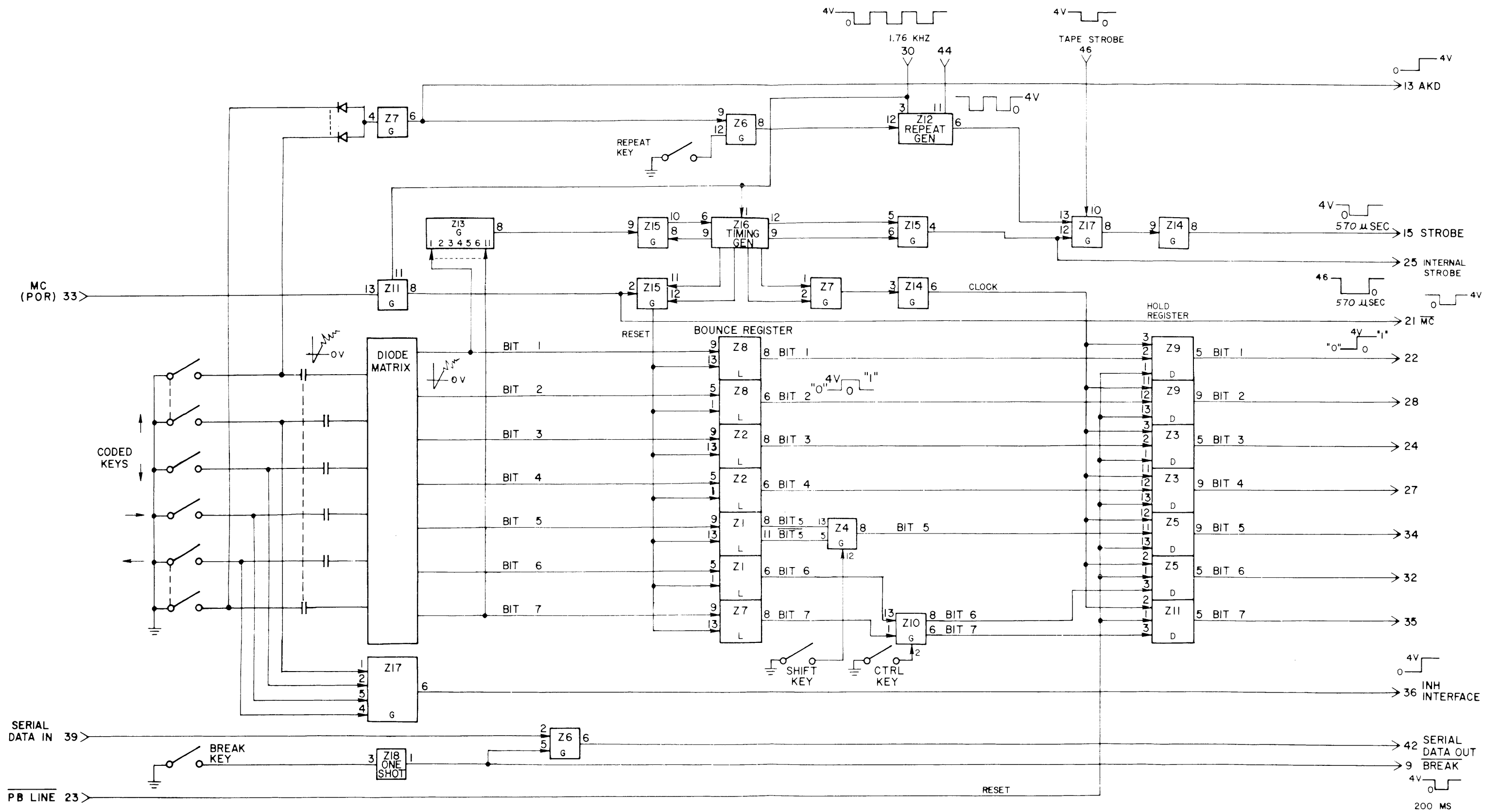


Figure 2-3. Block Diagram, Keyboard

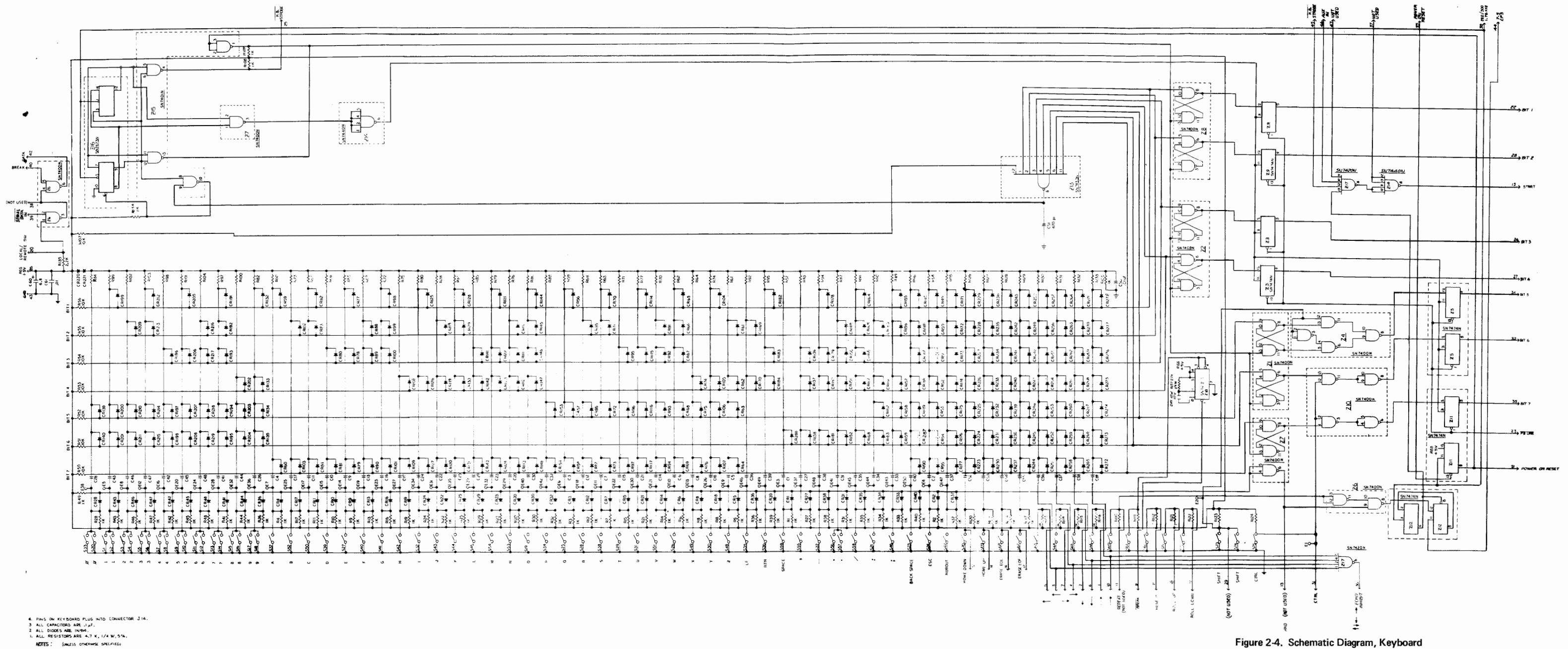


Figure 2-4. Schematic Diagram, Keyboard

When the contents of the bounce register is transferred to the hold register, bits 1 through 4 are transferred direct. Bits 5, 6 and 7 pass through gate arrays for possible modification. If the shift key is depressed, bit 5 is complemented by Z4 before it is stored in the hold register, thus creating the shifted character code. If the CTRL key is depressed, Z10 causes bits 6 and 7 to be stored into the hold register as "zeros", thus creating the control code.

The four cursor directional arrow keys are ORed through Z17 and driven to the interface circuitry on pin 36 to provide echo inhibit when these keys are depressed. When the coded cursor option is incorporated, this signal ensures that the cursor will not move more than one position due to echo-back of the same character from the computer.

The one-shot, Z18, is used to create a timed break pulse of approximately 200 milli-seconds. This pack is not present on all keyboards. When this pack is not present, the break signal remains as long as the key is held down. The break signal is ORed with serial data from the interface card by Z6 and is driven out on pin 42 to the interface buffer located on the deflection card.

## ANSWER-BACK

Answer-Back is a 21 character message option used for automatic terminal identification. The Answer-Back is similar to the mechanical answer-back wheel available on some teleprinter devices.

Twenty of the characters are programmable to establish the code for each specific terminal. The functional block diagram explained here is shown in figure 2-5. Figure 2-6 Answer-Back Schematic shows the details of this function.

The Answer-Back is started by the depressing of the HERE IS key causing a low at pin 3 or the receipt of a WRU (Control E) causing a pulse at pin 2. Either of these will cause Z6 pin 3 to go

low, which clocks the first JK flip-flop of the start control. The start control issues the "start initialize pulse" from Z20 pin 4. This pulse ensures that the circuit is ready to begin in the correct sequence and issues character number one by setting the D flip-flop Z7. The first character of the Answer-Back is always a suppress character.

The output of the JK flip-flop Z4 pin 13 is gated with the AB ENABLE clock from the Interface 1 card by Z1. The output of Z1 pin 3 is inverted by Z2 to enable the first ten (actually characters 2 thru 11) character gates. The shift register is clocked, from the Interface 1 card, once each character time by AB CLOCK. The phasing of AB ENABLE and AB CLOCK is such that after each shift time, the JK flip-flop Z4 is clocked. When the shift register reaches the last stage, Z12 pin 9 enables Z4 and the flip-flop changes state. The output of Z4 at pin 12 is gated with the AB ENABLE by Z1 and inverted by Z2 to enable the second set of characters (characters 12 through 21). When the shift register reaches the end and Z12 pin 9 allows Z4 to change states, pin 13 will enable Z13 pin 13 so that on the next AB CLOCK, Z13 pin 12 goes low and is ORed with the master clear (MC), which is the same as power on reset (POR). The output of Z6 pin 6 goes low and resets the start control at Z3 pin 2.

## Programming the Answer - Back

Programming the Answer-Back is a two part operation:

1. Programming the Answer-Back card.
2. Programming the cable from the Answer-Back card to the Keyboard.

Figure 3-8 is an example of the Answer-Back Coding Table used to determine where the jumpers should be installed for a particular Answer-Back program. Referring to figure 3-8, assume the Answer-Back to be programmed will read: return, Computer \* Terminal, return, control J. Enter this in the fifth blank line down, marked customer fill-in.

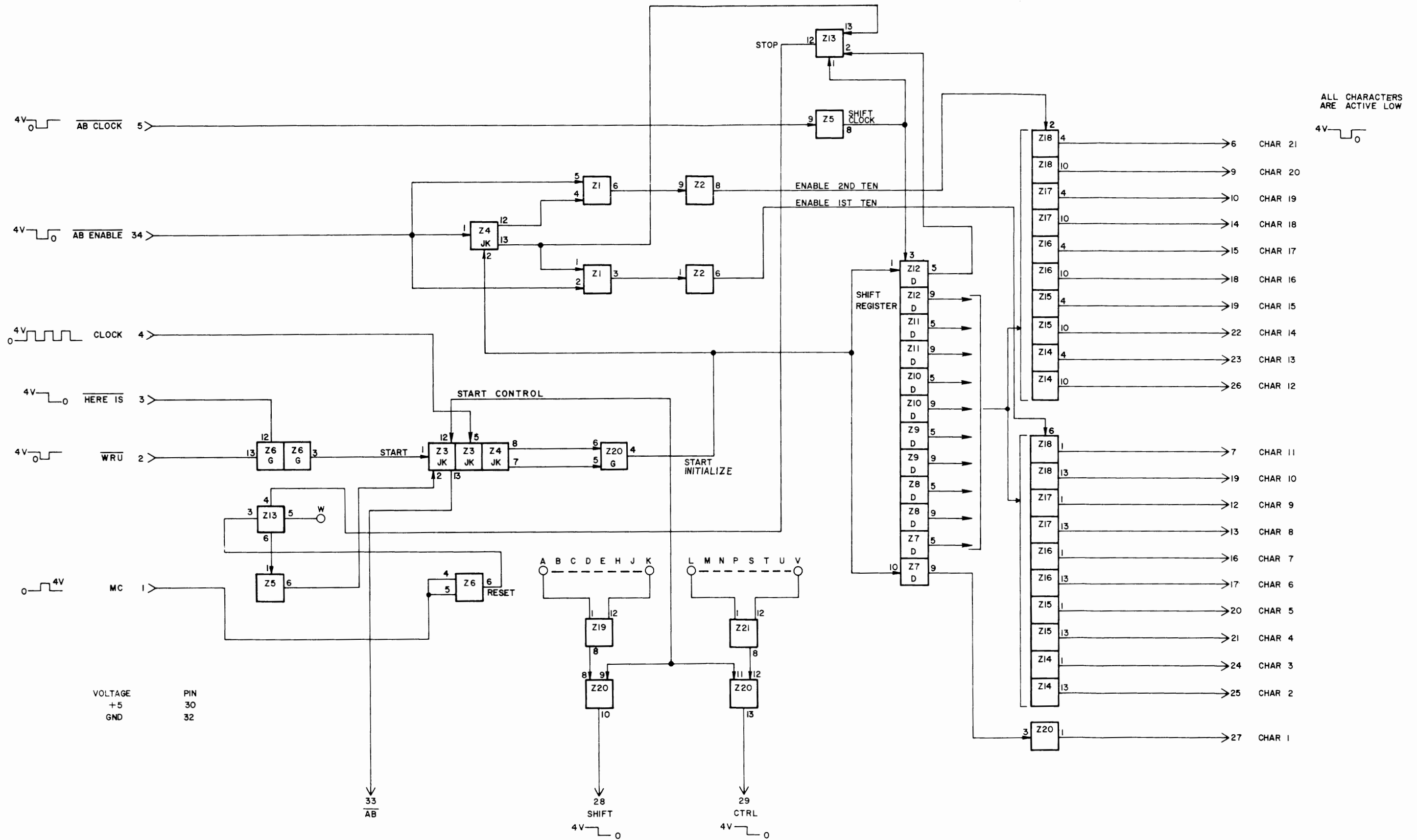
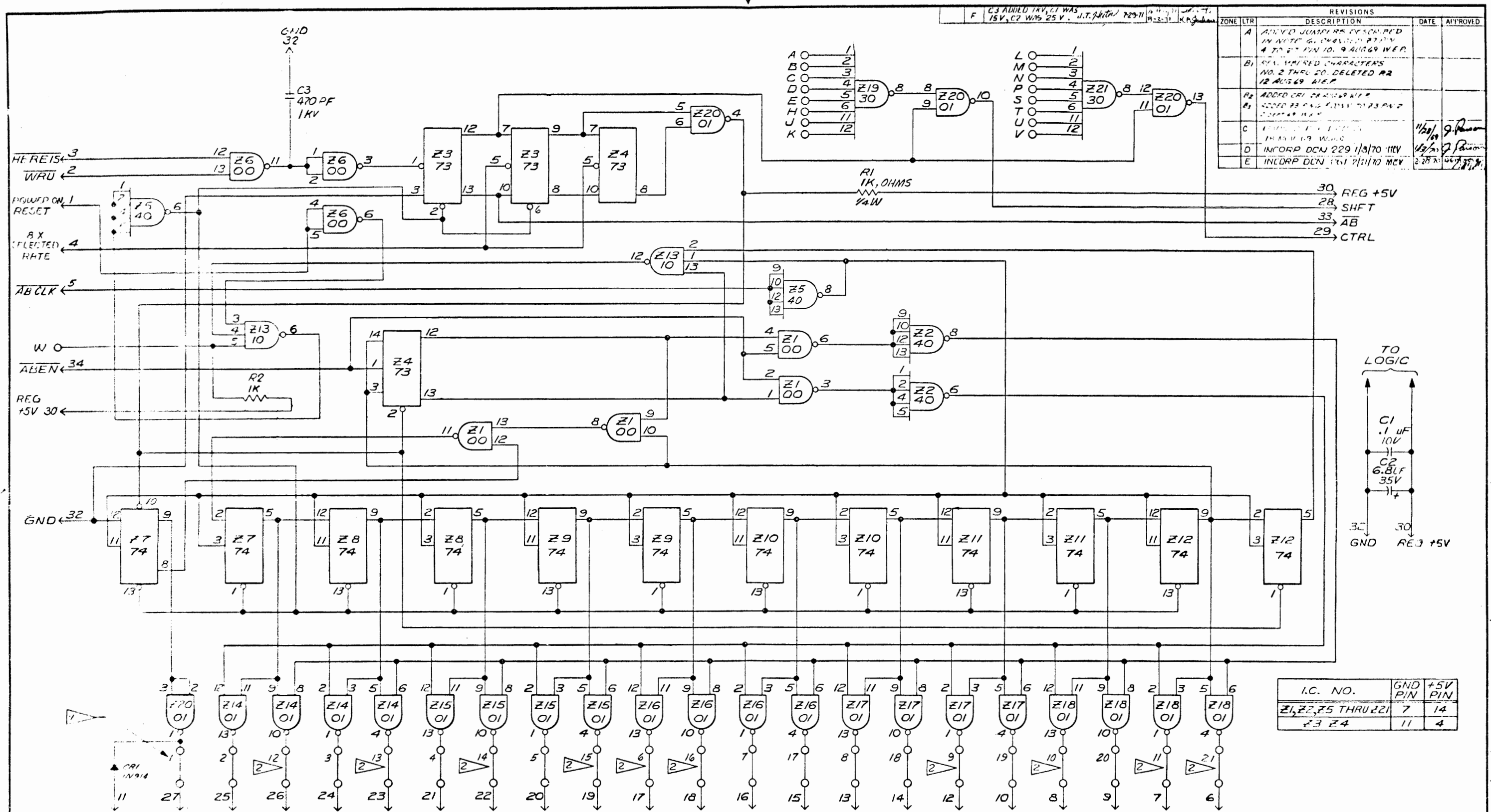


Figure 2-5. Block Diagram, Answer-Back

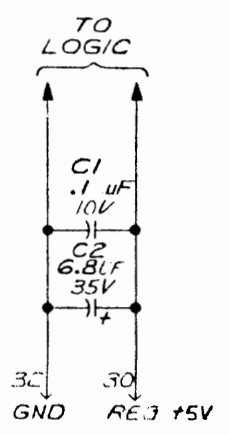




F C3 ADDED 1KV, C1 WAS 15V, C2 WAS 25V. J.T. Akita 72971

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		ADDED JUMPS AS DESCRIBED IN NOTE 6. CHANGED PINS 4 TO 27 PIN 10. 9 AUG 69 W.E.P.		
B		51A, 51B, 51C, 51D, 51E, 51F, 51G, 51H, 51I, 51J, 51K, 51L, 51M, 51N, 51O, 51P, 51Q, 51R, 51S, 51T, 51U, 51V, 51W, 51X, 51Y, 51Z, 51AA, 51AB, 51AC, 51AD, 51AE, 51AF, 51AG, 51AH, 51AI, 51AJ, 51AK, 51AL, 51AM, 51AN, 51AO, 51AP, 51AQ, 51AR, 51AS, 51AT, 51AU, 51AV, 51AW, 51AX, 51AY, 51AZ, 51BA, 51BB, 51BC, 51BD, 51BE, 51BF, 51BG, 51BH, 51BI, 51BJ, 51BK, 51BL, 51BM, 51BN, 51BO, 51BP, 51BQ, 51BR, 51BS, 51BT, 51BU, 51BV, 51BW, 51BX, 51BY, 51BZ, 51CA, 51CB, 51CC, 51CD, 51CE, 51CF, 51CG, 51CH, 51CI, 51CJ, 51CK, 51CL, 51CM, 51CN, 51CO, 51CP, 51CQ, 51CR, 51CS, 51CT, 51CU, 51CV, 51CW, 51CX, 51CY, 51CZ, 51DA, 51DB, 51DC, 51DD, 51DE, 51DF, 51DG, 51DH, 51DI, 51DJ, 51DK, 51DL, 51DM, 51DN, 51DO, 51DP, 51DQ, 51DR, 51DS, 51DT, 51DU, 51DV, 51DW, 51DX, 51DY, 51DZ, 51EA, 51EB, 51EC, 51ED, 51EE, 51EF, 51EG, 51EH, 51EI, 51EJ, 51EK, 51EL, 51EM, 51EN, 51EO, 51EP, 51EQ, 51ER, 51ES, 51ET, 51EU, 51EV, 51EW, 51EX, 51EY, 51EZ, 51FA, 51FB, 51FC, 51FD, 51FE, 51FF, 51FG, 51FH, 51FI, 51FJ, 51FK, 51FL, 51FM, 51FN, 51FO, 51FP, 51FQ, 51FR, 51FS, 51FT, 51FU, 51FV, 51FW, 51FX, 51FY, 51FZ, 51GA, 51GB, 51GC, 51GD, 51GE, 51GF, 51GG, 51GH, 51GI, 51GJ, 51GK, 51GL, 51GM, 51GN, 51GO, 51GP, 51GQ, 51GR, 51GS, 51GT, 51GU, 51GV, 51GW, 51GX, 51GY, 51GZ, 51HA, 51HB, 51HC, 51HD, 51HE, 51HF, 51HG, 51HH, 51HI, 51HJ, 51HK, 51HL, 51HM, 51HN, 51HO, 51HP, 51HQ, 51HR, 51HS, 51HT, 51HU, 51HV, 51HW, 51HX, 51HY, 51HZ, 51IA, 51IB, 51IC, 51ID, 51IE, 51IF, 51IG, 51IH, 51II, 51IJ, 51IK, 51IL, 51IM, 51IN, 51IO, 51IP, 51IQ, 51IR, 51IS, 51IT, 51IU, 51IV, 51IW, 51IX, 51IY, 51IZ, 51JA, 51JB, 51JC, 51JD, 51JE, 51JF, 51JG, 51JH, 51JI, 51JJ, 51JK, 51JL, 51JM, 51JN, 51JO, 51JP, 51JQ, 51JR, 51JS, 51JT, 51JU, 51JV, 51JW, 51JX, 51JY, 51JZ, 51KA, 51KB, 51KC, 51KD, 51KE, 51KF, 51KG, 51KH, 51KI, 51KJ, 51KK, 51KL, 51KM, 51KN, 51KO, 51KP, 51KQ, 51KR, 51KS, 51KT, 51KU, 51KV, 51KW, 51KX, 51KY, 51KZ, 51LA, 51LB, 51LC, 51LD, 51LE, 51LF, 51LG, 51LH, 51LI, 51LJ, 51LK, 51LL, 51LM, 51LN, 51LO, 51LP, 51LQ, 51LR, 51LS, 51LT, 51LU, 51LV, 51LW, 51LX, 51LY, 51LZ, 51MA, 51MB, 51MC, 51MD, 51ME, 51MF, 51MG, 51MH, 51MI, 51MJ, 51MK, 51ML, 51MM, 51MN, 51MO, 51MP, 51MQ, 51MR, 51MS, 51MT, 51MU, 51MV, 51MW, 51MX, 51MY, 51MZ, 51NA, 51NB, 51NC, 51ND, 51NE, 51NF, 51NG, 51NH, 51NI, 51NJ, 51NK, 51NL, 51NM, 51NN, 51NO, 51NP, 51NQ, 51NR, 51NS, 51NT, 51NU, 51NV, 51NW, 51NX, 51NY, 51NZ, 51OA, 51OB, 51OC, 51OD, 51OE, 51OF, 51OG, 51OH, 51OI, 51OJ, 51OK, 51OL, 51OM, 51ON, 51OO, 51OP, 51OQ, 51OR, 51OS, 51OT, 51OU, 51OV, 51OW, 51OX, 51OY, 51OZ, 51PA, 51PB, 51PC, 51PD, 51PE, 51PF, 51PG, 51PH, 51PI, 51PJ, 51PK, 51PL, 51PM, 51PN, 51PO, 51PP, 51PQ, 51PR, 51PS, 51PT, 51PU, 51PV, 51PW, 51PX, 51PY, 51PZ, 51QA, 51QB, 51QC, 51QD, 51QE, 51QF, 51QG, 51QH, 51QI, 51QJ, 51QK, 51QL, 51QM, 51QN, 51QO, 51QP, 51QQ, 51QR, 51QS, 51QT, 51QU, 51QV, 51QW, 51QX, 51QY, 51QZ, 51RA, 51RB, 51RC, 51RD, 51RE, 51RF, 51RG, 51RH, 51RI, 51RJ, 51RK, 51RL, 51RM, 51RN, 51RO, 51RP, 51RQ, 51RR, 51RS, 51RT, 51RU, 51RV, 51RW, 51RX, 51RY, 51RZ, 51SA, 51SB, 51SC, 51SD, 51SE, 51SF, 51SG, 51SH, 51SI, 51SJ, 51SK, 51SL, 51SM, 51SN, 51SO, 51SP, 51SQ, 51SR, 51SS, 51ST, 51SU, 51SV, 51SW, 51SX, 51SY, 51SZ, 51TA, 51TB, 51TC, 51TD, 51TE, 51TF, 51TG, 51TH, 51TI, 51TJ, 51TK, 51TL, 51TM, 51TN, 51TO, 51TP, 51TQ, 51TR, 51TS, 51TT, 51TU, 51TV, 51TW, 51TX, 51TY, 51TZ, 51UA, 51UB, 51UC, 51UD, 51UE, 51UF, 51UG, 51UH, 51UI, 51UJ, 51UK, 51UL, 51UM, 51UN, 51UO, 51UP, 51UQ, 51UR, 51US, 51UT, 51UU, 51UV, 51UW, 51UX, 51UY, 51UZ, 51VA, 51VB, 51VC, 51VD, 51VE, 51VF, 51VG, 51VH, 51VI, 51VJ, 51VK, 51VL, 51VM, 51VN, 51VO, 51VP, 51VQ, 51VR, 51VS, 51VT, 51VU, 51VV, 51VW, 51VX, 51VY, 51VZ, 51WA, 51WB, 51WC, 51WD, 51WE, 51WF, 51WG, 51WH, 51WI, 51WJ, 51WK, 51WL, 51WM, 51WN, 51WO, 51WP, 51WQ, 51WR, 51WS, 51WT, 51WU, 51WV, 51WW, 51WX, 51WY, 51WZ, 51XA, 51XB, 51XC, 51XD, 51XE, 51XF, 51XG, 51XH, 51XI, 51XJ, 51XK, 51XL, 51XM, 51XN, 51XO, 51XP, 51XQ, 51XR, 51XS, 51XT, 51XU, 51XV, 51XW, 51XX, 51XY, 51XZ, 51YA, 51YB, 51YC, 51YD, 51YE, 51YF, 51YG, 51YH, 51YI, 51YJ, 51YK, 51YL, 51YM, 51YN, 51YO, 51YP, 51YQ, 51YR, 51YS, 51YT, 51YU, 51YV, 51YW, 51YX, 51YY, 51YZ, 51ZA, 51ZB, 51ZC, 51ZD, 51ZE, 51ZF, 51ZG, 51ZH, 51ZI, 51ZJ, 51ZK, 51ZL, 51ZM, 51ZN, 51ZO, 51ZP, 51ZQ, 51ZR, 51ZS, 51ZT, 51ZU, 51ZV, 51ZW, 51ZX, 51ZY, 51ZZ		
B1		51A, 51B, 51C, 51D, 51E, 51F, 51G, 51H, 51I, 51J, 51K, 51L, 51M, 51N, 51O, 51P, 51Q, 51R, 51S, 51T, 51U, 51V, 51W, 51X, 51Y, 51Z, 51AA, 51AB, 51AC, 51AD, 51AE, 51AF, 51AG, 51AH, 51AI, 51AJ, 51AK, 51AL, 51AM, 51AN, 51AO, 51AP, 51AQ, 51AR, 51AS, 51AT, 51AU, 51AV, 51AW, 51AX, 51AY, 51AZ, 51BA, 51BB, 51BC, 51BD, 51BE, 51BF, 51BG, 51BH, 51BI, 51BJ, 51BK, 51BL, 51BM, 51BN, 51BO, 51BP, 51BQ, 51BR, 51BS, 51BT, 51BU, 51BV, 51BW, 51BX, 51BY, 51BZ, 51CA, 51CB, 51CC, 51CD, 51CE, 51CF, 51CG, 51CH, 51CI, 51CJ, 51CK, 51CL, 51CM, 51CN, 51CO, 51CP, 51CQ, 51CR, 51CS, 51CT, 51CU, 51CV, 51CW, 51CX, 51CY, 51CZ, 51DA, 51DB, 51DC, 51DD, 51DE, 51DF, 51DG, 51DH, 51DI, 51DJ, 51DK, 51DL, 51DM, 51DN, 51DO, 51DP, 51DQ, 51DR, 51DS, 51DT, 51DU, 51DV, 51DW, 51DX, 51DY, 51DZ, 51EA, 51EB, 51EC, 51ED, 51EE, 51EF, 51EG, 51EH, 51EI, 51EJ, 51EK, 51EL, 51EM, 51EN, 51EO, 51EP, 51EQ, 51ER, 51ES, 51ET, 51EU, 51EV, 51EW, 51EX, 51EY, 51EZ, 51FA, 51FB, 51FC, 51FD, 51FE, 51FF, 51FG, 51FH, 51FI, 51FJ, 51FK, 51FL, 51FM, 51FN, 51FO, 51FP, 51FQ, 51FR, 51FS, 51FT, 51FU, 51FV, 51FW, 51FX, 51FY, 51FZ, 51GA, 51GB, 51GC, 51GD, 51GE, 51GF, 51GG, 51GH, 51GI, 51GJ, 51GK, 51GL, 51GM, 51GN, 51GO, 51GP, 51GQ, 51GR, 51GS, 51GT, 51GU, 51GV, 51GW, 51GX, 51GY, 51GZ, 51HA, 51HB, 51HC, 51HD, 51HE, 51HF, 51HG, 51HH, 51HI, 51HJ, 51HK, 51HL, 51HM, 51HN, 51HO, 51HP, 51HQ, 51HR, 51HS, 51HT, 51HU, 51HV, 51HW, 51HX, 51HY, 51HZ, 51IA, 51IB, 51IC, 51ID, 51IE, 51IF, 51IG, 51IH, 51II, 51IJ, 51IK, 51IL, 51IM, 51IN, 51IO, 51IP, 51IQ, 51IR, 51IS, 51IT, 51IU, 51IV, 51IW, 51IX, 51IY, 51IZ, 51JA, 51JB, 51JC, 51JD, 51JE, 51JF, 51JG, 51JH, 51JI, 51JJ, 51JK, 51JL, 51JM, 51JN, 51JO, 51JP, 51JQ, 51JR, 51JS, 51JT, 51JU, 51JV, 51JW, 51JX, 51JY, 51JZ, 51KA, 51KB, 51KC, 51KD, 51KE, 51KF, 51KG, 51KH, 51KI, 51KJ, 51KL, 51KM, 51KN, 51KO, 51KP, 51KQ, 51KR, 51KS, 51KT, 51KU, 51KV, 51KW, 51KX, 51KY, 51KZ, 51LA, 51LB, 51LC, 51LD, 51LE, 51LF, 51LG, 51LH, 51LI, 51LJ, 51LK, 51LM, 51LN, 51LO, 51LP, 51LQ, 51LR, 51LS, 51LT, 51LU, 51LV, 51LW, 51LX, 51LY, 51LZ, 51MA, 51MB, 51MC, 51MD, 51ME, 51MF, 51MG, 51MH, 51MI, 51MJ, 51MK, 51ML, 51MM, 51MN, 51MO, 51MP, 51MQ, 51MR, 51MS, 51MT, 51MU, 51MV, 51MW, 51MX, 51MY, 51MZ, 51NA, 51NB, 51NC, 51ND, 51NE, 51NF, 51NG, 51NH, 51NI, 51NJ, 51NK, 51NL, 51NM, 51NN, 51NO, 51NP, 51NQ, 51NR, 51NS, 51NT, 51NU, 51NV, 51NW, 51NX, 51NY, 51NZ, 51OA, 51OB, 51OC, 51OD, 51OE, 51OF, 51OG, 51OH, 51OI, 51OJ, 51OK, 51OL, 51OM, 51ON, 51OO, 51OP, 51OQ, 51OR, 51OS, 51OT, 51OU, 51OV, 51OW, 51OX, 51OY, 51OZ, 51PA, 51PB, 51PC, 51PD, 51PE, 51PF, 51PG, 51PH, 51PI, 51PJ, 51PK, 51PL, 51PM, 51PN, 51PO, 51PP, 51PQ, 51PR, 51PS, 51PT, 51PU, 51PV, 51PW, 51PX, 51PY, 51PZ, 51QA, 51QB, 51QC, 51QD, 51QE, 51QF, 51QG, 51QH, 51QI, 51QJ, 51QK, 51QL, 51QM, 51QN, 51QO, 51QP, 51QQ, 51QR, 51QS, 51QT, 51QU, 51QV, 51QW, 51QX, 51QY, 51QZ, 51RA, 51RB, 51RC, 51RD, 51RE, 51RF, 51RG, 51RH, 51RI, 51RJ, 51RK, 51RL, 51RM, 51RN, 51RO, 51RP, 51RQ, 51RR, 51RS, 51RT, 51RU, 51RV, 51RW, 51RX, 51RY, 51RZ, 51SA, 51SB, 51SC, 51SD, 51SE, 51SF, 51SG, 51SH, 51SI, 51SJ, 51SK, 51SL, 51SM, 51SN, 51SO, 51SP, 51SQ, 51SR, 51SS, 51ST, 51SU, 51SV, 51SW, 51SX, 51SY, 51SZ, 51TA, 51TB, 51TC, 51TD, 51TE, 51TF, 51TG, 51TH, 51TI, 51TJ, 51TK, 51TL, 51TM, 51TN, 51TO, 51TP, 51TQ, 51TR, 51TS, 51TT, 51TU, 51TV, 51TW, 51TX, 51TY, 51TZ, 51UA, 51UB, 51UC, 51UD, 51UE, 51UF, 51UG, 51UH, 51UI, 51UJ, 51UK, 51UL, 51UM, 51UN, 51UO, 51UP, 51UQ, 51UR, 51US, 51UT, 51UU, 51UV, 51UW, 51UX, 51UY, 51UZ, 51VA, 51VB, 51VC, 51VD, 51VE, 51VF, 51VG, 51VH, 51VI, 51VJ, 51VK, 51VL, 51VM, 51VN, 51VO, 51VP, 51VQ, 51VR, 51VS, 51VT, 51VU, 51VV, 51VW, 51VX, 51VY, 51VZ, 51WA, 51WB, 51WC, 51WD, 51WE, 51WF, 51WG, 51WH, 51WI, 51WJ, 51WK, 51WL, 51WM, 51WN, 51WO, 51WP, 51WQ, 51WR, 51WS, 51WT, 51WU, 51WV, 51WW, 51WX, 51WY, 51WZ, 51XA, 51XB, 51XC, 51XD, 51XE, 51XF, 51XG, 51XH, 51XI, 51XJ, 51XK, 51XL, 51XM, 51XN, 51XO, 51XP, 51XQ, 51XR, 51XS, 51XT, 51XU, 51XV, 51XW, 51XX, 51XY, 51XZ, 51YA, 51YB, 51YC, 51YD, 51YE, 51YF, 51YG, 51YH, 51YI, 51YJ, 51YK, 51YL, 51YM, 51YN, 51YO, 51YP, 51YQ, 51YR, 51YS, 51YT, 51YU, 51YV, 51YW, 51YX, 51YY, 51YZ, 51ZA, 51ZB, 51ZC, 51ZD, 51ZE, 51ZF, 51ZG, 51ZH, 51ZI, 51ZJ, 51ZK, 51ZL, 51ZM, 51ZN, 51ZO, 51ZP, 51ZQ, 51ZR, 51ZS, 51ZT, 51ZU, 51ZV, 51ZW, 51ZX, 51ZY, 51ZZ		
B2		ADDED CR1 24 25 26 27 W.E.P.		
B3		DELETED CR1 24 25 26 27 W.E.P.		
C		INCORP DCN 229 1/3/70 11EV	11/20/70	J. P. ...
D		INCORP DCN 229 1/3/70 11EV	11/20/70	J. P. ...
E		INCORP DCN 229 1/3/70 11EV	11/20/70	J. P. ...

30 REG +5V  
28 SHFT  
33 AB  
29 CTRL



I.C. NO.	GND PIN	+5V PIN
Z1, Z2, Z5 THRU Z21	7	14
Z3 Z4	11	4

2 INSTALL JUMMERS AS FOLLOWS:  
 J1 FROM Z19-12-K TO CHARACTER NO. 2.  
 J2 FROM CHARACTER NO 10 TO CHARACTER NO. 11.  
 J3 FROM Z21-1-L TO CHARACTER NO. 21.  
 J4 FROM CHARACTER NO. 5 TO CHARACTER NO. 16.  
 J5 FROM CHARACTER NO. 6 TO CHARACTER NO. 18.  
 J6 FROM CHARACTER NO. 7 TO CHARACTER NO. 20.

1 NUMBERS 1 THRU 21 DESIGNATE ANSWER BACK CHARACTERS.

3. PINS ON ANSWER BACK BOARD PLUG INTO CONNECTOR J12

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	NOMENCLATURE OR DESCRIPTION	IDENTIFYING NO.	MATERIAL OR NOTE	ITEM NO.
LIST OF MATERIALS				
	C3			
	R2			
	Z21			
	CR1			
REFERENCE DESIGNATORS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		
LAST USED NOT USED		TOLERANCE ON FRACTIONS ± 1/64 DECIMALS ± .010 ANGLES ± 1/2°		
		MATERIAL		
		DRAWN BY: J. P. ...		
		DATE: 11/20/70		
		APP'D: J. P. ...		
		APP'D: J. P. ...		
		DESIGN RELEASES		
		SIZE D		
		DWG NO. 01-1-01-0007 F		
		SCALE		
		WEIGHT		
		SHEET 1 OF 1		

Figure 2-6. Answer Back



Physically examine the Answer-Back card and determine the numbering sequence etched on the Answer-Back card near the connector. These character numbers will correspond to the line marked FROM CHARACTER NUMBER "OLD" or "NEW" on the Answer-Back Coding Table. For this example, the Answer-Back Card will have the "OLD" character number sequence. To avoid confusion, the character number sequence marked "NEW" could be lined out.

The coding above the "customer fill-in" line pertains to the coding that must be done on the Answer-Back card and everything below this line applies to the cable hook-up between the Answer-Back card and the Keyboard.

The first line moving up the form is for repeated characters. In the example, the first repeated character is "return". In the E row at the bottom of the form place a dash, and in the repeated character row place the character number of the first "return" (3) over the second "return", in this case, character number 19. This same procedure is repeated for each repeated character. A character may be repeated any number of times by strapping the proper numbers together. On the card, jumper plug in pads are available on the character number lines.

The next row up is used for shifted characters. In the example, the "\*" is a shifted character. In the shifted character row, directly above the "\*" place an A, B, C, D, E, H, J or K. These are all inputs to the shift gate Z19 on the card. If another shifted character were present, another one of the letters in the group would be chosen.

The next row up the form is for control characters. The "J" is a control character in the above example. In the CTRL CHAR row directly above the "J" place L, N, M, P, S, T, U or V. These are inputs to the control gate Z21 on the card.

This completes the card coding portion of the form. The following jumpers may now be placed on the Answer-Back card.

FROM PAD	TO PAD
2	15
5	16
6	18
9	8

FROM PAD	TO PAD
19	3
20	A
21	L

The lower portion of the form may now be completed. In the example the first character that requires an entry on the last row of the form, marked "keyboard E row", is the character "C". The procedure is to look up the character "C" in the table located below the coding form. From this table it can be determined that the character "C" corresponds to E-17 on the keyboard. Write the number 17, directly below the character "C" in the "keyboard E row" of the form. After every character has been assigned an "E" number, the cable portion of the form will be complete.

The pin numbers on the row marked "25 pin connector" are the pin numbers on an amphenol 17-304-01 or equivalent connector. This connector will mate with the male connector on the Answer-Back assembly. From the form it can be seen that the following connections must be made.

FROM CONNECTOR PIN	TO KEYBOARD E NUMBER
25	47
4	17
7	40
11	42
12	30
20	44
2	22
5	14
6	18
9	33
10	34
13	29
14	7
17	39
19	49
21	31
23	2
24	1

In the above example all 20 characters were used; however, it is not necessary to use all character positions. When the full 20 characters are not used the character position following the last character of the Answer-Back must be jumpered to pad W or pin 5 of Z13.

## INTERFACE 1

The Interface 1 card contains the transmit circuitry, which is basically a parallel to serial converter and the special character decode matrix. The functional block diagram explained here, is shown in figure 2-7. Figure 2-8 is the schematic of the Interface 1 card.

Data appears from the keyboard or tape cassette at the inputs of Z43 and Z49. After a delay of 570 micro-seconds the start strobe at pin 44 occurs. The start pulse presets the D flip-flop Z48 so that Z48 pin 9 enables the gate Z13 allowing the eight times selected rate signal at pin 53 to pass through and clock the clock generator, which is a divide by eight counter. There are four decodes off of the clock generator T1, T4, T6 and T8. The sequence of events are as follows: At T1, the bit counter is advanced and the parity generator is clocked at Z42 pin 11, if the last bit in the shift register has a one output at Z42 pin 5. T1 is inverted at pin 6 of Z25 and applied to the NAND gate Z25 pin 9. If the above conditions are met the output at Z25 pin 8 goes low. Because the parity generator is a D flip-flop, the actual clocking does not occur until the ascending edge of T1. This sequence repeats once per bit time at T1.

At T4, the data is loaded into the output shift register, if the bit counter is in the first count position. At this time, the NAND gate Z35 will be satisfied and pin 11 will be low. The inverted T4 satisfied the NOR gate Z40 causing a high output at pin 13 which loads the data through Z43 and Z49. Also at T4, the NOR gate Z40 at pin 9 is enabled. If it is bit 8 time (parity bit time), either Z19 pins 8 and 9 or 5 and 6 will be satisfied causing pin 8 of Z40 to be enabled. The 10/11 bit input at connector pin 50 is gated with the outputs of Z30 to determine the parity bit time. If an eleven bit code is being generated, the input at pin 50 will be high. This high causes the second stop bit to be added at Z25 pin 1 when the data is loaded. Also, the bit counter sequence is controlled by this high through gate Z7. The output at Z7 pin 1 causes the counter to count eleven bits and the output at Z7 pin 4 will cause a ten bit count, if the input at pin 50 was low.

Returning to the NOR gate Z40, the output at pin 10 will go high. If the output of Z42 pin 9

(the parity generator) is high, indicating that an odd number of ones have been detected at the output of the shift register, Z35 pin 8 will go low, setting a "one" into the last bit position of the shift register at Z42 pin 4, thus creating the even parity.

At T6, the shift register is advanced. T6 is generated by Z20 pin 6 and inverted by the power inverter Z14. The output of Z14 at pin 8 clocks the D flip-flops in the output shift register on the leading edge of T6. As data is shifted out of Z48 pin 5, it is inverted by Z7 so that the serial data output appears at connector pin 5 and the inverted data at pin 47.

This sequence repeats until the bit counter reaches the last count (either 10 or 11). The output of Z40 pin 1 will be high when the last count is reached. If another strobe from the keyboard or tape cassette has not been received while the previous character was being shifted out, Z8 pin 8 will be high. This allows Z13 pin 8 to go low which puts a low on the D input of Z48. When T8 occurs, Z48 pin 9 goes low and inhibits the 8 times selected rate signal from clocking the clock generator.

In the event that a second strobe did occur while the first character was being processed, the output of Z25 at pin 11 would have clocked Z8 causing pin 8 to go low. When Z8 pin 8 is low, Z48 does not receive a clock, and the input clock is not inhibited and the clock generator goes into another cycle immediately. This condition may occur during a fast two character typing sequence, e.g. T-H.

The seven data bits from the input hold register are hard wired through the decode matrix to the various gates to sense particular control characters. The backspace gate Z30 is a programmable gate. Any backspace code may be selected by jumpering the numbered pads at the input of Z30 to the proper lettered pads at the decode matrix input.

The rubout, SPOW, backspace and all of the control characters are not loaded into the memory; therefore, the flag to the MOS memory must be inhibited. The output of Z39 at pin 8 is ORed with the control character outputs on the

Interface 2 board to inhibit the flag during any of the special characters.

The automatic Space Overwrite (SPOW) is a special feature of the Datapoint 3300 and functions as follows: With each line feed character, the D flip-flops Z50 are reset and the latch Z39 is set. The first flag from the interface appearing at connector pin 11, indicating that a printable character has occurred, will reset the latch Z39 causing Z39 pin 6 to go low. This low is inverted by Z45 and clocks D flip-flop Z50 so that Z50 pin 5 goes high enabling the D flip-flop Z50 at

pin 12. When the next carriage return occurs, it will clock Z50 at pin 11 on its ascending edge. This will cause Z50 pin 9 to go high enabling Z29. If the next character is a line feed, the circuit will be reset through Z45; however, if no line feed does occur, the next space character will satisfy Z29. The output of Z29 at pin 8 inhibits the flag to the memory; therefore, no new character is entered. This output is also ORed with the right arrow decode by Z3. The result is that the space character, which is destructive, is converted to the right arrow character which also advances the cursor, but does not destroy the memory contents.

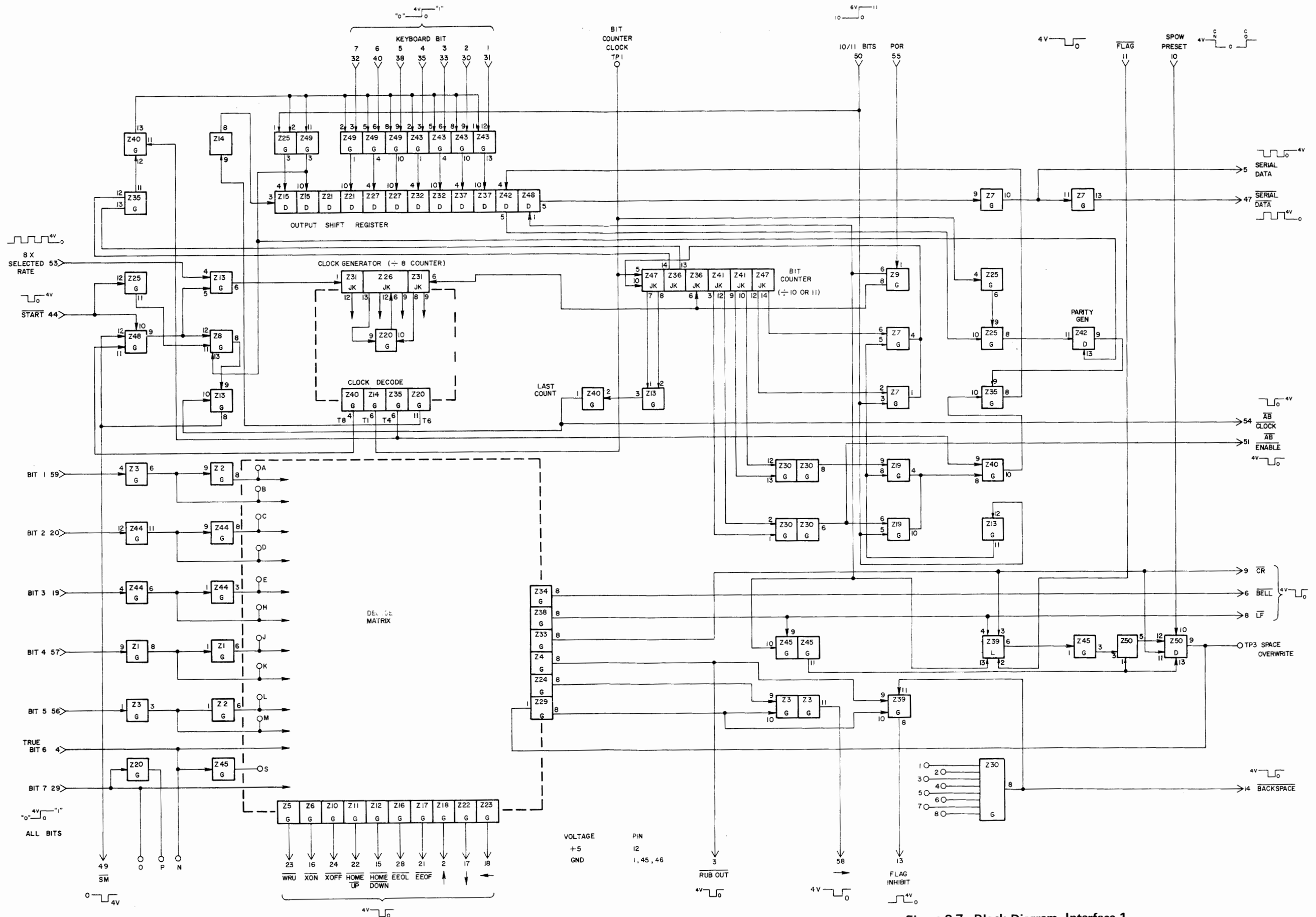
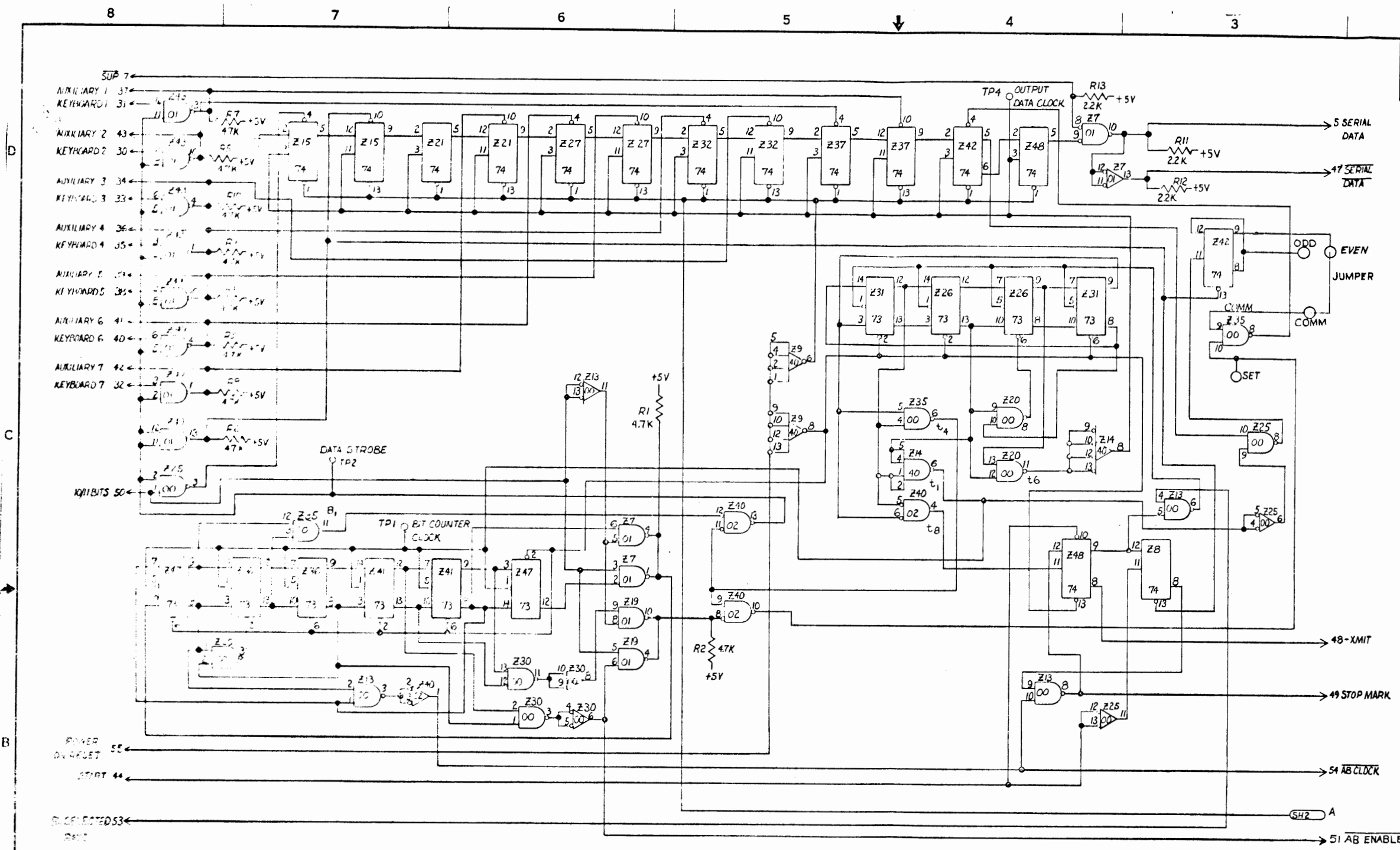
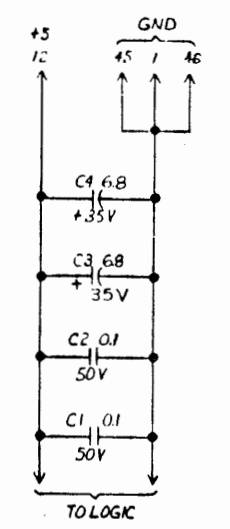


Figure 2-7. Block Diagram, Interface 1



REVISIONS					
TAB REV	INC EG	DESCRIPTION	ENGR APVD	DATE	APVD
		REV PER MARKED SEP14		2-11-69	J.S.
				3-14-69	W.R.P.
DCN 204		19-NOV-1969 W.J.C.	J.M.	11-26-69	B. D.M.
DCN 242		12-JAN-70 M.E.V.	G.A.	1-22-70	C. D.M.
DCN 259		2-23-70 M.E.V.	G.A.	2-27-70	D. D.M.
SOSG		10-9-73 J.L.L.	J.M.	10-11-73	E. B.M.
		REDRAWN FROM J'S SIZE WITHOUT CHANGE 4-24-74 W.A.G.	J.M.	5-21-74	F. W.L.M.



Z8	74	1,2,3,4	5,6
Z19	01	11,12	13
Z19	01	2,3	1
Z35	00	1,2	3
REF DES	TYPE	INPUT	OUTPUT
		SPARES	

1. NAME OF INTERNAL LOGIC KEYBOARD IS NOT TO BE USED.  
 2. NUMBER OF PINS FOR EACH IC MUST BE SPECIFIED.  
 3. ALL GATES MUST BE SPECIFIED BY TYPE AND MANUFACTURER'S PART NUMBER.  
 4. ALL IC'S MUST BE SPECIFIED BY TYPE AND MANUFACTURER'S PART NUMBER.  
 5. ALL LOGIC SYMBOLS ARE TO BE DRAWN TO THE STANDARD LOGIC SYMBOLS LIST.  
 6. ALL LOGIC SYMBOLS ARE TO BE DRAWN TO THE STANDARD LOGIC SYMBOLS LIST.  
 7. ALL LOGIC SYMBOLS ARE TO BE DRAWN TO THE STANDARD LOGIC SYMBOLS LIST.  
 8. ALL LOGIC SYMBOLS ARE TO BE DRAWN TO THE STANDARD LOGIC SYMBOLS LIST.  
 9. ALL LOGIC SYMBOLS ARE TO BE DRAWN TO THE STANDARD LOGIC SYMBOLS LIST.  
 10. ALL LOGIC SYMBOLS ARE TO BE DRAWN TO THE STANDARD LOGIC SYMBOLS LIST.

**NOTES: (UNLESS OTHERWISE SPEC)**

Figure 2-8. Interface Logic 1 (1 of 2)

SN7474	14	7
SN7401	10	11
SN7473	4	11
IC TYPE	+5	GND

Z50	---
TP4	---
R13	---
C4	---
LAST USED	NOT USED
REF DES	---

DO NOT SCALE PRINT		DRAWN	DATE
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND IN-LINE APPLICABLE		WOODY GORDON	1-24-74
TOLERANCE		UNIFORM	4/4/70
.XX ± .02 .XXX ± .010 L ± .30"		ENGINEERING APPROVAL	5-10-74
HOLE DIA. TOLERANCE		ENGINEERING APPROVAL	
0 thru .250 .251 thru .500 .501 & up		ENGINEERING APPROVAL	
+.003 +.006 +.010		RELEASE	
-.002 -.003 -.008			
TITLE: EXT 2A, INT 2B			5-21-74

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REVISION INDEX	SHEET	REV
	12	F

**Datapoint**  
 SCHEMATIC DIAGRAM,  
 INTERFACE LOGIC NO.1

SIZE: D DWG NO: 01-1-01-0005 REV: F

SCALE: NONE

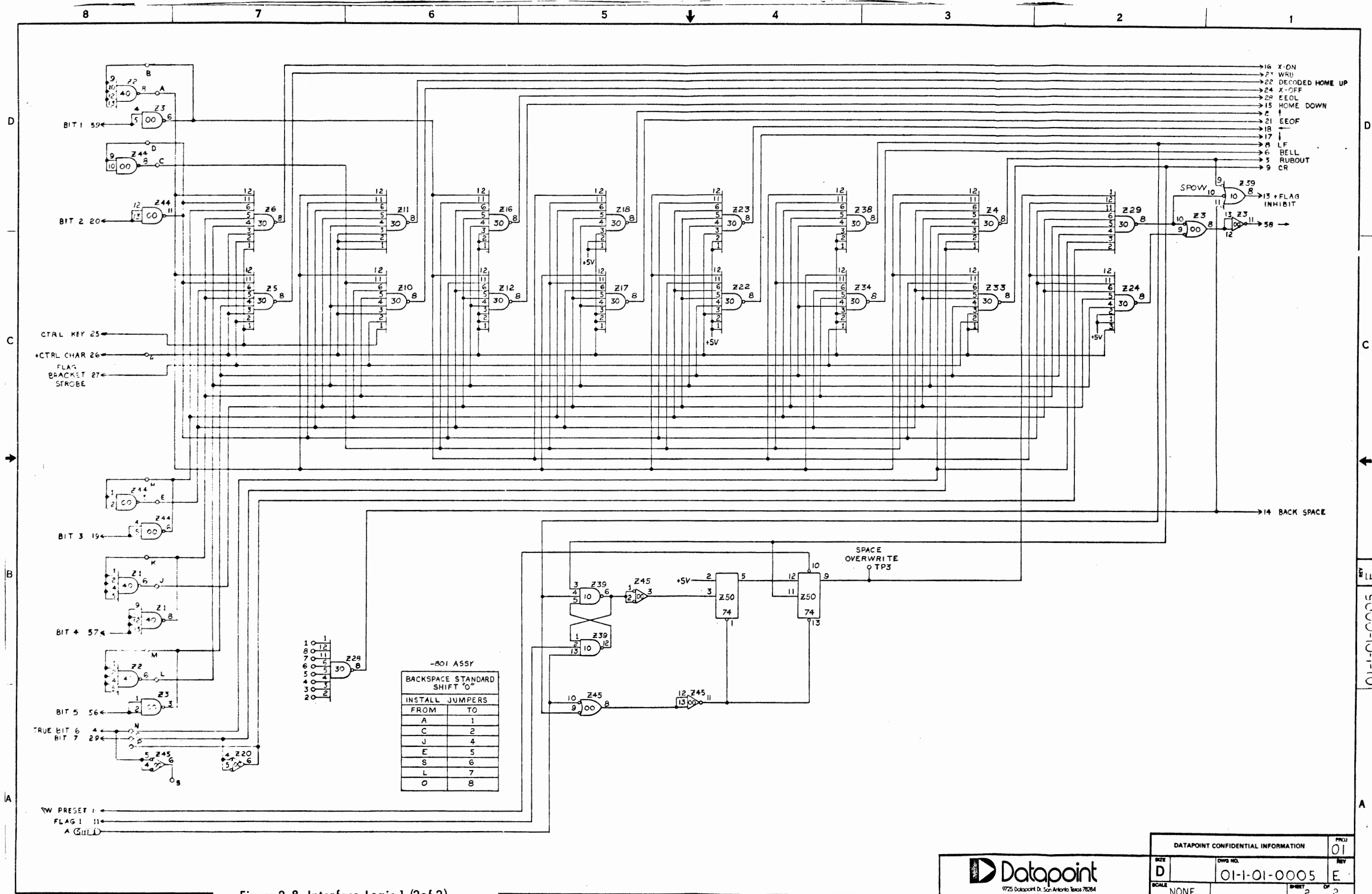


Figure 2-8. Interface Logic 1 (2 of 2)



DATAPPOINT CONFIDENTIAL INFORMATION		PROJ	01
SIZE	D	DWG NO.	01-1-01-0005
SCALE	NONE	REV	E
		SHEET	2 OF 2

## INTERFACE 2

The Interface 2 card consists primarily of the data receiver for the Datapoint 3300. Serial data being received is presented to the display memory and the function matrix as parallel characters. Other functions located on the Interface 2 card are the two bit-rate oscillators/dividers, the request to send latch with high speed data turn-around circuit, Space Overwrite preset, bell driver and a control-character reset circuit. Also, included on some Interface 2 cards is the optional speed buffer and its associated control circuits.

Figure 2-9 is a functional block diagram of the Interface 2 card without Speed Buffer. A block diagram of the Speed Buffer is shown in figure 2-10. Figure 2-11 shows the Interface 2 card with Speed Buffer and all associated circuitry. Figure 2-12 shows the Interface 2 card without the Speed Buffer.

Input data is routed through Z29 to the input shift register, Z61-Z65. The start space sets the start latch, Z28, which removes the reset from the input register and gates the 8x Bit Rate Clock to the input bit chopper, Z68 and Z69. The input bit chopper, a radix-eight Johnson counter, reduces the input clock to bit rate. The fourth count is decoded by Z46 and is used to clock the input register on its rising edge. The rising edge occurs half-way through each bit time, thus sampling the incoming data in the middle of each bit.

The presence of the start space at Z65 pin 5 (after 10 shift clocks) enables succeeding timing pulses to be gated through Z57 pins 4, 10 and 13. The output of Z57 pin 4 occurs at "time 5" of the radix-eight bit chopper and is gated through Z56 pin 8 and Z15 pin 8 to clock the data now present in the input register into the input hold register, Z11 pin 14. The output of Z57 pin 10 (time 6) will be gated through Z18 pin 8 as  $\overline{FLAG}$  unless the character that has been transferred is a control character. The output of Z1 pin 8 detects control characters and inhibits the  $\overline{FLAG}$  through Z26 pin 6 and Z36 pin 8. The outputs of Z57 pin 13 and Z57 pin 1 (time 7) provide resets to both the control character reset latch, Z28 pin 11, and the start latch, Z28 pin 3.

Word sync is maintained by gating the reset timing pulse, Z57 pin 1, with the start space,

Z56 pin 6, and the first stop mark, Z61 pin 9. These three inputs are gated through Z67 pins 9, 10 and 11. The rising edge of Z67 pin 8 will clock the start latch, Z28 to the reset condition.

If the character present in the input hold register is decoded as any of the functions brought back to Z5 pins 3, 4, 5, 6, 11 or 12, the control character reset latch, Z28 pins 8 and 9, immediately resets the input hold register. The resulting decoded outputs, excepting HOME DOWN, are only present for approximately 125 nano-seconds. A decoded HOME DOWN sets latch Z17, Z27 and allows divider Z38 to count out a "time window" ( $\geq 600$  micro-seconds) to allow the control logic timer enough time to execute HOME DOWN. HOME DOWN is not executed in speed ranges over 440 bits/seconds due to the time required.

The two bit-rate oscillators are two-transistor, crystal controlled circuits with a discrete buffer on each. The 225.28 KHz oscillator provides the basic frequency for all 11-bit code data rates, e.g. 110, 220, 440, 880 and 1760, while the 307.20 KHz oscillator provides all 10-bit code data rates, e.g. 150, 300, 600, 1200 and 2400. The output of each oscillator is gated into Z66. A single 10/11 control line is brought into Z66 to allow one of the oscillators to be gated into Z16 and Z7, the dividers. Outputs from the dividers (actual frequency is eight times the data rate) are routed to the rotary switch for baud rate selection.

The Space Overwrite consists of Z3, Z4 and one Z14 flip-flop. The output of Z3 presets Z14 pin 5 to "zero" upon decoding a "control N". A "zero" on Z14 pin 5 is sent to the Interface 1 card to lock its circuit into Space Overwrite. The output of Z4, upon receipt of a "control 0", presets Z14 pin 5 to a "one" thereby releasing the Space Overwrite circuit.

The bell-driver consists of Z20, two Z19 gates and a discrete output driver. When either a decoded BELL or count 64 is received, Z19 and Z20 supply an output to the discrete driver, the width of a 7.5 Hz clock pulse, thereby gating the tone generator for a period great enough to be audible.



The request-to-send latch is Z9. In the REMOTE mode, depressing any key provides a START pulse which sets the latch and raises the request-to-send line. When operating with any data set other than a 202, the request-to-send latch will remain engaged until the LOCAL/REMOTE switch is moved to the LOCAL position. When operating high-speed with 202 data sets, the remote computer may control the status of the request-to-send latch through the "carrier detected" and "reverse channel received" inputs.

If the remote terminal or remote computer lowers its reverse channel, the change is gated through the Schmitt Trigger, Z1 pin 3, Z19 pin 3 and appears as a clipped, differentiated pulse at Z1 pin 6. This pulse is gated through Z2 pin 4 to reset the request-to-send latch, thereby lowering the request-to-send line to the data set. If the remote terminal or remote computer has completed its transmission, it may raise the request-to-send line by lowering its carrier or main channel. The change is gated through Z6 pin 11 thereby clocking the request-to-send latch back to the "send" mode.

### **Speed Buffer**

The purpose of the Speed Buffer is to temporarily store incoming high-speed (>600 bits/second) characters, until synchronization with the display is achieved. Characters may then be written in rapid succession at the display memory stepping rate of 130 KHz.

The Speed Buffer consists of a clock divider, load control circuits, the high-speed circulating registers (memory), a temporary holding register and the unload control circuits.

This explanation will refer to the block diagram figure 2-10 and details of the Interface 2 card with the Speed Buffer are shown in the schematic figure 2-11.

The clock divider is a radix-six Johnson counter, Z70 and Z60, that divides the 13.3 MHz master clock to 2.22 MHz. The high speed circulating registers, Z31 - Z35, Z41, Z43 and Z45 are clocked from Z50 pin 11 which decodes count 1. Shift occurs on the rising edge of count 1.

Referring to the input shift register and input bit chopper clock, the presence of the start space at Z65 pin 5 arms Z48 pin 12. One output of the "TAG" high-speed register Z35 pin 14, is tied to Z48 pin 11 so that if data is present in the registers, the new character will be loaded only when the falling edge of the TAG occurs. If a TAG is present, Z48 pin 8 will be clocked "low" thereby starting the load sequence. If no TAG is detected by time 5 of the input bit chopper, the output of Z56 pin 6 initiates the load sequence through Z58 pin 11.

Either of these load commands clocks Z59 pin 5 high which will allow the next speed buffer clock time 4 to clock Z59 pin 9 high and also be gated through Z58 pin 3. (This is a latching circuit to permit only one, time 4 pulse to be gated through.) This time 4 pulse is decoded at Z50 pin 6 and inverted through Z58 pin 8. This gated time 4 pulse clocks Z48 pin 6 low. Z49 pins 4 and 10 invert this output to enable all "load" gates contained in Z52 - Z55 that are tied to this line. The "recirculate" gates, also contained in Z52 - Z55, are tied to Z49 pin 1 and 13 are now inhibited. Data present in the input shift register will now be entered into the speed buffer on the rising edge of the next speed buffer clock (rising edge of time 1). A TAG bit will also be entered into Z35.

The next speed buffer time 2 pulse that occurs, gated through Z50 pin 3, will apply a reset at Z48 pin 1 and Z59 pin 13 thereby returning the buffer to the "recirculate" mode and restoring the load circuits to their original states. The input register data has now been entered into the Speed Buffer which allows the input register to be reset.

Since the Speed Buffer data must be maintained in first-in, first-out order, the unload sequence must begin on the rising edge of the TAG, which represents the first character entered Z24 pin 5 to clocked high on the rising edge of TAG applied to Z24 pin 3. Z24 pin 5 enables Z40 pin 6 to allow the next time 4 Speed Buffer clock to clock the data into the temporary holding register Z21 - Z24, through Z25 pin 6. At the same time, Z30 pin 5 was preset to the "one" state,



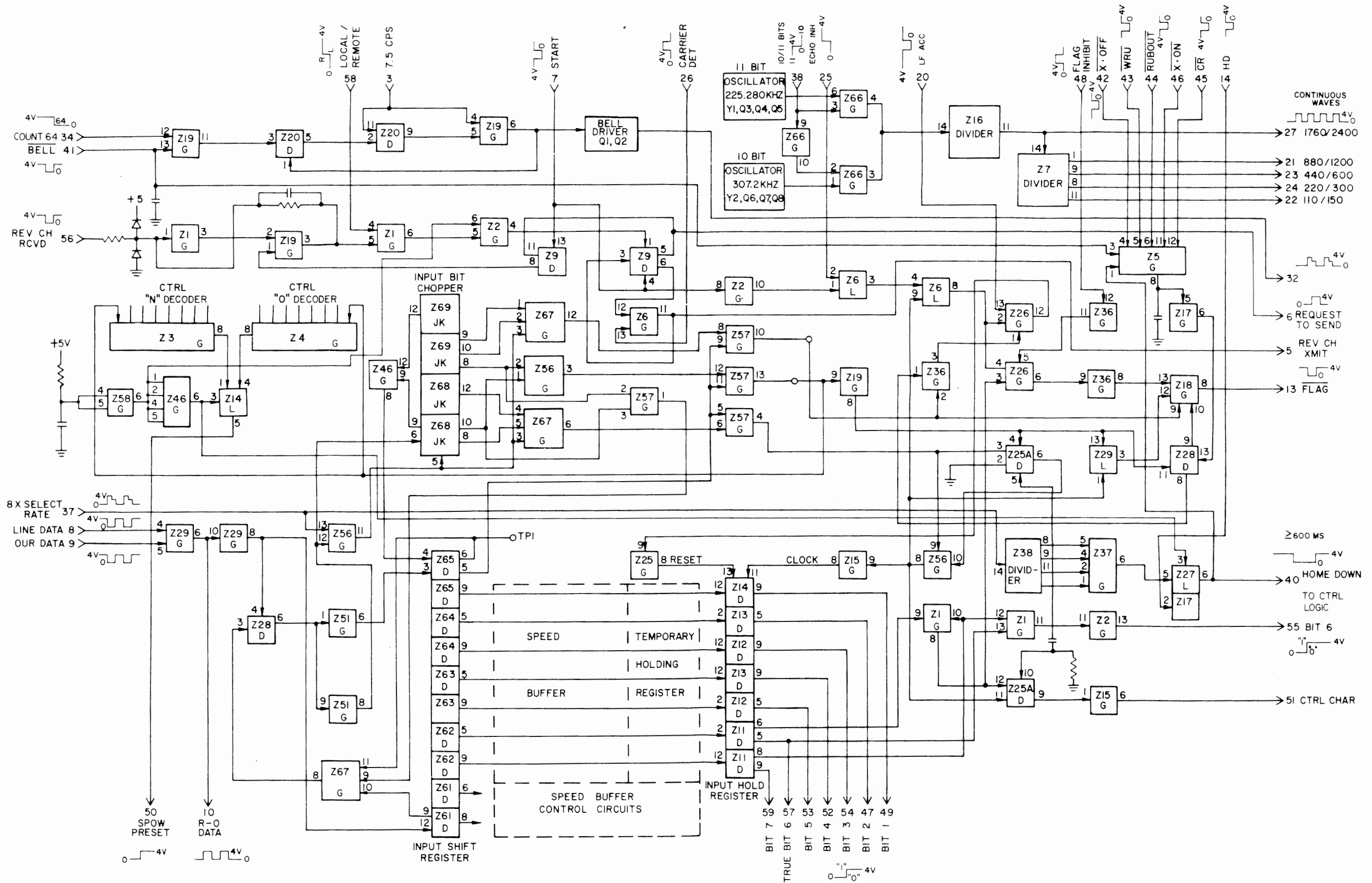


Figure 2-9. Block Diagram, Interface 2

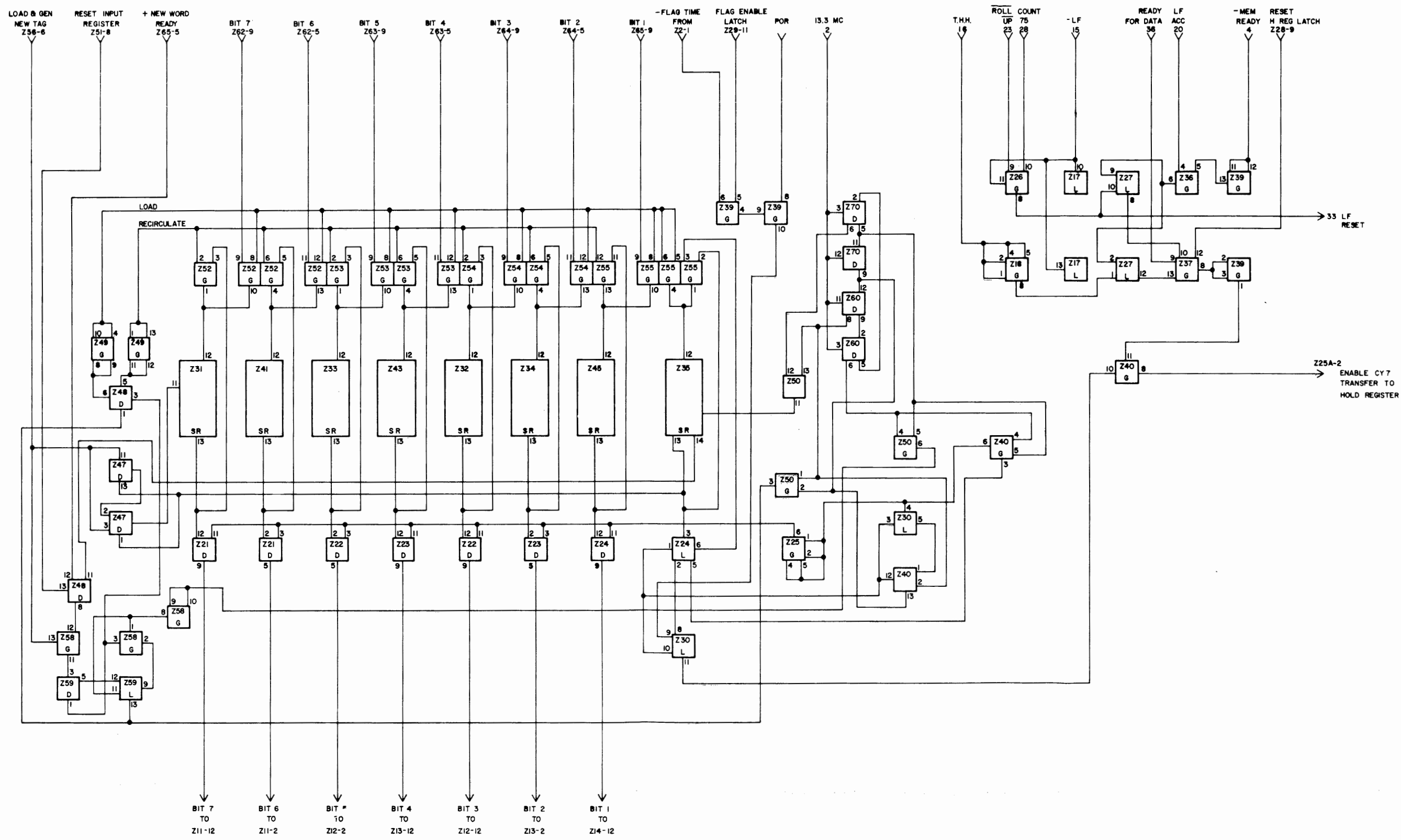


Figure 2-10. Block Diagram, Speed Buffer

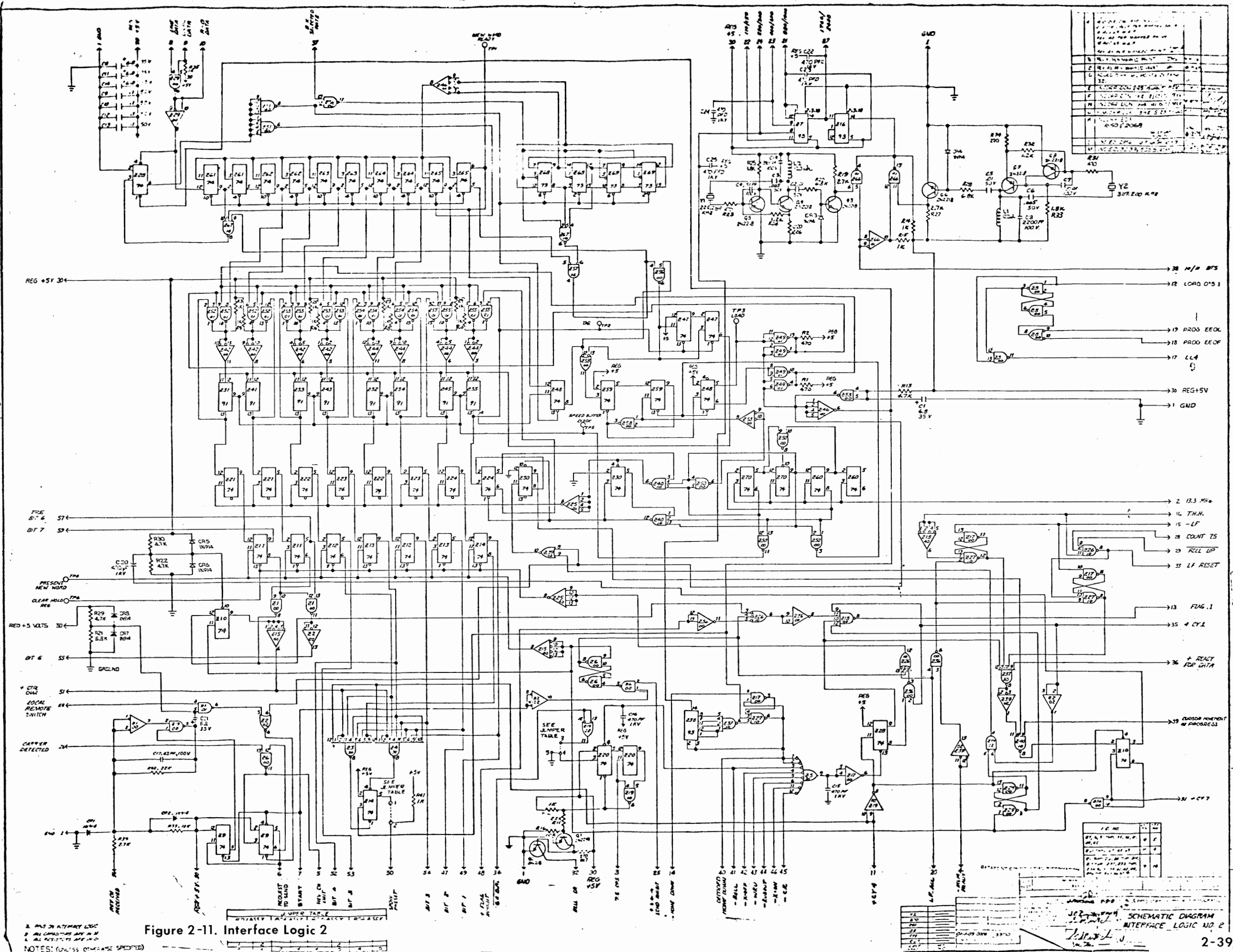


Figure 2-11. Interface Logic 2

NOTES: (UNLESS OTHERWISE SPECIFIED)

**INTENTIONALLY LEFT BLANK**

**"DRAWING DELETED"**

**Figure 2-12.**

**2-41/(2-42 blank)**

thus allowing Z40 pin 12 to reset and clock respectively, Z24 pin 5 and Z30 pin 5 to their original states. During this period, Z24 pin 6 has been routed back to Z55 pin 3 which enters a "zero" in the TAG, representing this character, that has been removed from the Speed Buffer. Before this character can be transferred to the "input hold register", six conditions must be met. They are:

1. A ROLL UP must not be in progress, denoted by Z27 pin 12 being high. (Latch formed by Z17 pin 11, Z27 pin 12, reset by Z18 pin 6.)
2. A LINE FEED must not be in progress, denoted by Z27 pin 8 being high. (Latch formed by Z17 pin 8, Z27 pin 8, reset by Z26 pin 8.)
3. No holding register reset must be present, denoted by Z27 pin 8 being high.
4. Data must be present in the temporary holding register, Z30 pin 9 high.
5. The ready-for-data line, pin 36, must be high.
6. The memory ready line, pin 4, must be low and the LF accepted line, pin 20, must have returned high.

When all of these conditions have been met, Z40 pin 8 will go low thus enabling the next cycle 7 clock to change Z25 pin 6 high and gate through one cycle 7 pulse. The cycle 7 pulse is gated through Z15 pin 8, which clocks the data in the temporary holding register into the input hold register.

If the character transferred is a printable character, cycle 1 will be gated through Z18 pin 8 and sent to the display memory as a FLAG. If it is a control character, Z1 pin 8 will inhibit the flag and the matrix on Interface 1 will decode the character. After execution of the control character, it will either be reset by the control character latch or be reset from the Control Logic via the LF accepted line, pin 20.

At the time the transfer occurred, (Cycle 7 through Z56 pin 8), latch Z29 pin 3 and Z29

pin 11 enabled Z18 pin 12 to pass the next cycle 1 (FLAG). After this latch set, cycle 1 was also gated through Z39 pin 4 and Z39 pin 10 to clock Z30 pin 8 back to the "ONE" state, thus denoting the character had been taken from the temporary holding register. This initiates an immediate search for the next character in the Speed Buffer.

The completion of the unload cycle occurs on the following cycle 4. The cycle 4 input at pin 11, gated through Z19 pin 8, resets the Z29 pin 11, Z29 pin 3 latch and resets Z25 pin 6 to its original state.

Now that synchronization with the display memory has been achieved, the Ready-for-Data line will return high on the following cycle 6. Since the temporary holding register will have another character by this time, the unload cycle will repeat on the following cycle 7 until the Speed Buffer is empty.

## MOS

The MOS card contains the Circulating Memory, the Read Only Memory (ROM) and the Master Oscillator Circuitry. This explanation makes reference to the Block Diagram in figure 2-13. Figure 2-14 is the MOS Schematic Diagram providing additional details of the circuits.

The Master Oscillator is a dual transistor 26.6 MHz crystal controlled circuit. JK flip-flop, Z19, serves as a buffer and a divide-by-two counter for the oscillator output. The output of Z19 is present at connector pin 13 and is connected to NAND gate Z22 pin 1. The NAND gate Z22 is not satisfied until pin 11 of the latch Z22 is high. This occurs each time the 60 Hz line tap at connector pin 28 goes positive. Latch Z22 is reset by the End of Frame (EOF) signal from the control logic. The output of Z22 pin 3 is a 13.3 MHz burst starting with each cycle of the line voltage and ending with the display frame. This technique prevents any flicker in the display due to a difference beat between the line frequency and the frame rate.

The synchronized 13.3 MHz drives the dot generator which is a divide-by-seven synchronous counter. Gates Z35 and Z36 decode the seven dot times from the counter.

The dot times are the seven vertical dots of the 5 x 7 dot matrix. Dot number one appears at Z35 pin 11 and the dots are decoded sequentially with dot seven appearing at Z36 pin 3. Adjacent dot times occur 75 nanoseconds apart and the dot width is approximately 37.5 nanoseconds.

Dot seven enables the JK flip-flop Z18 which is being clocked by the 13.3 MHz clock. The output at Z18 pin 6 is the 950 KHz signal used for the minor vertical deflection frequency. The inverted 950 KHz is present at Z8 pin 6. This signal is used to drive the cycle generator which is another divide-by-seven synchronous counter.

The cycle generator is the heart of the master timing system. Decoded signals from the cycle generator control the ROM read cycles and the phase clock generation for the Circulating Memory and clock pulses for the memory character counter on the control logic card. Gates Z34 and Z33 decode five counts which cause the ROM to access five sequential words. The two counts connected to Z13 pins 8 and 12 are the input gates to the phase clock generator or clock drivers. The transistors Q1 through Q6 convert the logic level cycle clocks into MOS compatible signals.

The Circulating Memory consists of fifty-four 200 bit shift registers. The memory is configured in six tracks of nine packs each, providing the 1800 character length and the six bit width. All tracks operate identically therefore, only bit 1 or track 1 will be discussed.

Data is normally recirculating in the memory at a 135 KHz rate. The collectors of Q3 and Q6 provide the two phase 135 KHz clock pulses. As data passes through the eighteen hundredth position, it is passed from Z61 pin 6 through gate Z29 to the recirculating gate Z1 pin 6. In the recirculating mode, pin 5 of Z1 will be high, thus allowing the data to re-enter the circulating memory through Z1. If new data is to be entered in place of the circulating data, the bit will be present at connector pin 56 and Z1 pin 11. A flag will occur at connector pin 12 causing the output of the D flip-flop, Z9 pin 5, to go high. When the compare point is reached, the pulse occurring at connector pin 7 will cause latch Z17 pin 6 to go low, thus, causing the latch Z17 pin 11 to go low.

The low from Z17 pin 11 is applied to Z7 pin 8 and Z7 pin 11. The resulting high output at Z7 pin 9 enables the "new data gate" Z1 pin 12 and allows the new bit to be entered. The resulting low at Z6 pin 10 disables the recirculating gate Z1 at pin 5. The gate Z5 output at pin 1 serves to enable and disable the auxiliary inputs in the same manner as Z7 pin 9 output does for the receive bits.

The cursor is advanced after the character is loaded into the memory. The latch, Z17, was set during the load time, making Z17 pin 3 high. This high enables Z21 and Z20. The output at Z21 pin 6 occurs at cycle 5 and advances the cursor one character position. The output at Z21 pin 8 is passed through the inverter Z14 and produces the roll advance strobe at connector pin 23. The output of Z20 pin 6 resets the first Z17 latch at cycle 6. The second Z17 latch is reset by cycle 7 from Z50 pin 12. At this time, the input gates return to the recirculating mode.

The memory is cleared by loading zeros into the bit positions. The gates, Z12 pins 4 and 5 and Z16 pins 1, 2 and 13, receive the various functions that require zeros to be loaded. The functions are: ERASE END OF LINE (EOL), ERASE END OF FRAME (EOF) and POWER ON RESET (POR). The outputs of Z10 pins 1 and 4 occur at compare time and are connected to the OR gate Z12 pin 1. The other input to Z12 at pin 2 comes from the control logic card and occurs when the frame is being rolled down. The output of Z12 pin 3 is a high which causes Z6 pin 13 to go low, thus inhibiting the recirculating gates and zeros are placed in the memory.

A character is present at the Circulating Memory output for approximately 7.5 micro-seconds, due to the clock rate, before it is shifted around and replaced by the next character. Gates Z30 and Z33 present the six data bits to the ROM during this time and define one of 64 unique blocks of five addresses. The cycle counter pulses the ROM approximately once every micro-second until five words have been read out. The output of the ROM is a seven bit word. The first word corresponds to the first column of seven dots, the second word corresponds to the second column of seven dots, etc.

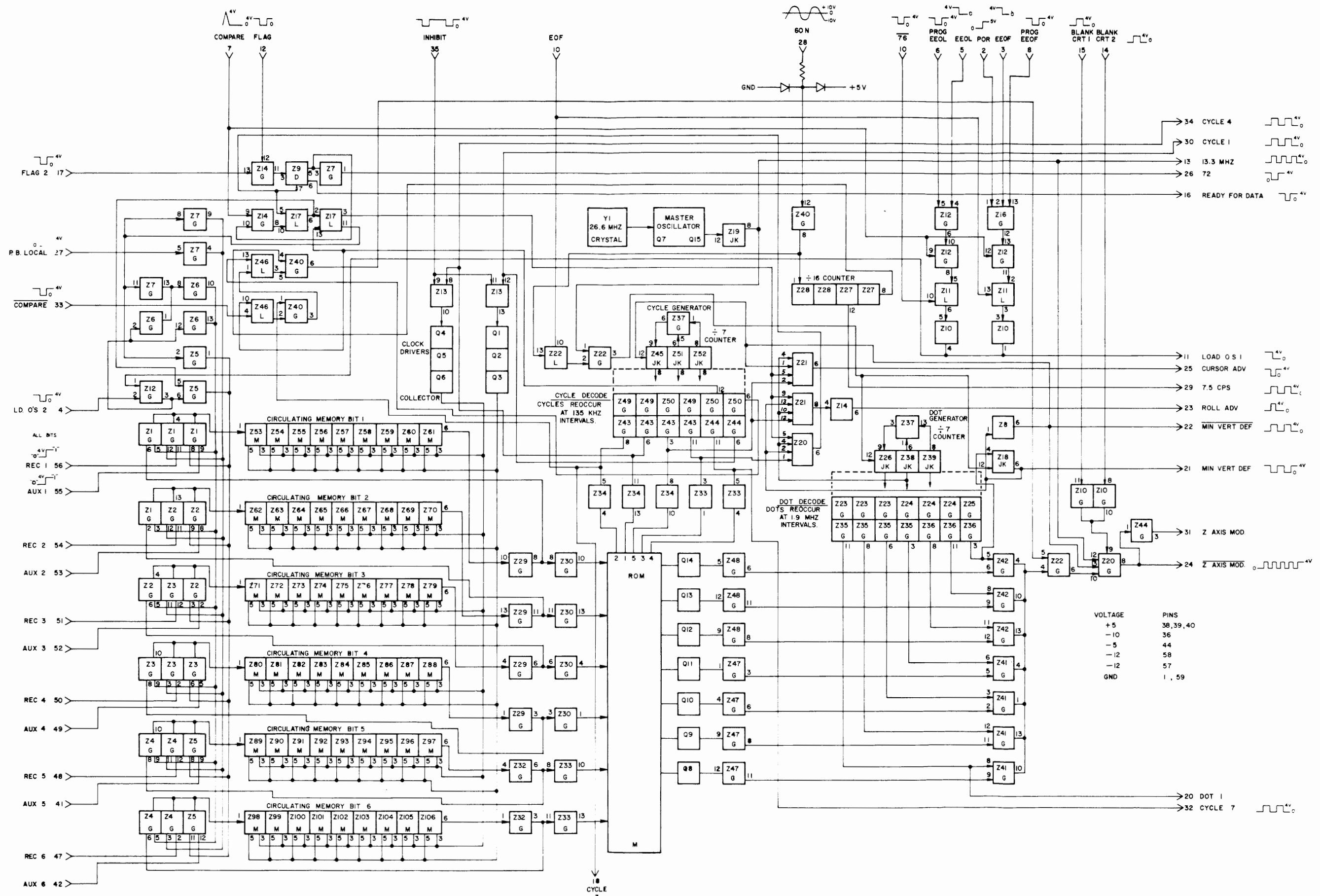


Figure 2-13. Block Diagram, MOS







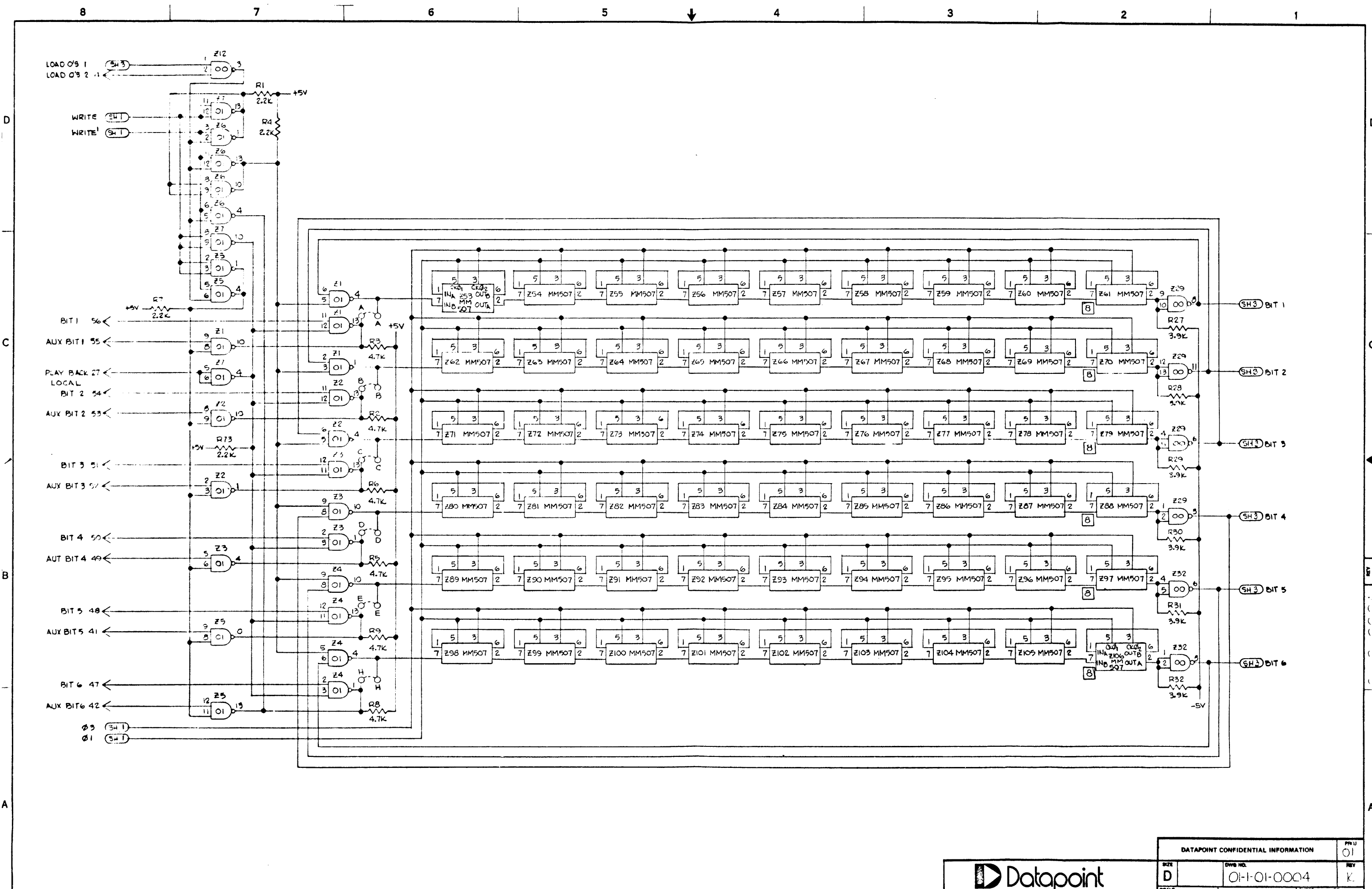


Figure 2-14. MOS Control Logic (2 of 3)

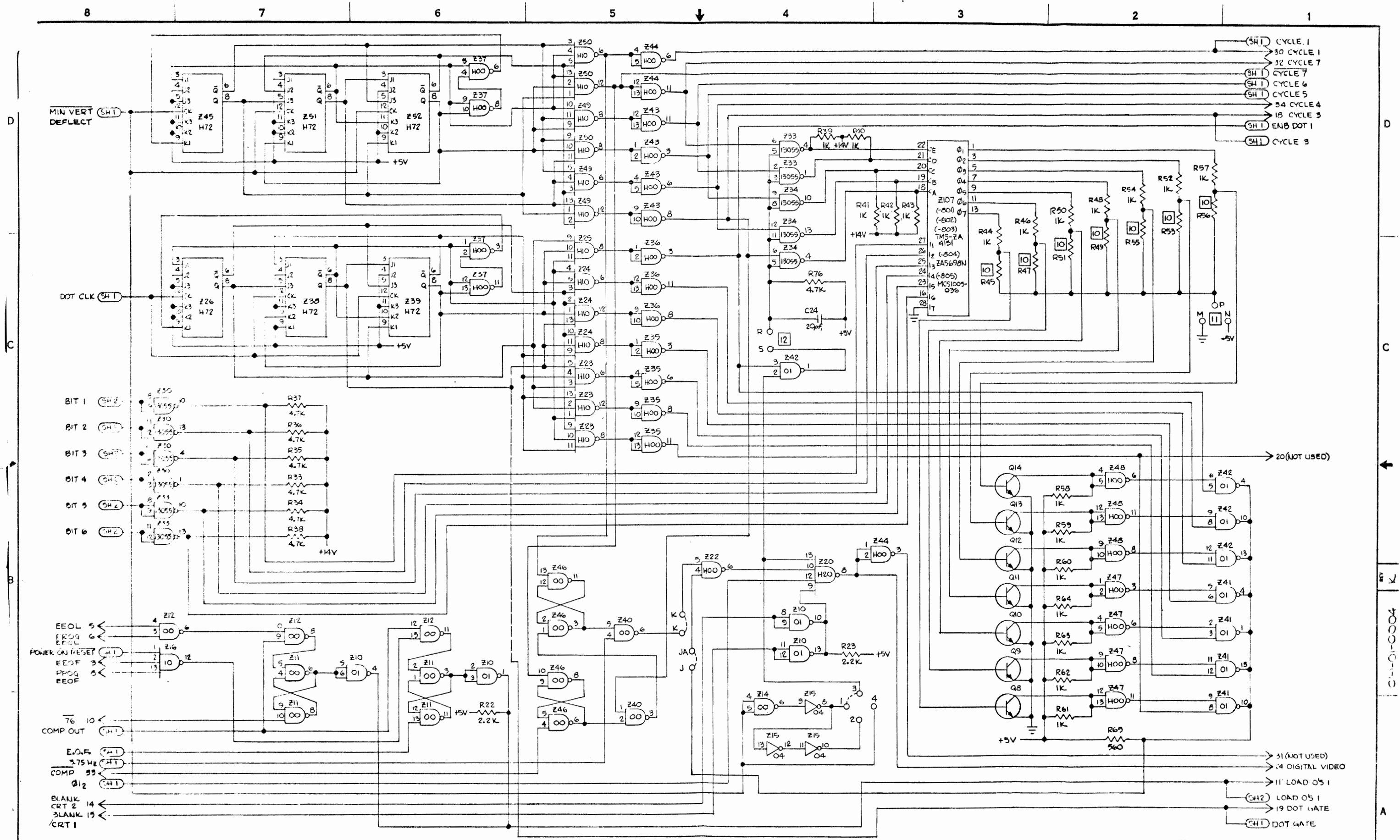


Figure 2-14. MOS Control Logic (3 of 3)



Datapoint CONFIDENTIAL INFORMATION		REV
SIZE	DWG NO.	REV
D	01-1-01-0004	K
2-51/(2-52 blank)		

The transistors Q8 through Q14 convert MOS LEVELS to logic levels and passes them through gates Z47 and Z48. The outputs of Z47 and Z48 enable the dot gates Z41 and Z42 when a "one" is present. While each seven bit word is present, the dot generator scans each gate in sequence. The outputs of Z41 and Z42 are collector ORed (wire ORed) together so that if any one gate is satisfied, a pulse appears at Z22 pin 4. The dot pulses are ORed with cursor pulses by Z22. The cursor occurs at compare time and consists of all 35 dots. A 3.75 Hz signal from Z27 pin 8 is gated with the cursor enable at Z40 pin 4. The output of Z40 pin 6 is a 35 dot burst occurring approximately every 20 frames, thus giving the cursor a blink rate of about three times per second. The output of Z22 pin 6 is gated with the 13.3 MHz clock, Cycle 1 and the CRT blanking inhibits at gate Z20. The output of Z20 at pin 8 is the minor vertical deflection modulation. The inverter Z44 provides the compliment of the minor vertical deflection modulation at Z44 pin 3. The dot times occur at 75 nano-second intervals with each dot being 37.5 nano-seconds wide. The 5 x 7 dot matrix generation for the character "A" is shown in figure 2-15.

A malfunctioning MOS is indicated by a character changing when a displayed line of characters is rolled up or down the screen.

To identify a faulty MOS in LOCAL mode, momentarily depress HOME UP key and then ERASE EOF key. Type alternately the @ symbol and the question mark (?) until the first display line is filled, e.g. @ ? @ ? @ ? @ ? , etc. This loads characters into the MOS which will exercise maximum change within the MOS, since the @ symbol is a binary code of 1000 000 and the question mark (?) is a binary code of 0111 111. (Only the first six bits are significant to character display and are stored in MOS.)

If this displayed line is now moved down the screen, using the ROLL DOWN key, any character change in the displayed line is indicative of a faulty MOS at that point in the memory. Identify on which line the character changed and which character it is in the displayed line.

By using the code assignments shown in Table 1-2, identify which of the six bits in the symbol is changing, e.g. the 39th character changed from

the @ symbol to a B when moved to the 12th line. The binary code change was from a zero to a one in Bit 2.

Using this example, refer to figure 2-17, and locate the changing character position in the 39th vertical column of spaces and the 12th line down. This space location shows the changing character is stored in the MOS cans located in the 5th column on the MOS card. Refer to the MOS locator in figure 2-16 and the faulty MOS is in the Bit 2 row under the 5th column.

To completely check every MOS, repeat the procedure but this time start typing the display line with the question mark (?) and then the @ symbol, e.g. ? @ ? @ ? @ ? @ etc.

To preclude rolling the displayed line off the screen, use the cursor HOME UP prior to ROLL UP or the cursor HOME DOWN prior to ROLL DOWN and the cursor will indicate the 1st display line or the 25th display line, respectively.

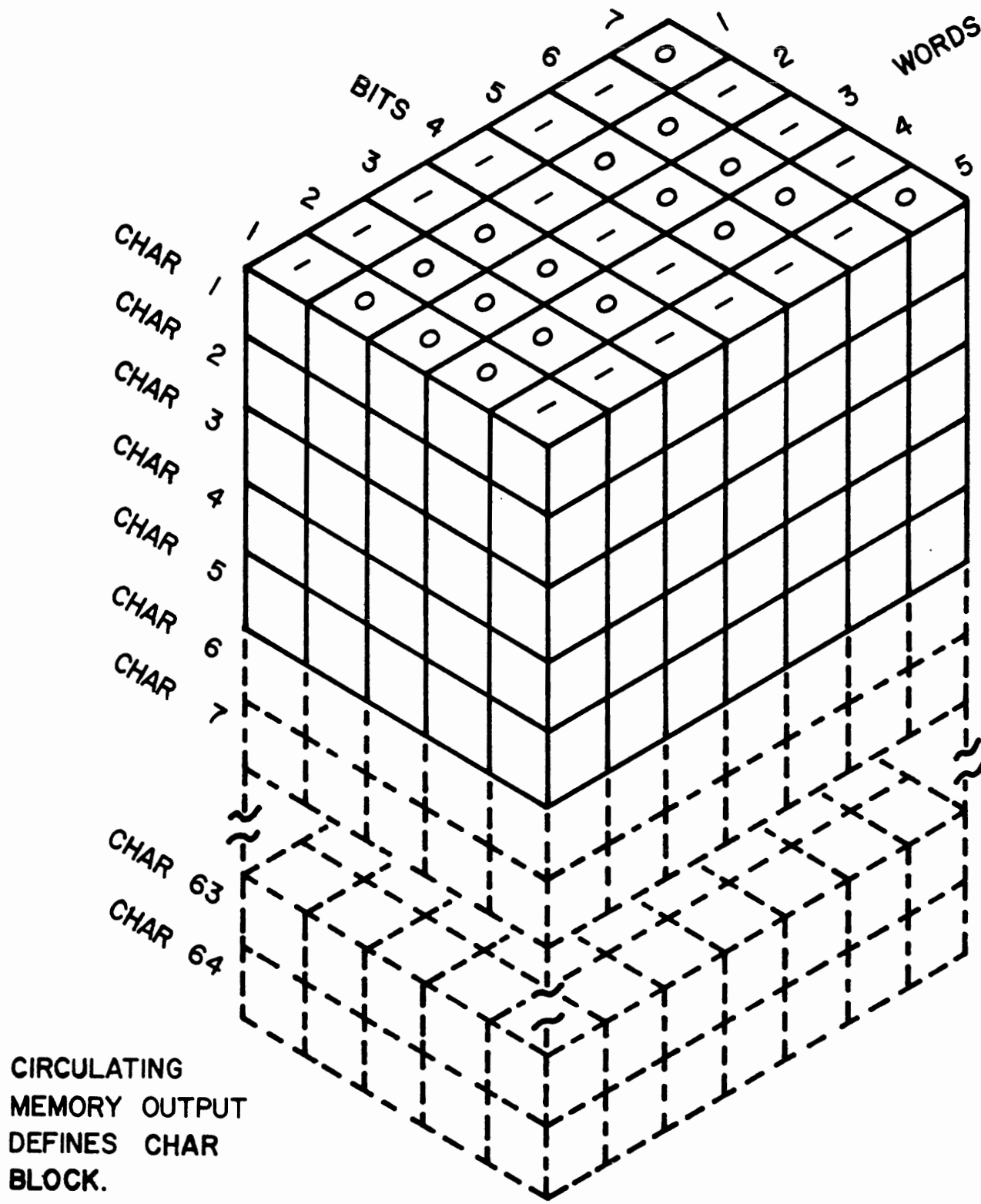
## DEFLECTION AMPLIFIER

The Deflection Amplifier card contains the write, vertical and horizontal deflection amplifiers, the video amplifier and the RS-232-B converters.

Figure 2-20 is a functional block diagram and figure 2-21 is a schematic diagram. This explanation makes reference to figure 2-21.

The 950 KHz minor vertical deflection square wave from the MOS card enters the deflection board at connector pin 13. Transistor Q6 provides isolation of the logic on the MOS card from the higher DC voltages present in the write amplifier. The output of Q6 is clamped by diode CR7 and passed through the filter consisting of C5, C6 and L2. The filter circuit removes the DC component of the wave and makes the waveform symmetrical around ground. Transistors Q7 and Q8 form a differential input to the operational amplifier formed by Q7 through Q13. Transistors Q9 and Q10 form a current source for the output base drivers. As the voltage at the base of Q7 increases in the positive direction, Q7 begins to conduct, shunting some of the current that

**ROM  
FORMAT**



CIRCULATING  
MEMORY OUTPUT  
DEFINES CHAR  
BLOCK.

	WORDS				
	1	2	3	4	5
7	0	1	1	1	0
6	1	0	0	0	1
5	1	0	0	0	1
4	1	1	1	1	1
3	1	0	0	0	1
2	1	0	0	0	1
1	1	0	0	0	1

BITS

CYCLE COUNTER STROBES  
OUT FIVE WORDS FROM  
SELECTED BLOCK.

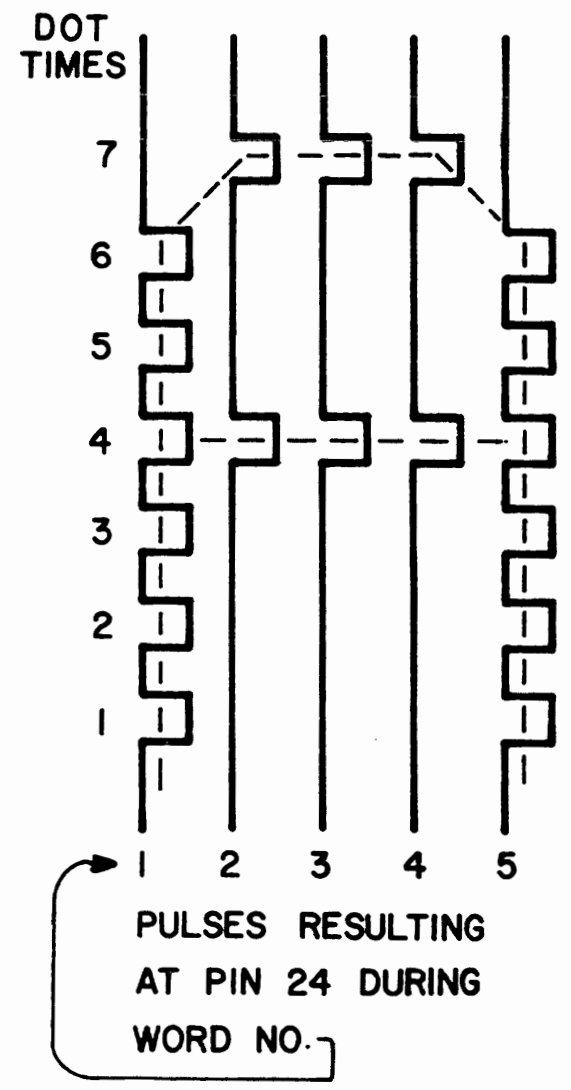


Figure 2-15. Dot Matrix Generation

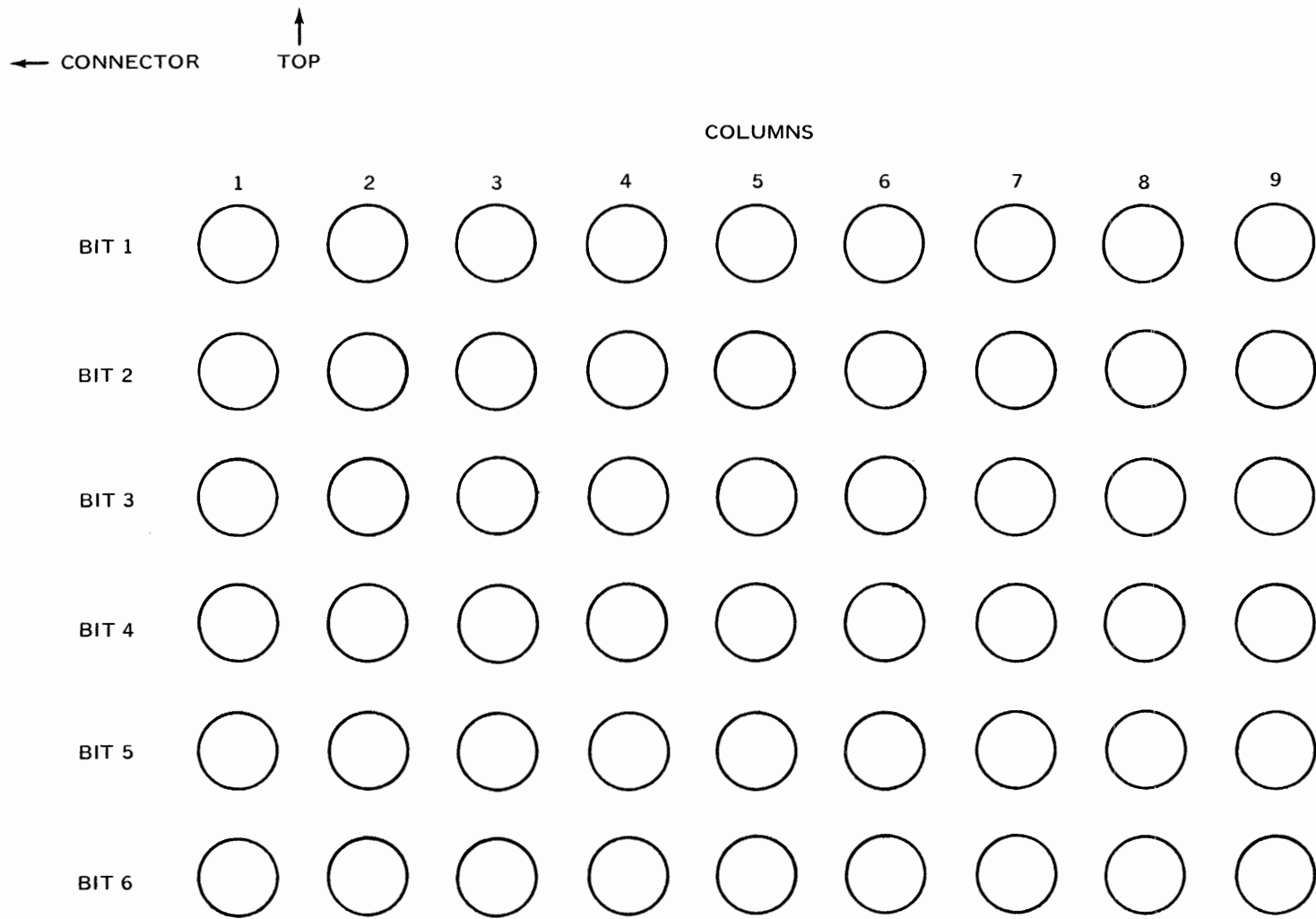


Figure 2-16. MOS Locator

CHARACTER SPACES

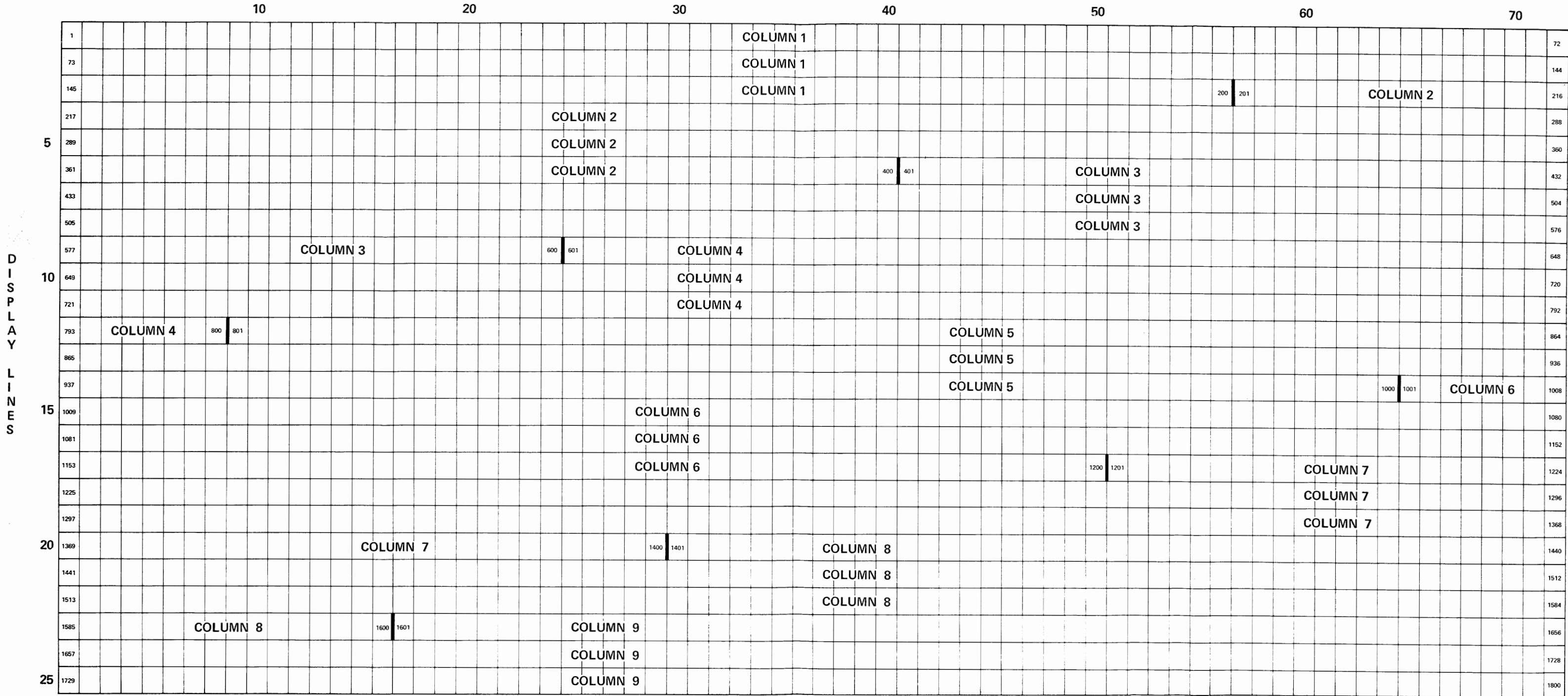


Figure 2-17. Character Display

had been going through Q9. As Q7 conducts, Q8 conducts less, due to the increasing positive voltage at its emitter. This causes more current to flow through Q10, which is inverted by Q12. This action decreases the drive to the bases of Q11 and Q13 and the output drive of their emitters is decreased. The output transistors Q11 and Q13 drive the bases of the power drivers that are mounted on the air duct on the back panel. (See figure 3-14 ).

Figure 2-18 shows the general connection from all three of the deflection amplifiers to the power drivers on the rear panel. The diodes CR8, CR9 and CR10 are connected between the base of Q11 and Q13 to approximately match the four base-emitter junctions of the base drivers, Q11 and Q13 and the power drivers on the rear panel. This diode arrangement prevents any distortion of the output due to zero crossover.

All three sweep amplifiers are identical except for the feed-back source. The write amplifier uses voltage feed-back while the vertical and horizontal amplifiers use a current feed-back taken from the sense resistor on the particular yoke.

The geometry of the CRT is such that the characters are distorted at the sides of the tube, both in height and width. The characters tend to be short and wide at each side and uniform in size at the center of the tube. To correct for this geometric distortion, the horizontal current is monitored from the sense resistor and brought into Q2 and Q3. These transistors provide a steady current through CR13, which develops a voltage across R9 in proportion to the horizontal sweep position. The voltage at R9 is connected through R39 to control the charging rate of the horizontal sweep capacitor, C18.

The output of Q2 and Q3 is also inverted by Q4 and passed through the emitter follower, Q5. The output of Q5 sets the clamp voltage on CR7. This results in the output of Q6 being clamped at a higher voltage at the beginning and end of the sweep than it is clamped to at the center of the sweep. This allows the characters that are normally smaller on the sides of the CRT to have more gain than those in the center. The net result is characters of uniform height across the entire sweep.

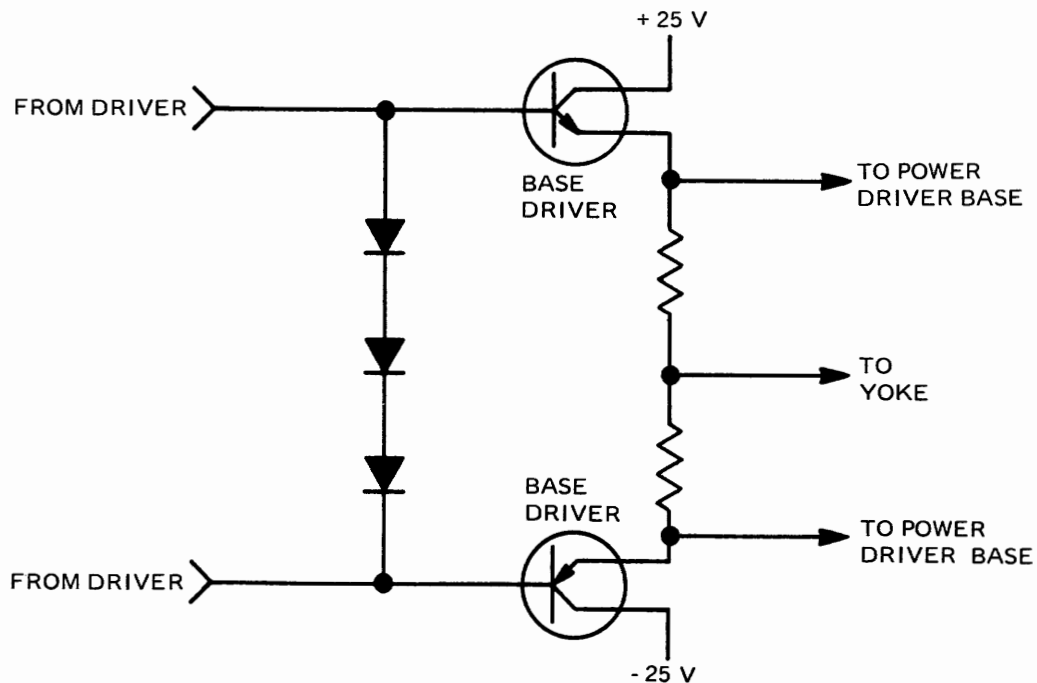


Figure 2-18. Driver Connection

The horizontal ramp frequency from the control logic enters the card at pin 29. Transistor Q14 is an inverter to control the conducting time of Q15. Transistor Q15 is a current generator to charge the sweep capacitor C18. The base of Q15 is held at a constant voltage by VR1 and the charging current at the collector is controlled by the emitter circuit. The correction voltage is connected to the emitter of Q15 and controls the voltage at this point. At the beginning and end of the horizontal sweep, more current is drawn through R39 than is drawn through it at the center of the sweep. The result is a slower rate of charge on capacitor C18 at the ends of the sweep than in the center. The changing charge rate of capacitor C18 throughout the sweep compensates for the geometric distortion and results in characters of uniform size during the entire sweep.

The voltage ramp from C18 is passed through the emitter followers Q16 and Q17 to buffer the capacitor from the amplifier input. Two emitter followers are used (one NPN and one PNP) to compensate for the junction drops in the transistors which would cause an offset in the generated sweep.

Transistors Q18 through Q24 form the horizontal amplifier which is identical to the write amplifier previously described.

The vertical sweep is controlled by the output of the line counter on the control logic card. The inverted inputs from the counter enter the deflection card on pins 5 through 9. Gates Z1 and Z2 form the input to a digital to analog converter. The base of Q26 is the summing junction for the converter. When all of the outputs of Z1 and Z2 are at ground, the only current available at the summing junction is through R72 which has a resistance value chosen to place the first line of the sweep in the desired position.

Resistors R67 through R71 have chosen resistances that will allow current flow in a binary magnitude, e.g., with the same source voltage, each resistor will pass two times the current as the one before. The output of the line counter is a binary count, therefore, the current at the summing junction increases in a binary progression.

The voltage source for resistors R67 through R71 is held at 5V through matched diodes CR18 through CR22. The transistor Q25 is a regulator used to hold the 5V generated across VR2 at a constant level. The values of R60 through R64 are chosen to provide a constant current from each circuit when the corresponding gate input is not active.

The current summing junction is the input to the vertical amplifier which is identical to the write amplifier previously described.

Digital video pulses from the MOS card enter the deflection card at pin 38. The resistor R3 and diodes CR1 and CR2 are a terminating network that suppresses any overshoot or undershoot that is commonly present on high-speed pulsed lines. The pulses are coupled to Q1 through C1. The collector of Q1 contains the peaking coil L1 which ensures a sharp video pulse of approximately 40 V amplitude. The diodes CR3, CR4, CR5 and CR6 protect Q1 from either excessive saturation current or from the inductive kick developed by L1.

In order to protect the video amplifier from internal CRT arcs to the grid, the output of Q1 is AC coupled by C3 to the output, pin 30. Diodes CR12 and CR34 restore the coupled signal to near ground level. The Transorb and Driver diode serves as an arc suppressor to protect the circuit.

There are two identical RS-232-B receive circuits on the deflection board, the receive data circuit consisting of Z3 and the carrier detect circuit consisting of Z1. The RS-232-B carrier detect signal enters the deflection card at pin 10 where diodes CR32 and CR33 clip the input at 5V and ground respectively. Gate Z1 produces a logic level out while R2 and C30 prevent any oscillation of the circuit caused by poor rise times of the input signal. The receive data circuit is identical in operation.

There are three identical RS-232-B transmit circuits on the deflection card. The RO Data Circuit consisting of Q33 and Q34, the Transmit Data Circuit consisting of Q35 and Q36 and the Request-to-Send Circuit consisting of Q37 and Q38. The data to be transmitted enters the



circuit at pin 51. The input is pulled up by R99 and clamped to 5V by CR31. When the input at pin 51 is positive, indicating that a mark is present, Q35 conducts, furnishing base drive to Q36 which conducts, causing the output at pin 52 to approach -12V. When the input at pin 51 is ground, indicating a space, Q35 does not conduct and Q36, having no base current, does not conduct. The output at pin 52 at this time is +14V. The resistor, R111, protects the output transistor Q36 from externally applied short circuits to ground.

The circuit consisting of Z3 and Q39 normally is the circuit used for the reverse channel transmit circuit, however, it may be used to provide a current loop interface circuit. The reverse channel signal from the Interface 2 card enters the deflection card at pin 47. The level at pin 18 is from the keyboard and is high, except when the BREAK key is depressed. When the output of Z3 pin 3 is low, the transistor Q39 does not conduct and the output at pin 56 is +14V. When Z3 pin 3 is high, the output at pin 56 is ground. When the BREAK key is depressed, the input at pin 18 goes low forcing Z3 pin 3 high and the output at pin 56 goes to ground.

A current loop interface, referred to earlier, may be provided if the circuit for Z3 and Q39 is modified. Using an Elco pin pusher, remove the contacts from connector locations 18, 47 and 56. Tape these wires and turn them back into the harness. Push the pin out of location 51 and

insert it into position 47. Push the pin out of location 52 and insert it in position 56. If the computer furnishes drive from a voltage source greater than 5V, the preceding modification is all that is required. If the computer drive is from a voltage source less than 5V, on the deflection card, resistor R88 must be shorted and a 10K ohm resistor added from connector pin 55 to a -12V source. With this modification, the transmitted data is available on J9 pin 3. Connector pins 1 and 7 are ground points.

## ADJUSTMENTS

Adjust deflection amplifier as follows:  
Connect electrical power and place master power switch to the ON position.

Fill screen with the letter "E". Observe screen for linearity. If necessary adjust magnetes on CRT yoke to obtain best rectangular shape.

To obtain desired line length adjust R41.

To obtain desired vertical length adjust R73.

Adjust R115 to center screen presentation horizontally and R114 to center screen presentation vertically, (if bow exist on left hand margin reverse leads on high voltage power supply.)

To obtain desired letter height adjust R116 (on earlier models R116 does not exist).

## LOGIC POWER SUPPLY

The Logic Power Supply consists of six separate supplies, operating from one common transformer. The voltages provided are:

1. +5VDC
2. -5VDC
3. -12VDC
4. +14VDC
5. +25VDC
6. -25VDC

The negative going pulse used for POWER ON RESET is developed from the REG +5VDC circuit within the Logic Power Supply.

On early models of the Datapoint 3300, an over-voltage protection circuit was incorporated to disable the +5VDC output if an over-voltage condition occurred.

The theory of operation deals with the +14 VDC supply. The same theory will apply to the +5 VDC supply. The -5VDC and -12VDC supplies are complements of the positive supplies.

The block diagram in figure 2-19 is typical of the functions within the 5, 12 and 14 volt supplies.

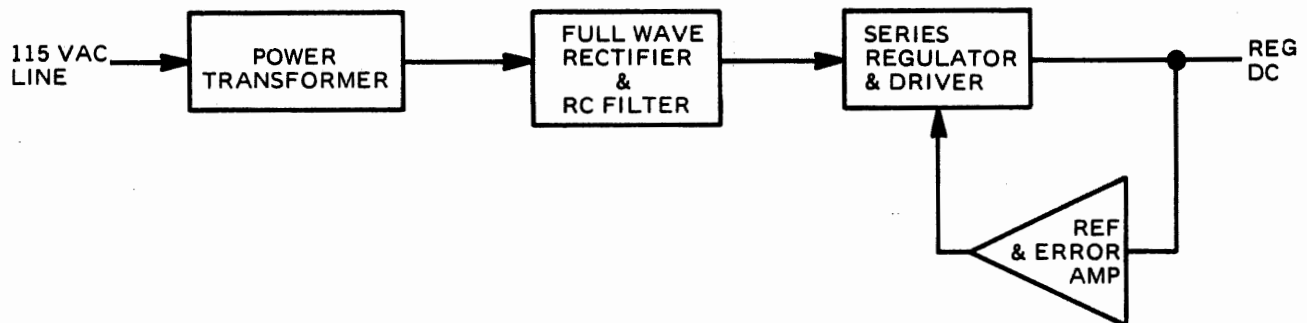
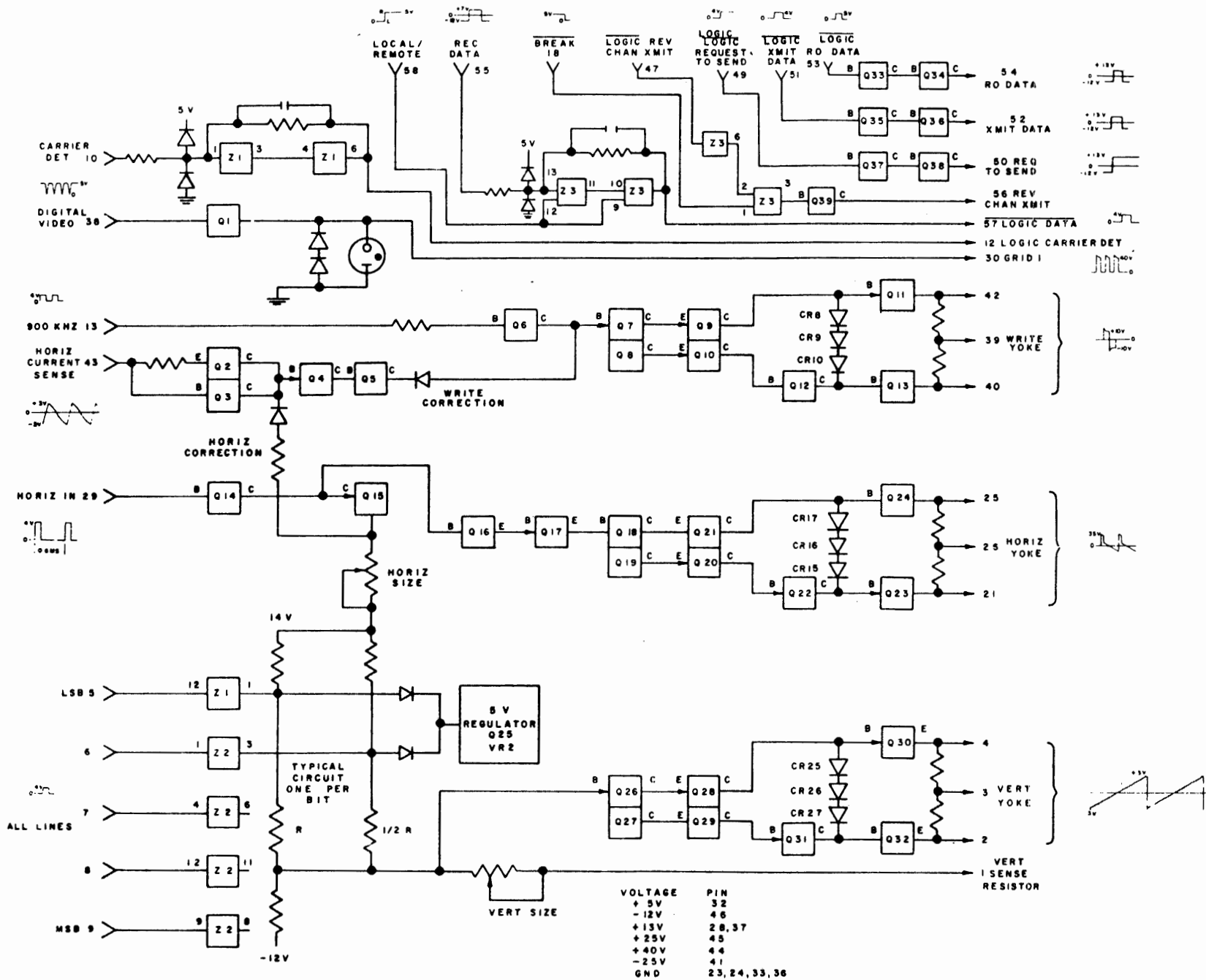
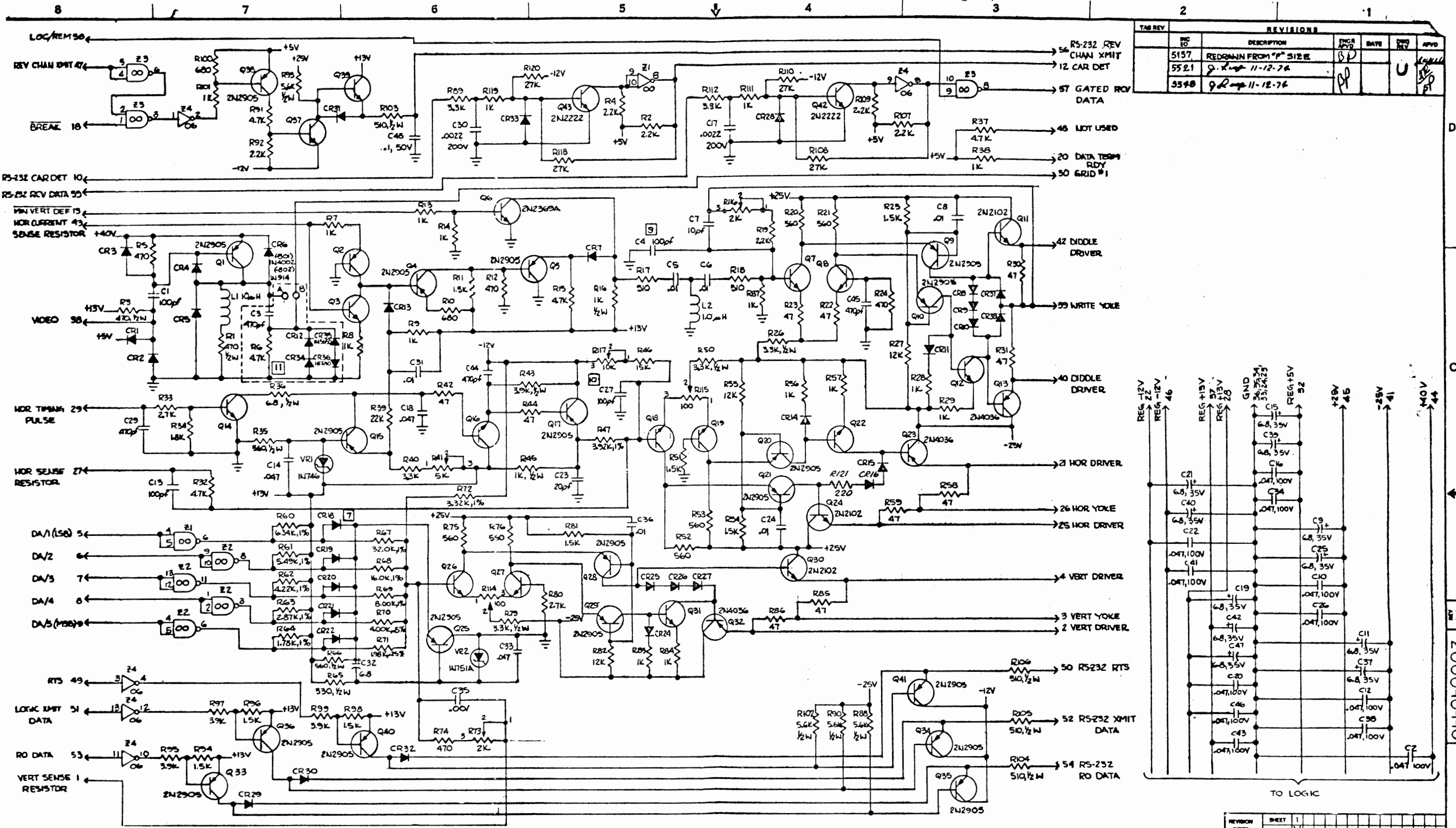


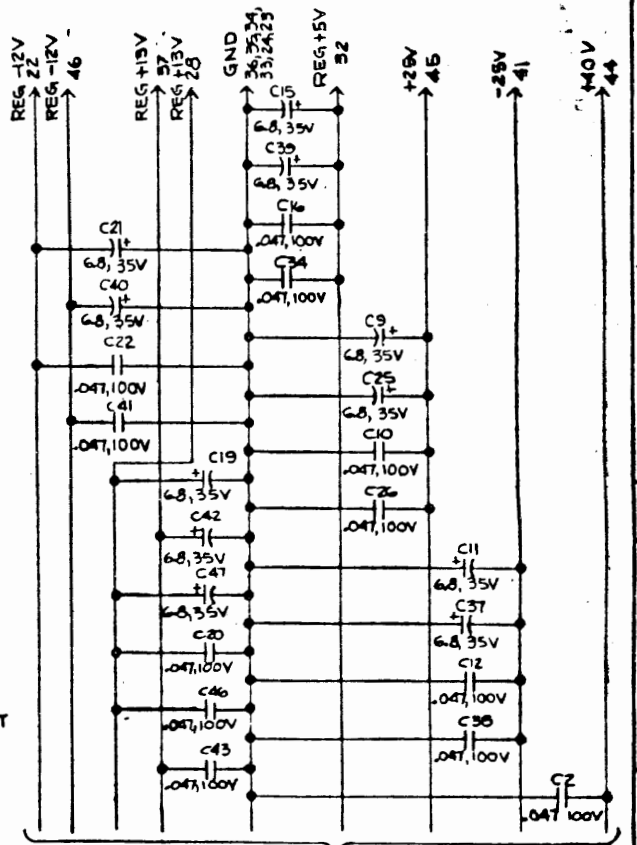
Figure 2-19. Typical Power Supply Block Diagram

Figure 2-20. Block Diagram, Deflection Amplifier





TAB REV	REV	DESCRIPTION	ENGR	DATE	REV	APVD
	5157	REDRAWN FROM "P" SIZE	BP			
	5521	Q. Rev 11-12-76				
	5548	Q. Rev 11-12-76				



- 7 CR8 thru CR22 MATCHED TO 10MV
  - 6 ALL TRANSISTORS ARE 2N2719A
  - 5 ALL DIODES ARE IN314
  - 4 ALL CAPACITANCE VALUES ARE IN MICROFARADS
  - 3 ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
  - 2 LOGIC SYMBOLS PER USA STD Y32-14
  - 1 ELECTRONIC SYMBOLS PER USA STD Y32-67
  - NUMBERS SHOWN BELOW REFERENCE DESIGNATIONS WITHIN LOGIC SYMBOLS ARE SEGMENTS OF VENDOR PART NUMBER DESCRIBED IN PARTS LIST
- NOTES: (UNLESS OTHERWISE SPECIFIED)

- 11 C3, R6, CR12, CR34, CR35, CR36 - 802 ASSEMBLY ONLY; JUMPER "A" "B" - 801 ASSEMBLY ONLY.
- 12 CAPACITOR "C27" MAY BE REMOVED OR ITS VALUE CHANGED BETWEEN 10 AND 500PF AS NECESSARY TO STABILIZE HORIZONTAL AMPLIFIER AT TEST ON -801 OR -802 VERSIONS.
- 13 "C4" IS 500PF ON "J" REV ARTWORK BOARDS ONLY
- 14 PINS ON DEFLECTION AMPLIFIER BOARD PLUG INTO CONNECTOR "J1"

Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10
00	12,13	3,11							
00	12,13	11							
06	5	6							

IC TYPE INPUT OUTPUT  
SPARE CHART

IC	TYPE	INPUT	OUTPUT
5N7400	7	14	
5N7406	7	14	
IC	GND	+5V	

VOLTAGE CHART

VR2	Z4	Q43	CR38	R121	C48	C28	LAST	NOT

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH.

TOLERANCE  
X = ±.02    XXX ±.010    L = ±.007

HOLE DIA. TOLERANCE  
Ø thru .250    .251 thru .500    .501 & up  
+.003    +.005    +.010  
-.002    -.003    -.005

THREADS: EXT 2A, INT 2B

DRAWN: *J.R. Boyd* DATE: 4-16-74

CHECKED: *J. Wolfhuhl* DATE: 9-28-74

ENGINEERING APPROVAL: *Bill Newton* DATE: 11/21/74

RELEASE: *R. Meland* DATE: 11-25-74

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REVISION INDEX	SHEET	REV	DATE	APVD
	1			

**Datapoint**  
975 Dabount Dr. San Antonio, Texas 78244

**SCHEMATIC DIAGRAM**  
**DEFLECTION AMPLIFIER**

PROJ: 01

DWG NO: 01-F01-0003

DATE: 2-67/(2-68 blank)

Figure 2-21. Deflection Amplifier

The three major sub-circuits of the +13VDC power supply (See figures 2-22 and 2-23) are as follows:

1. Diodes CR3 and CR4, CR17 and CR18 and capacitor C2 comprise the rectifier-filter circuit. Pins 13 and 14 from the power transformer provide in excess of 14VAC to rectifiers CR 3 and CR4, CR17 and CR18 with respect to ground. The pulsating DC from CR3 and CR4 is smoothed by the RC filtering action of C2.
2. The series regulator and driver circuit consists of series regulator Q1 and driver transistor Q2, resistor R1, Zener diode CR21 and capacitor C22. The series regulator circuit controls all current to the load from the rectifier-filter circuit in response to signals from the error amplifier. A driver circuit is provided in the base of the series regulator to increase the current gain of the error signal. All current to the load must flow through the series regulator Q1. Therefore, the voltage drop across Q1 for a given current will determine the voltage across the load. The drop across Q1 is solely dependent upon the feed-back signal from the error amplifier within the limits of regulator Zener diode, CR21 and resistor R1 limit the voltage drop across Q1 to a safe value. These two components do not appear in the 5 volt power supplies since a 5 volt drop is entirely within the capability of the series regulator transistor. Capacitor C22 in the base of Q1 assures a smooth and well damped response of Q1 to signals to the error amplifier.
3. The Reference and Error Amplifier is a common mode differential amplifier, consisting of transistors Q3 and Q4; resistors R2, R3, R4, R11, R33; Zener diode CR5 and capacitors C1 and C3. Since the amplifier is differential, many of the effects of heat and component aging are cancelled. Zener diode CR5 provides the reference potential on the base of Q3. When the potential at the base of Q4 is identical to that on the base of Q3, the amplifier is considered to be in balance, and no error signal results. Any deviation of the base of Q4 from the reference level of Q3 would result in an unbalanced condition. The resultant signal from the error amplifier would cause a change in base voltage on driver Q2 and

would ultimately vary the drop across Q1 to compensate for the deviation in supply voltage.

To clearly understand the operation of the 5, 12 and 13 volt power supplies, assume the +13 volts power supply to be operating at the nominal +13 volts DC level. Assume that due to variations of line or load or both, the voltage across the load exceeds +13VDC. Since the voltage to the load exceeds pre-set level the base of Q4 will become more positive. The drop across Q4 will decrease causing its emitter and therefore the emitter of Q3 to go more positive. Since the emitter of Q3 is now more positive with respect to its base (which is held at the reference potential), the current through Q3 will be diminished. The drop across R33 in the collector of Q3 will be less, causing the base of Q2 to go more positive. Q2, being a PNP transistor, will decrease its current to the base of Q1. When the base of Q1 goes less positive, the drop across Q1 will increase such that the voltage appearing on the output terminal of the power supply will again be the nominal 13 volts, and the voltage at the base of Q4 will return to the pre-set level.

Now assume that due to line or load variations the potential at the output terminal of the +13 volts power supply should drop below the nominal 13VDC value. The base of Q4 would go less positive decreasing the current thru Q4. The emitter of Q4 would then become less positive. Since Q3 and Q4 share a common emitter resistor, R4, the emitter of Q3 would also become less positive. Again, since the base of Q3 is held at a fixed reference potential, if the emitter becomes less positive the current through Q3 would increase, causing a greater drop across collector resistor R33. The base of driver, Q2, would therefore go less positive, increasing the current to Q1. The drop across Q1 would decrease, thus increasing the potential at the power supply output terminal to the nominal 13 volts.

Capacitor C1 provides additional filtering at the output terminal and minimizes variations in voltage which would exceed the response time of the regulator circuit. R11 provides a means of adjusting the output voltage to a nominal  $13 \pm 1$ VDC.

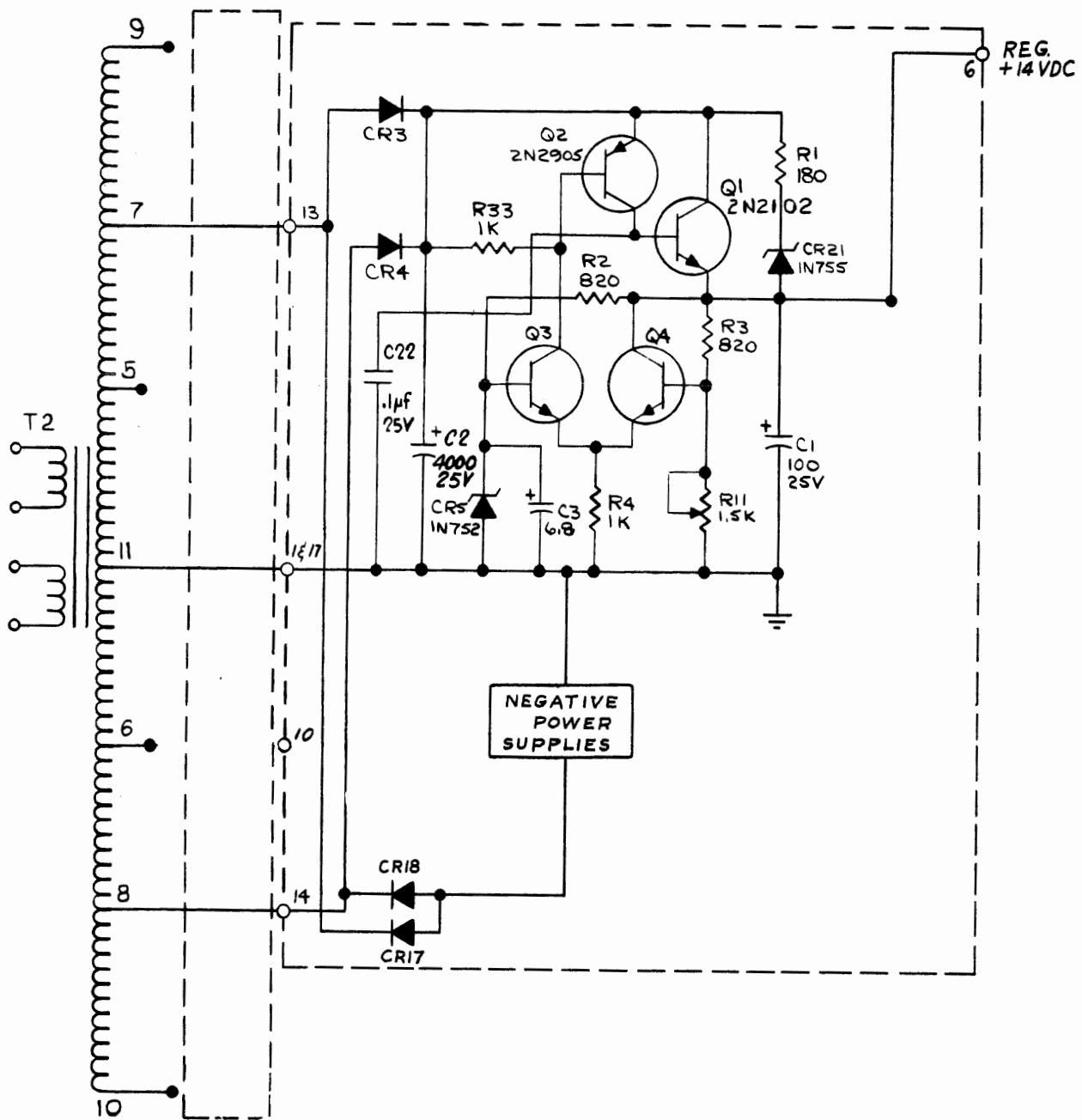


Figure 2-22. +14VDC Power Supply

The +25VDC and -25VDC used for the deflection drivers is obtained from transformer T2. Plus 25 volts is obtained by rectifying the output of T2 pins 9 and 10 across CR6 and CR7, CR8 and CR9. Filtering is accomplished with C17. The output is to the +25VDC fuse F2. Negative 25 volts is a complement of the +25VDC supply with filtering accomplished by C18. The output is to the -25VDC fuse F3.

### Power On Reset

The power on reset circuit consists of R13, C8, R17, Q15, R14, C7, R15, R16, Q18, R18, R19, R34 and Q16. (See figure 2-23.)

The purpose of the circuit is to provide a negative going pulse to the POWER ON RESET BUS during a brief interval following turn-on of the +5VDC supply, thus assuring a resetting of all logic elements each time power is recycled.

When power is first applied to the reset circuit, capacitors C8 and C7 will be discharged (C8 by R17 and C7 by R14, R15 to the +5VDC bus). The base of Q18 will immediately go sufficiently positive to turn off Q18. As a result, Q16 will be turned off.

Meanwhile, after a time constant determined by values of C8 and R13, C8 will charge to a value sufficiently positive to saturate Q15 bringing the negative side of capacitor C7 to approximately ground potential. For a brief time interval (determined by the values of C7 and R15), Q18 will saturate and remain in this state until C7 has charged, thus driving Q16 into saturation and providing a negative going pulse to the Power On Reset bus. As C7 charges, the base of Q18 will then become sufficiently positive to cut off Q16, thereby restoring the conditions which existed immediately following application of power.

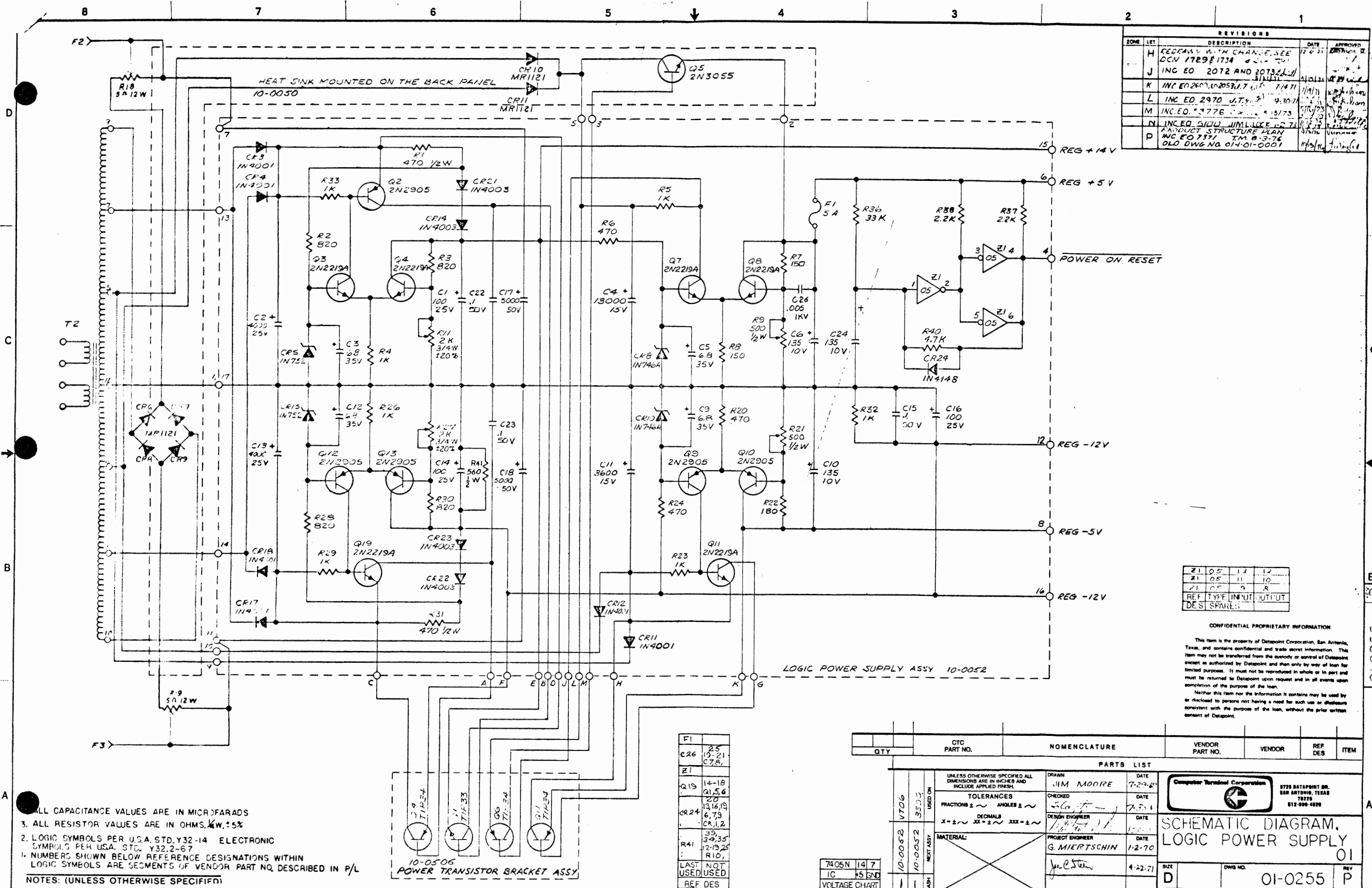
### DEFLECTION POWER SUPPLY

The Deflection Power Supply provides additional voltages for the deflection circuits. Figure 2-24 shows the +40VDC portion of the Deflection Power Supply.

Approximately 40VAC from transformer T2 is applied to the bridge rectifier, CR3 - CR6. The full wave rectified output is filtered by C2, R5 and C7 and is clamped by Zener diode CR5 to produce a +40VDC output at pin 6.

Figure 2-25 shows the circuitry which provides +120VDC and +450VDC to the deflection circuits. Approximately 550VAC from the secondary of T2 is applied to the power supply on pin 1. A +450VDC output on pin 4 is provided by rectifier CR1 operating in the RC filter R8 with C3 and C4. The +120VDC supply is derived from the +450VDC supply through divider R1 and R22. R2 and R3 are the bleeder resistors for the Deflection Power Supply.

Figure 2-26 is the schematic diagram of the complete Deflection Power Supply circuitry.



REVISIONS				
ZONE	LET	DESCRIPTION	DATE	APPROVED
H		REDRAWN WITH CHANGE, SEE DCN 1729 & 1734	12-2-71	[Signature]
J		INC EO 2072 AND 2073	11-11-71	[Signature]
K		INC EO 2607, 2653, 2707	7-14-71	[Signature]
L		INC EO 2970	9-30-71	[Signature]
M		INC EO 3776	5-15-73	[Signature]
N		INC EO 5102, 5111, 5122, 5172	11-12-73	[Signature]
P		PRODUCT STRUCTURE PLAN INC EO 7371, TM 8-3-76	8-11-76	[Signature]
		OLD DWG NO. 01-01-0001		

Z1	05	13	12
Z1	05	11	10
Z1	05	9	8
REF TYPE	INPUT	OUTPUT	
DES	SPARES		

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1. ALL CAPACITANCE VALUES ARE IN MICROFARADS  
 2. ALL RESISTOR VALUES ARE IN OHMS,  $\frac{1}{2}W, \pm 5\%$   
 3. LOGIC SYMBOLS PER U.S.A. STD. Y32-14 ELECTRONIC SYMBOLS PER U.S.A. STD. Y32.2-67  
 4. NUMBERS SHOWN BELOW REFERENCE DESIGNATIONS WITHIN LOGIC SYMBOLS ARE SEGMENTS OF VENDOR PART NO. DESCRIBED IN P/L

NOTES: (UNLESS OTHERWISE SPECIFIED)

F1	Q26	Z1	Q19	CR24	R41
25	19, 21, 27, 8		14-18, 15, 6	13, 16, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35	12, 19, 25, 31, 10
LAST USED	NOT USED				
REF DES					

7405N	147
IC	+5 GND
VOLTAGE CHART	

QTY	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM

PARTS LIST			
USED ON	DATE	DESIGN ENGINEER	DATE
V706	7-29-60	JIM MOORE	7-29-60
10-0052	7-20-71	[Signature]	7-20-71
10-0052	1-2-70	G. MIERTSCHIN	1-2-70
DASH	4-22-71	[Signature]	4-22-71

Computer Terminal Corporation	8728 BATAPPOINT DR., SAN ANTONIO, TEXAS 78288
SCHEMATIC DIAGRAM, LOGIC POWER SUPPLY	
01	01-0255 P
2-73/(2-74 blank)	

Figure 2-23. Logic Power Supply



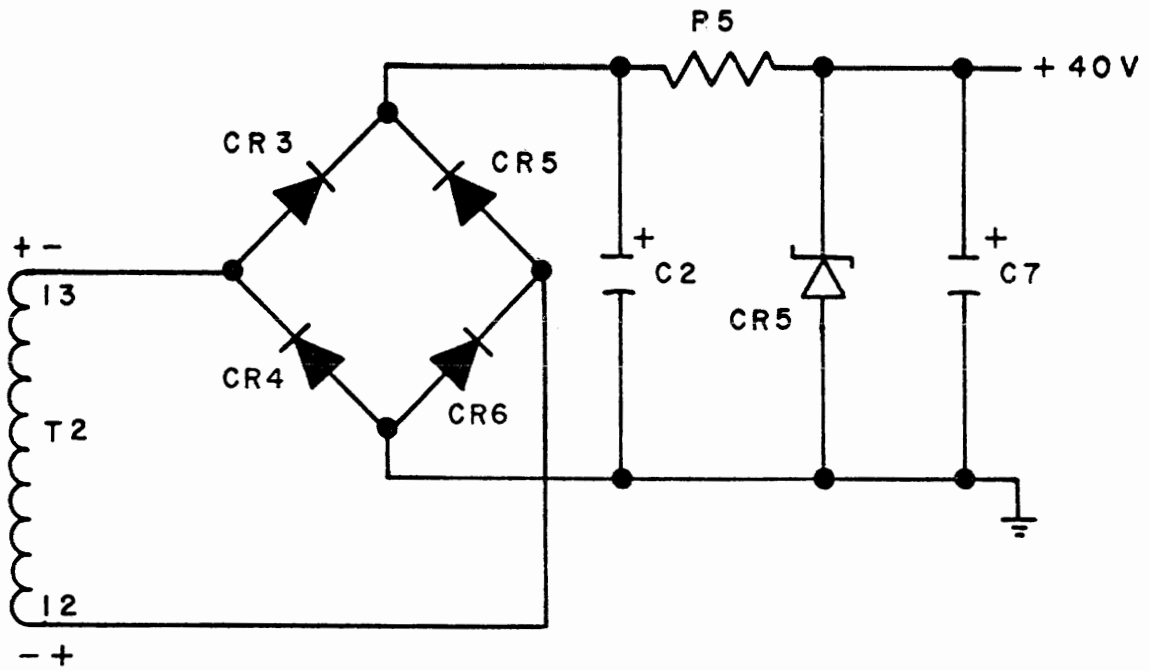


Figure 2-24. +40VDC Circuit

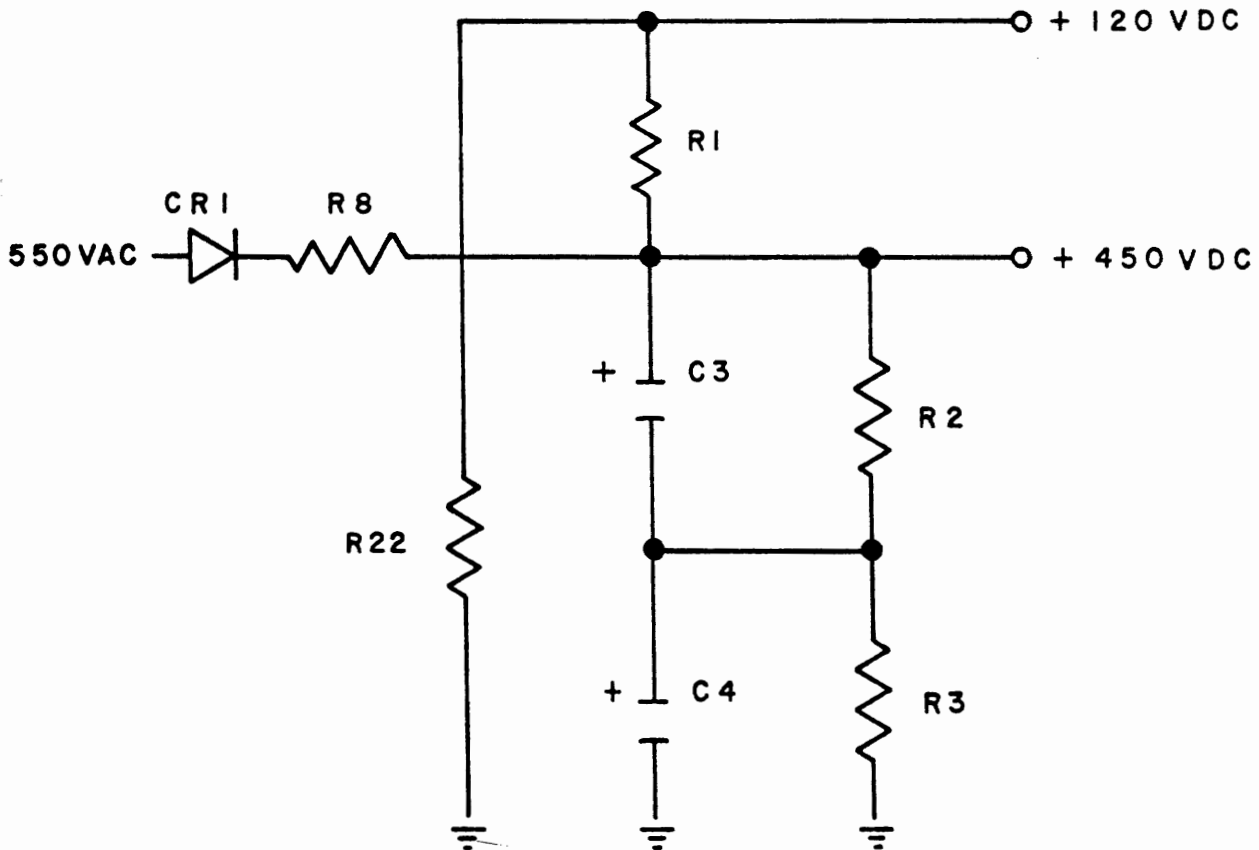
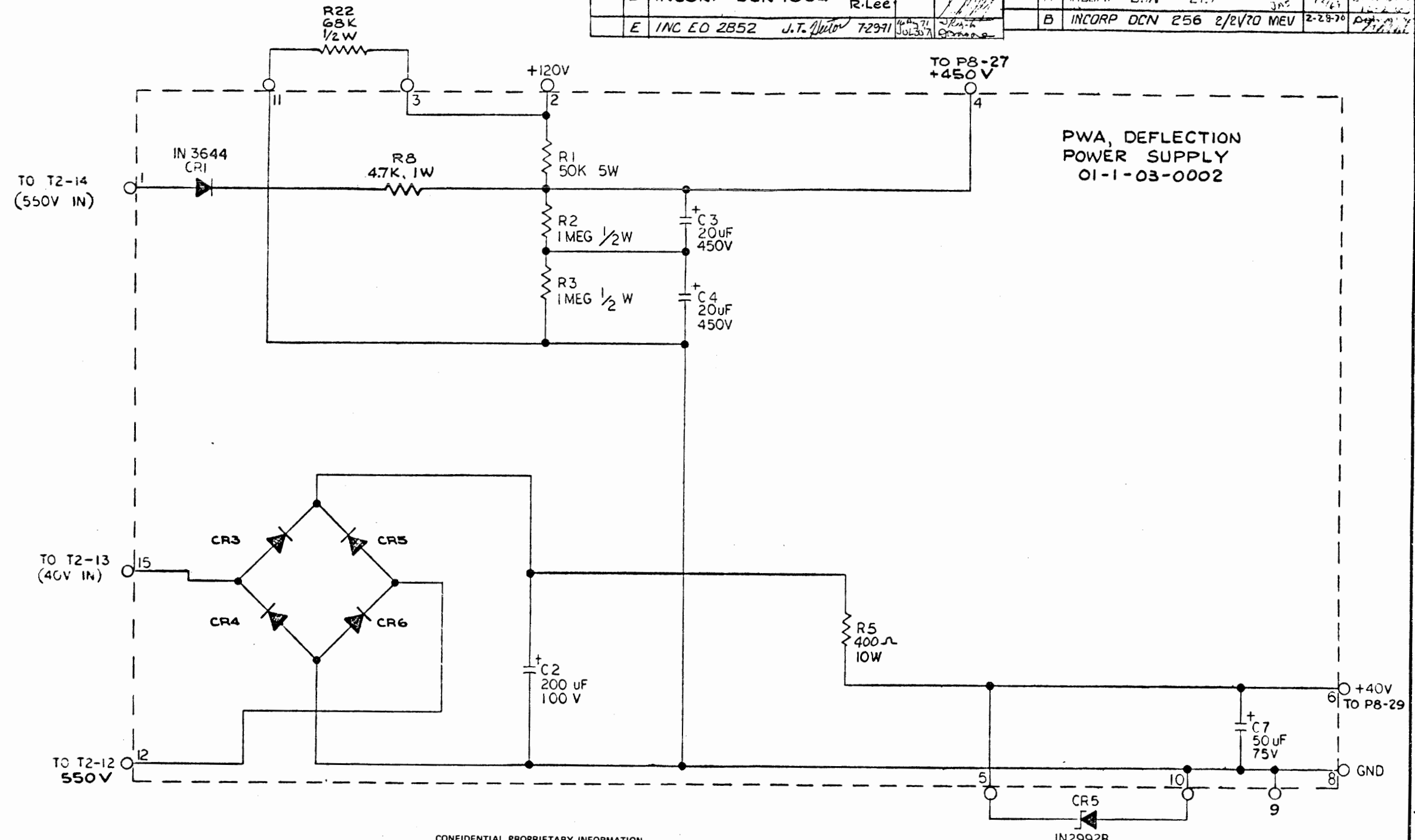


Figure 2-25. +120VDC and +450VDC Circuit

C	IN CORP DCN 1430	7-13-70	JRS	7-14-70	ADMOUC
D	IN CORP DCN 1604	10-31-70	R.Lee	10-12-70	ADMOUC
E	INC ED 2852	J.T. DeLo	72971	7-14-71	ADMOUC

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	IN CORP DCN # 219	JRS 12/2/69	ADMOUC
	B	IN CORP DCN 256	2/27/70 MEV	ADMOUC



PWA, DEFLECTION  
POWER SUPPLY  
01-1-03-0002

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- 2. RESISTANCE VALUES ARE IN OHMS.
  - 1. ALL DIODES ARE IN4003.
- NOTES: (UNLESS OTHERWISE SPECIFIED)

QTY REQD	NOMENCLATURE OR DESCRIPTION	IDENTIFYING NO.	MATERIAL OR NOTE	ITEM NO.
LIST OF MATERIALS				
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON FRACTIONS ± 1/64 DECIMALS ± .010 ANGLES ± 1/2°	DRAWN CHECKED DATE 7-30-69	SCHEMATIC DIAGRAM, DEFLECTION POWER SUPPLY	
01-1-03-0002	3300	APPD APPD APPD		
01-1-03-0002	VTO6	DESIGN RELEASES <i>[Signature]</i>	SIZE C	DWG NO. 01-1-01-0002
NEXT ASSY	USED ON		SCALE	WEIGHT
APPLICATION				SHEET 1 OF 1

Figure 2-26. Deflection Power Supply

01-1-01-0002

## HIGH VOLTAGE POWER SUPPLY

The High Voltage Power Supply is a sealed unit. When 95 - 135VAC, at 60 Hz, is applied to the input tab sockets, 15,000 VDC will be present at the output high voltage lead. If input voltage is correct and 15 KVDC is not present, replace the High Voltage Power Supply.

## CONTROL LOGIC

### General

The functions of the Control Logic card are

- (1) Generate the horizontal and vertical timing pulses.
- (2) Provide blanking pulses for horizontal and vertical retrace.
- (3) Control the cursor movements (i.e. left arrow, right arrow, up arrow and down arrow).
- (4) Provide line feed, carriage return roll up and roll down functions.
- (5) All compare circuitry for data entry into circulating memory.
- (6) All address counters for memory and cursor.

### Horizontal Deflection Timing (See Figures 2-27 and 2-28.)

The horizontal deflection timing pulses are generated by a synchronous binary counter, consisting of Z62 through Z65, referred to as the Character Counter. The Character Counter Clock and cycle 7 pulses to the input pins of Z65 will increment the counter each character time. The Character Counter counts to 82 although there are only 72 characters displayed per line. The ten extra counts are to allow for horizontal retrace and recovery of the yoke after retrace. The Character Counter has a normal radix of 128, therefore Z86, Z76 and Z75 provide the necessary feedback to turn the Character Counter around at count 82. Z86 decodes a count of 82 (a binary count of 81 is actually the 82nd count, since the first count is zero) and returns the Character Counter to the zero state with the next clock pulse.

The N jumper at pin 6 of Z86 is provided to aid in isolating a malfunction within the Character Counter and feedback circuit. With the N jumper removed, the feedback path is broken and the Character Counter will cycle through its radix of 128. The output of each succeeding flip-flop in

the counter chain will be twice the period of the preceding flip-flop. It is then a matter of determining whether the malfunction is in the counter chain or in the feedback path.

The horizontal ramp clock is generated by Z33, which is connected in a standard latch configuration. Z84 decodes the 72nd count and the output at pin 8 of Z84 is connected to pin 9 of Z33. When the 72nd count is detected, Z84 pin 8 drives Z33 pin 9 low, setting Z33 pin 8 high. At this point, Z63 pin 8 which connects to Z33 pin 13 is high. On the 80th count, Z63 pin 8 will go low, setting Z33 pin 11 to a high and resetting Z33 pin 8 to a low. The horizontal ramp is generated when Z33 pin 8 goes from a high to a low and is terminated when Z33 pin 8 goes from a low to a high. The horizontal sweep begins (left hand margin of the CRT) with the 81st count and ends (right hand margin of the CRT) with the 72nd count. The 81st and 82nd counts are not used to display information but do allow time for the horizontal yoke to gain speed. The function of the Clock Inhibit signal is to inhibit the clock pulses to the MOS recirculating register during horizontal retrace. Z66 pin 1 goes low on count 72 and remains in this state until the Character Counter cycles to the first count (zero state).

### Vertical Deflection Timing

The vertical deflection sweep is generated by a synchronous binary counter which consists of Z60 through Z62 and is referred to as the Line Counter. Feedback is provided to change the Line Counter natural radix of 32 to a radix of 26. Z79 pin 12 goes low on the 26th count (binary count of 25 since zero is the first count) and in conjunction with Z70 pin 11 and Z13 pin 4, steer the counter-back to the zero state on the next clock pulse. The clock pulse to the Line Counter is generated by the Character Counter. Z84 decodes the 72nd count of the Character Counter and this count is inverted by Z75 to be applied to pin 2 of Z13. (Pin 3 of Z13 and pin 10 of Z12 will be considered at this time to be in the high state.) The pulse is gated through Z13 and Z12 and applied to Z82 which is an inverting buffer. Z82 has an extended fan-out capability and applies a low going clock pulse to the Line Counter.

The D/A 1 through D/A 5 outputs of the Control Logic card are the Q outputs of the Line Counter flip-flops. These outputs are used to drive the Digital-to-Analog converter which generates the vertical sweep signal. The End-of-Frame signal which leaves the Control Logic card on connector pin 16 is generated by JK flip-flop Z39 pin 8. The K input, pin 10 of Z39, is steered by Z79 pin 12 which is the decoded 26th count. The output of Z79 pin 12 is inverted by Z70. Pin 11 of Z70 drives the J input, pin 7 of Z39. The following clock pulse which sets the Line Counter to the zero state, clocks Z39 pin 8 low. Z39 pin 9 connects to Z66 pin 12. Z66 pin 1 is wire-ORed with Z66 pin 1 which is the horizontal retrace clock inhibit signal. Z39 pin 9 stops high during the vertical retrace until the end of the first horizontal sweep. This forces Z66 pin 13 low during this period of time to inhibit the recirculating memory clock. In order to allow time for the recovery of the horizontal yoke after vertical retrace, the first horizontal sweep is not used to display information. This is why the Line Counter has a radix of 26 rather than a radix of 25. The End-of-Frame signal and the Clock Inhibit signal are gated together by Z12. The output, pin 11 of Z12, leaves the deflection card on connector pin 47 and is referred to as the Blank CRT 1 signal. This signal is used to blank the CRT display during the horizontal retrace and the vertical retrace. The 76th count of the Character Counter is decoded by Z83, inverted by Z72 and leaves the Control Logic card on connector pin 42. This signal is used on the MOS card to perform the Erase-End-of-Line function. The End-of-Frame signal is used to perform the Erase-End-of-Frame function.

### **Cursor Positioning**

The positioning of the cursor on the CRT display is controlled by the Cursor Character Counter and the Cursor Line Counter. The Cursor Character Counter is an up-down 72 count counter, consisting of flip-flops Z43, Z44, Z45 and Z46 with their associated steering gates. The Cursor Line Counter is an up-down 25 count counter, consisting of Z40, Z41 and Z42 with their associated steering gates. The outputs of these two counters are compared to the outputs

of the Memory Character Counter and the Memory Line Counter. These four counters are compared by Z50, Z51, Z52, Z54 and Z55 whose outputs are wire-ORed. The binary outputs of the Cursor Character Counter and the Cursor Line Counter indicates the location of the cursor in the CRT display. The output of the digital comparator, pin 9 of Z69, will remain low as long as the four counters are not in agreement. When the two sets of counters compare, the comparator output will go high for a single character time. The pulse width of the digital comparator is narrowed by gating it with three signals from the MOS card. The digital comparator, Cycle 1, Dot gate and the Character Counter Clock are ANDed together by Z69. The digital comparator output is inverted by Z69 and the pulse width is reduced to a single dot time. The output of Z69 on pin 8 leaves the card on connector pin 18 and this same output is inverted by Z59 pin 13 to provide the Comparator Output from the card on connector pin 19.

The first character position on a line is represented by the zero state of the Cursor Character Counter. In order to move the cursor to the right on the display, the Cursor Character Counter is incremented up, to move the cursor to the left the Cursor Character Counter is incremented down. The steer up and steer down lines of the Cursor Character Counter are jumpers A and L respectively. These lines are normally high. To steer the counter up, jumper A remains high while jumper L is pulled low. To steer the counter down, jumper A is pulled low while jumper L remains high. Jumpers A, L and K are provided into the counter so that trouble-shooting the counter may be simplified. By removing these jumpers, external steering controls and an external clock may be applied to the counter. The Cursor Line Counter is implemented in a similar manner to the Cursor Character Counter. Jumpers E and B represent the steer up and steer down lines respectively, of the counter. By removing jumpers E, B and C, external steering controls and an external clock may be applied to the Cursor Line Counter. It was noted earlier that the Line Counter used to generate the vertical deflection is a divide by 26 counter. The

first horizontal line after vertical retrace, is used to allow time for the horizontal yoke to recover rather than to display information on the CRT. The outputs of the first flip-flop, Z42 pins 9 and 8 in the Cursor Line Counter, are reversed from the normal configuration in that the  $\bar{Q}$  output of Z42 is wired into the digital comparator as the Q input. This prohibits a comparator output for the first horizontal deflection line and allows a comparator output for the second horizontal deflection line. This means that the home up position is actually the first character in the second horizontal sweep. This allows time for the horizontal yoke to recover and gain speed after vertical retrace.

The Cursor Right, Cursor Left, Cursor Up and Cursor Down functions are decoded commands from the computer to increment the Cursor right, left, up or down. These commands are decoded on the Interface 1 card and are inputs to the Control Logic card. The Left Arrow, Right Arrow, Up Arrow and Down Arrow function are switch closure commands from the keyboard to move the cursor left, right, up or down. The Left Arrow, Right Arrow, Up Arrow and Down Arrow commands out of the Control Logic card are functions that indicate a keyboard switch has been closed. These outputs are wired back to the keyboard where they are encoded and then transmitted to the computer.

The Cursor Right function enters the Control Logic card on connector pin 9 and follows two paths. The first path is through Z78 pin 2, which inverts the signal and applies the inverted signal to Z57 pins 11 and 12. Z57 pin 13 is connected to jumper L, the steer down line and goes low to steer the counter up. The second path followed by the Cursor Right signal is to Z78 pin 4 where the signal is gated and inverted. Z78 pin 6 then connects to Z78 pin 9 and uprights the signal. Z78 pin 8 connects to Z28 pin 4. Z28 is a four input NAND gate. The other three inputs to the gate at this time are high, therefore with Z28 pin 4 going low, Z28 pin 6 goes high. Z28 pin 6 connects to Z7 pin 10 where it is gated with count 76 from the Character Counter. The output of Z7 pin 8 sets a latch, consisting of Z8 pins 1, 2 and 3 and Z7 pins 1, 2, 12 and 13. The output, Z8 pin 3, of the latch is gated with count 82 by Z8 pins 11, 12 and 13. Z8 pin 11 sets a second latch which resets Z8 pin 3 to a

low. The output of the first latch now has a pulse on it which lasts from count 76 of the Character Counter until count 82. This pulse is inverted by Z16 pins 11, 12 and 13 and then gated, by Z16 pins 8, 9 and 10, with the normally high Cursor Advance Signal from connector pin 57. Z16 pin 8 is gated by Z26 with Z15 pin 8. Z15 decodes the zero state of the Cursor Character Counter and its output is high when clocking the Cursor Character Counter up. The output of Z26 is inverted by Z32 which drives the Clock line to the Cursor Character Counter. Since the steer down line had previously been pulled low, the application of the clock to the Cursor Character Counter by Z32 will now clock the counter up by one. The second latch, consisting of Z8, pins 4, 5, 6 and 8, 9 and 10, which was set by count 82, will be reset by Z28 pin 6 on the trailing edge of the data pulse. The output, Z8 pin 8 of this latch is inverted and buffered by Z86 and Z82 and leaves the Control Logic Board on connector pin 43. This signal, referred to as Line Feed Accepted, clears the holding register on the Interface 2 card and informs the Interface 2 card that the desired function has been completed. The Cursor Left function is performed in a similar manner to the Cursor Right function. The difference being that the steer up line (jumper A) is pulled to ground and the steer down line (jumper L) remains high. The Cursor Left clock path is also through Z28 pin 6. The clock pulse may be checked at Test Point 2.

The Cursor Up function enters the Control Logic Card on connector pin 34 and is normally high. The steering path for the Cursor Up function is through Z77 pin 12 and Z57 pins 5 and 6. Upon application of the Cursor Up signal, Z57 pin 4 drives the steer up line, jumper E, of the Cursor Line Counter low. The clock path for the Cursor Up function is through Z77 and Z28 pin 9. Upon application of the Cursor Up signal, Z28 pin 8 (Test Point 1), is driven high. The logic high signal on Test Point 1 is gated by Z17 with count 76 of the Character Counter. The output, Z17 pin 8, sets a latch which is reset by a second latch at count 82 of the Character Counter. (This technique is similar to that used for Cursor Right and Cursor Left.) The output of the first latch, Z58 pin 3, is wired through Z59 pins 4 and 5. The signal is passed by Z20 and presented to Z1 pin 11. Z1 pin 9 is connected to Z21 pin 8. Z21

decodes the zero state of the counter and inhibits clock pulses to the counter when the all zero state and a steer up signal are detected. Z1 pin 10 is connected to Z69 pin 6 which decodes the 25th count, corresponding to the 25th line. Z69 inhibits clock pulses to the counter when the 25th count and a steer up command are detected. If neither one of these states is detected by Z21 or Z69, Z1 pin 8 will present the pulse to Z32 to drive the clock line to the Cursor Line Counter. The Cursor Line Counter will then be incremented down by a single count.

The Cursor Down function is accomplished in a similar manner to that of Cursor Up. The steering path is through Z77 and Z57 pin 1. Z57 pin 1 drives jumper B low thus allowing the Cursor Line Counter to be incremented up. The clock path is through Z28 pin 8, Test Point 1, and may be checked at Test Point 1.

Switch bounce protection circuitry for allowing automatic repeating of the function after a slight delay are provided for these signals. The switch closure corresponding to the Cursor Right movement enters the card on connector pin 8 and is normally high. The steering path for this function is through Z78 and Z57. Upon application of the Right Arrow signal, Z57 pin 13 drives the steered down line, jumper L, low, thus allowing the Cursor Line Counter to be incremented up. The clock path for the Right Arrow signal is through Test Point 2. The switch closure is inverted by Z67, pin 11 the output, is connected to Z37 pin 11. The signal is still "bouncy" at this point and is inhibited by Z37 pin 10. The inverted switch closure from Z67 pin 11 is applied to Z47 pin 11. This forces Z47 pin 13 low, thereby setting a latch consisting of Z48 pins 11, 12 and 13 and Z48 pins 8, 9, 10. Z48 goes low and is connected to the input of Z38 pins 8 and 9 in O1 gate. The output, Z38 pin 10, is connected to an RC filter, consisting of R19 and C2, which smoothes out the switch bounce. After the filtering action, C2 charges up and forces Z49 pin 6 to go low. Z49 pin 6 sets a latch consisting of Z49 pins 8, 9 and 10 and Z49 pins 1, 2 and 3, forcing Z49 pin 8 to go high. Z49 pin 8 connects to Z37 pin 10. Since Z37 pin 9 is normally high, the bounceless switch closure is gated out of Z37 pin 8 which connects to Z28 pin 2. This forces Test Point 2 to go to a

logic 1 state. From Test Point 2, the generation of the clock pulse for the Cursor Character Counter follows the identical path for the Cursor Right and Cursor Left functions.

If the Cursor Control switch is depressed and held, Z38 pin 13, will begin to charge C1. After a short delay, the charge on C1 is sufficient to forward bias CR1 and Q1. The collector of Q1 is connected to Z27 pin 5. Q1 going into saturation forces Z27 pin 6 high. Z27 pin 6 is connected to Z27 pin 12 where it is gated with a 7.5 Hertz signal which enters the Control Logic card on connector pin 36. The 7.5 Hertz will then be passed through to either Test Point 1 or Test Point 2, where continuous clock pulses for either the Cursor Character Counter or the Cursor Line Counter will be generated.

### **Carriage Return**

The Carriage Return function is performed by clearing the Cursor Character Counter to the zero state. The Carriage Return signal enters the card on connector pin 39 and normally is a logic one. When connector pin 39 is pulsed, Z29 pin 8 is driven to a logic zero through a series of inverters and wired OR connections. Z29 pin 8 is connected to the Clear Inputs of the Cursor Character Counter and clears the counter.

### **Home Up**

The Home Up function is performed by clearing both the Cursor Character Counter and the Cursor Line Counter to the zero state. There are three command signals which will home the cursor display up. These are:

1. The Power On Reset pulse.
2. The Decoded Home Up command.
3. The Home Up key switch closure.

The Power On Reset pulse enters the card on connector pin 6, the Decoded Home Up command enters the card on connector pin 5 and the Home Up key switch closure enters the card on connector pin 17. These three signals are normally a logic one and are gated together by Z68. If any of the signals are pulsed, Z68 pin 12 goes high and through a series of inverters and

wired OR gates, drives Z29 pin 8 low and clears the Cursor Character Counter to the zero state. Z29 pin 6 is also driven low, thus clearing the Cursor Line Counter to the zero state.

### Home Down

The Home Down function is performed by clearing the Cursor Character Counter to the zero state and by counting the Cursor Line Counter to the 25th line with a burst of high speed clock pulses. Connector pin 11 is wired to the decoded home down command and connector pin 12 is wired to the Home Down key switch closure. These inputs are gated by Z78 and normally are a logic one state. When either of these inputs is pulsed, Z29 pin 8 is driven low and clears the Cursor Character Counter. Z59 pin 1 is connected to the steer down line of the Cursor Line Counter and is driven low. Z59 pin 8 is driven high and enables Cycle 3, a high speed clock, to be gated out on Z59 pin 10 which is the clock path for the Cursor Line Counter.

### Line Feed and Reverse

The Line Feed function has two standard operating modes. When the Datapoint 3300 is not operated in conjunction with the 3300T (companion magnetic tape cassette unit), Line Feed steps the cursor down to the 25th line of the display, one line at a time. Upon reaching the bottom line, each succeeding Line Feed will perform the Roll Up function. When the Datapoint 3300 is operated with the Tape Cassette 3300T in the read reverse mode, the Line Feed steps the cursor up the screen to the first line, one line at a time. Each succeeding Line Feed rolls the information down. These two modes of operation are controlled by the reverse line which enters the Control Logic card on connector pin 15. When the Datapoint 3300 is not operating with the 3300T, the reverse line is grounded through the 50 pin Tape Cassette Unit connector on the back panel of the Datapoint 3300. This explanation will consider the Reverse line to always be at ground level. The Line Feed signal enters the Control Logic card on connector pin 27 and is normally a logic one state. The Line Feed signal connects to Z28 pin 10 and when pulsed, drives Z28 pin 8, Test Point 1, high. A pulse applied to Test Point 1 will generate a clock signal to the Cursor Character Counter.

The logic zero level of the reverse line is inverted by Z10 and applied to Z9 pin 3. Z9 pin 2 is connected to the inverted Line Feed pulse. The output, Z9 pin 1, is connected to the steer down line of the Cursor Character Counter. When Line Feed is pulsed, the steer down line of the Cursor Line Counter will be lowered and a clock pulse will be generated to increment the counter up, this will move the cursor down on the display. The clock pulse will be applied to Z1 pin 11. Z69 detects whether or not the cursor is on the 25th line. If the cursor is not on the 25th line, the output, Z69 pin 6, will be high and the clock pulse will be gated through Z1. This will increment the Cursor Line Counter by 1. If, however, the cursor is on the 25th line, Z69 pin 6 will be low and the clock will be inhibited. The output of Z69 is inverted by Z20 and gated by Z19 with a not reverse line. Z19 pin 8 goes low forcing Z19 pin 6 high. Z19 pin 6 is connected to Z7 pin 3. Z7 pin 5 is connected to the inverted line feed pulse. Z7 pin 4 is connected to Z33 pin 6 which is a clock pulse generated from Test Point 1. The clock pulse is gated through Z7 and inverted by Z10. The output, Z10 pin 8, is gated by Z9 with the not reverse line. The clock pulse is gated out of Z9 on pin 13 and applied to Z6 pin 10. By applying this pulse to Z6, the Roll Up function is initiated.

### Roll Up

The function of rolling up information displayed on the CRT is performed by slipping sync between the vertical deflection and the MOS recirculating memory. The clock pulses to the Memory Character Counter are inhibited for a particular count while the MOS recirculating memory clock pulses are continued. This has the effect of holding the horizontal sweep in the same vertical position for two horizontal line times, while the information contained in the memory is advanced two line times.

The Roll Up signal enters the Control Logic card on connector pin 44 and is normally a logic high. This signal connects to Z6 pin 9. Z6 pin 10 is activated by the Line Feed function. If either of these input pins to Z6 is pulsed, the output, Z6 pin 8, is forced to a logic high. The signal is then gated by Z6 with the 82nd count of the Character Counter and the End of Frame signal. End of frame goes to a logic 1 at the beginning



of vertical retrace and gates count 82 through Z6. This forces the output, Z6 pin 6 low, setting a latch consisting of Z5 pins 1, 2 and 3 and Z2 pins 8, 9, 10 and 11. One output of the latch, Z2 pin 8, is set to a logic 0 and gated by Z13 with the clock pulse for the line counter. This condition is maintained until the following count 82 of the Character Counter is gated through Z4 pin 8, which resets the latch circuitry. Since Z13 pin 3 was held at a logic 0 for a complete line time, the clock pulse to the Line Counter was inhibited and the Line Counter remained in the all zero state. Following vertical retrace, the recirculating memory clock is inhibited during the first horizontal sweep since this line position is not used for displaying data. The memory clocks are inhibited by wired OR gates Z66 pin 13. Z2 pin 8 however, holds Z66 pin 13 at a logic 1 during the Roll Up process thus allowing the memory clocks to continue. The recirculating memory then has advanced the information one line time while the Line Counter has remained in the same state for two counts. Information displayed on the first line of the CRT prior to the Roll Up command must be erased. This is accomplished on the MOS board by the load 0's 1 pulse which leaves the Control Logic card on connector pin 58. This signal is the inversion of Z2 pin 8, by Z13 pin 10.

### **Roll Advance**

Roll Advance enters the Control Logic card on connector pin 31. This signal is used as a Roll Up command when the cursor is located on the 72nd character of the 25th line. Roll Advance is gated by Z1 with two control lines to detect that the 72nd character of the 25th line has been written. The Roll Advance pulse is gated through Z11 and applied to Z6 pin 12. This initiates the Roll Up function.

### **Roll Down**

The Roll Down key switch closure enters the Control Logic card on connector pin 10. The

switch bounce is filtered out by R19 and C2 before the signal is gated through Z18. Z18 pin 13 is wire ORed with Z9 pin 10 (a function of the line feed signal on the Datapoint 3300 when it is operated with the 3300T). These signals connect to Z2 pin 3, a three input gate connected in a latch configuration with Z11 pins 8, 9 and 10. Z2 pin 3 going low, forces Z2 pin 6 to a logic one. This signal is gated by Z4 with count 76 from the Character Counter and the End of Frame signal. End of Frame is high except during the time of vertical retrace and therefore allows count 76 to be gated through Z4 at any time except vertical retrace. The output of Z4 pin 6 sets a latch consisting of Z3 pins 1, 2 and 3 and Z1 pins 3, 4, 5 and 6. One output of the latch, Z3 pin 3, is inverted by Z13 and wired with Z13 pin 1 which is the clock pulse for the line counter. The second latch consisting of Z3 pins 8, 9 and 10 and Z3 pins 4, 5 and 6 is set on count 82 and resets Z13 pin 13 to a high. The remaining latch circuitry is reset on the following count 72 of the Character Counter. By adding an additional clock pulse to the Line Counter, sync is momentarily lost while the vertical sweep moves one full line time ahead of the recirculating memory. When Z4 pin 6 went low, following count 76, a latch consisting of Z80 pins 8, 9 and 10 and Z80 pins 4, 5 and 6 was set. Z80 pin 8 leaves the Control Logic card on connector pin 25 and is referred to as the Blank CRT2 signal. This signal is initiated at the beginning of the Roll Down function and is used to blank the CRT during the Roll Down process. Z80 pin 8 is gated with count 72 and Z39 pin 12 by Z79, Z39 pin 12 goes high at the beginning of the second horizontal sweep (first horizontal sweep display). This gates Z79 pin 8 low, setting a latch consisting of Z80 pins 1, 2 and 3 and Z70 pins 1, 2 and 3. The output of this latch, Z70 pin 3, leaves the Control Logic card on connector pin 23 and is referred to as the Load 0's 2 signal. This signal is used to erase information in the recirculating memory that has been positioned on the bottom line prior to the Roll Down signal. The latch circuitry is reset on count 72 by Z80 pin 11.



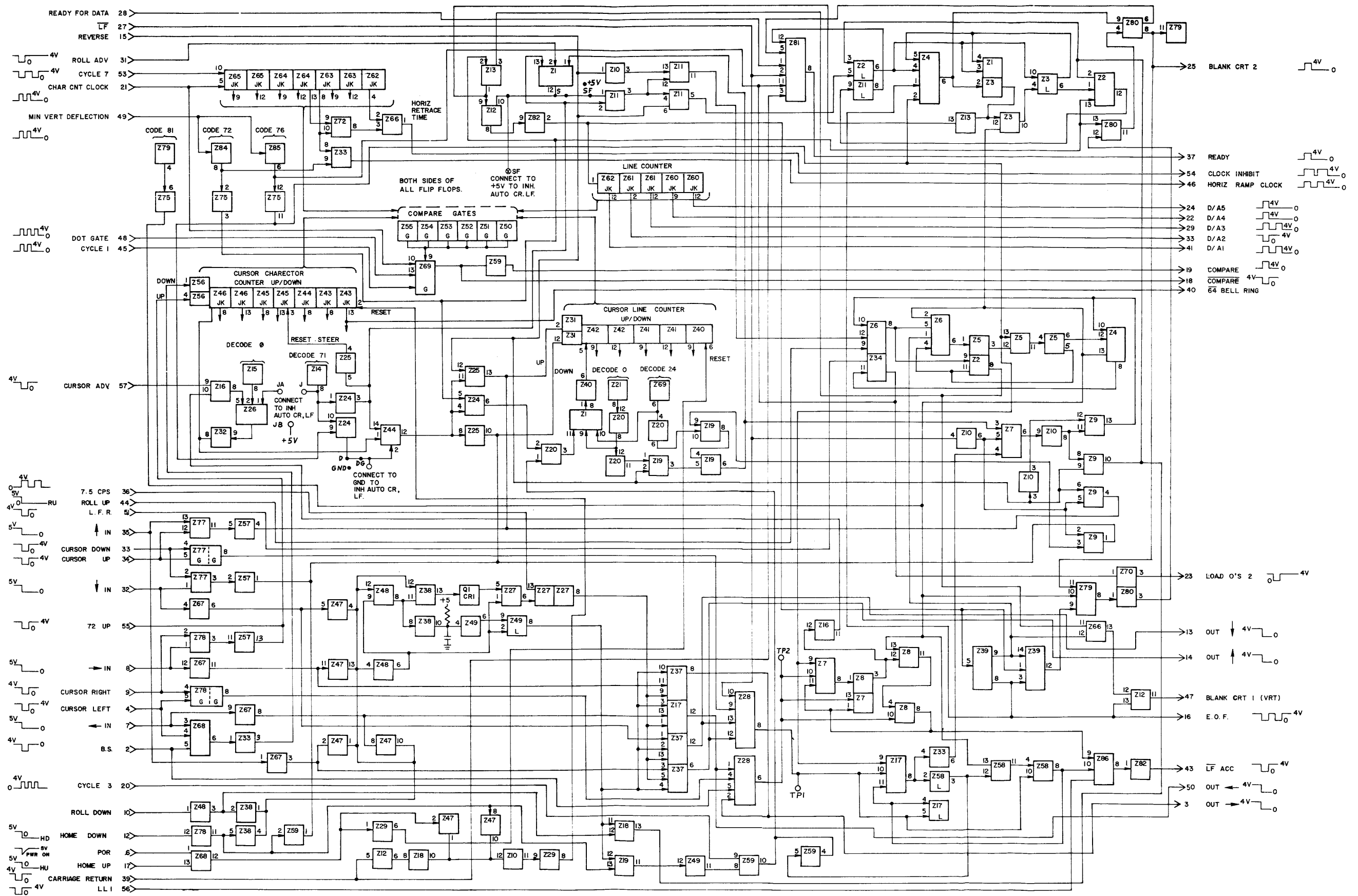
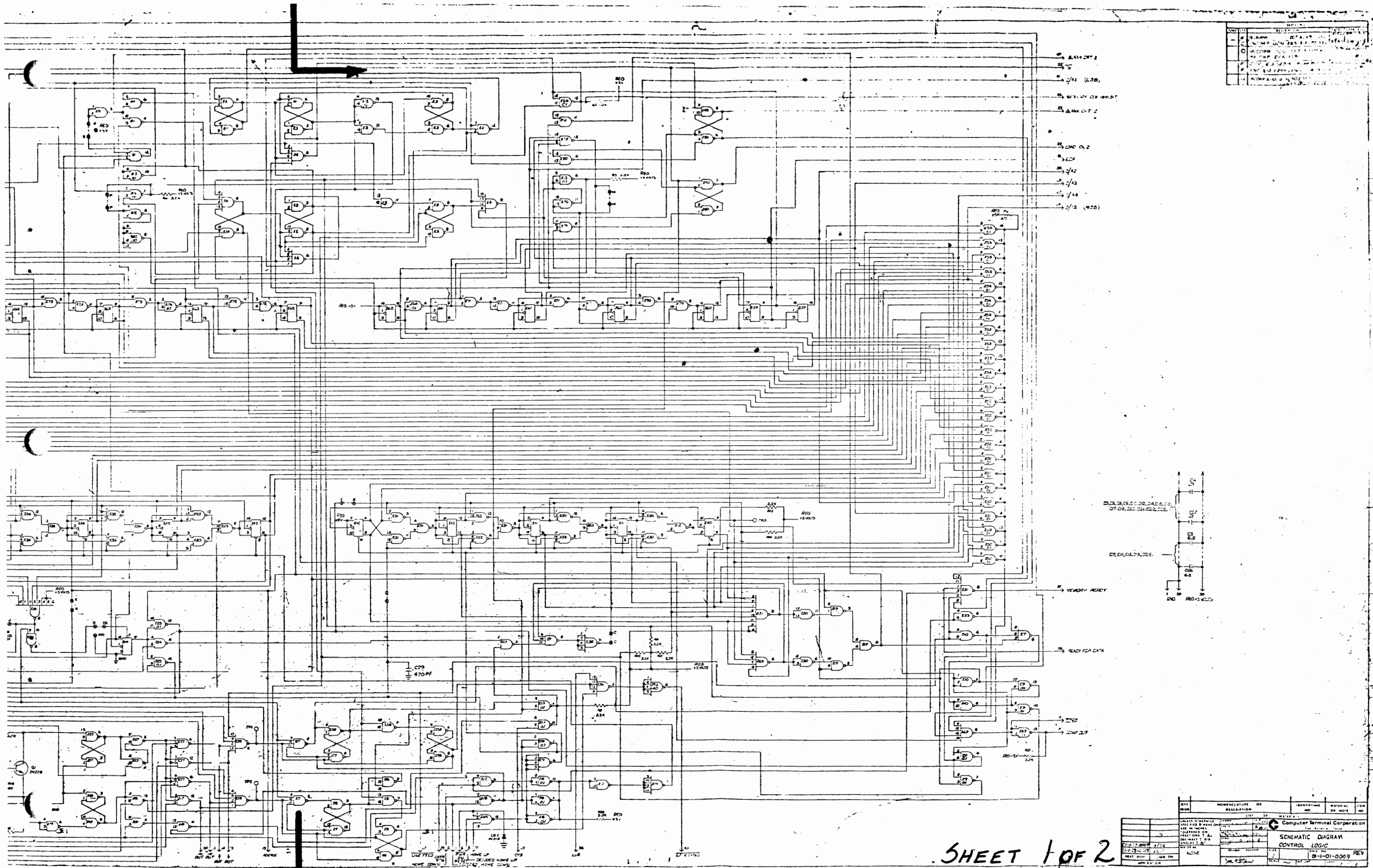
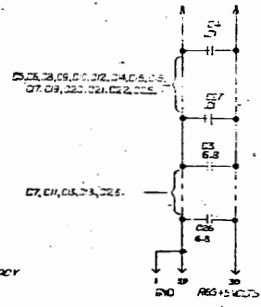


Figure 2-27. Block Diagram, Control Logic



REV	DATE	BY	CHKD
1	10/1/58	J. J. ...	...
2	10/1/58	J. J. ...	...
3	10/1/58	J. J. ...	...
4	10/1/58	J. J. ...	...



SHEET 1 OF 2

QTY	DESCRIPTION	IDENTIFYING NO.	MATERIAL OR NOTE NO.	ITEM NO.
1	Computer Terminal Corporation			
1	SCHEMATIC DIAGRAM			
1	CONTROL LOGIC			
1	0-1-01-0003			

Figure 2-28. Control Logic (1 of 2)









# MAINTENANCE

## SECTION III

### General

Become familiar with the various functions and data flow through the Datapoint 3300 by referring to Section II of this manual and the Operators Manual provided with the equipment. To gain access to the equipment for maintenance, it is necessary to remove the housing from the base plate and if any of the printed circuit cards require replacement, it will be necessary to remove the keyboard from the terminal base plate.

### WARNING

With the housing removed and power on, 15,000 volts is present at the CRT.

### REMOVAL

#### Housing Removal From Base

The terminal housing is secured to the base plate by 3 Allen head screws. One is located on each side of the base plate, 3-1/2 inches from the rear and the third is located in the front center of the base plate. A 5/32 inch Allen wrench is required to remove these screws. After removing the screws, lift the housing (not including the back panel) straight up until it is clear of the unit and the back panel. This will provide access to the keyboard and the printed circuit cards without removing the back panel.

If it is necessary to remove the back panel, proceed as follows:

1. Remove the two Phillips head screws securing the Data Set connector and unplug the connector.
2. Remove the two Phillips head screws securing the Recorder Model 3300T connector and unplug the connector.

3. Disconnect the AC Power cord from the 115 VAC 60 Hz connector.
4. Remove the fuse holder cap and fuse.

### NOTE

Turn Baud Rate Switch knob to a point where the index mark points straight down. This places the switch in the null position for ease in re-indexing and also makes the knob set screw easily accessible.

5. Using a 1/16 inch Allen wrench, loosen the set screw in the knob on the Baud Rate Switch and remove the knob.

Tilt the back panel toward the rear and lift the panel off the base plate.

### NOTE

Before operating with the cover removed, the fuse and cap, Baud Rate Switch knob, 3300T connector and AC power cord must be replaced. The null position of the Baud Rate Switch will display a cursor however no data can be displayed.

#### Keyboard Removal From Terminal

The Keyboard must be removed from the terminal in order to remove any of the other printed circuit cards. The Keyboard is held in place by four Phillips screws located on the bottom of the terminal base plate, two on each end of the Keyboard. The screw holes through the terminal base plate are slotted to facilitate forward and backward adjustment of the keyboard. Once the mounting screws are removed, unplug the main connector on the right hand side of the keyboard, remove the two Phillips screws securing the small power connector to

the keyboard and unplug the connector. The entire keyboard may now be lifted out.

### **Keyboard Removal From Base**

The Keyboard is secured to its mounting plate with 8 hex head screws. The screws are located on the bottom of the keyboard mounting plate and must be removed to free the printed circuit card from the mounting plate.

### **Key Switch Removal From Keyboard**

Remove the Keyboard printed circuit card from the Keyboard mounting plate. Two types of key switches are used, GRI and NAVCOR. The GRI switch is secured to the printed circuit card by one hex nut and two solder connections and the NAVCOR switch is secured to the printed circuit card by a slotted head screw and three solder connections. After removing the screw or nut, hold the Keyboard upside down and heat all solder connections simultaneously until the switch drops free. It will be necessary to clean all of the switch mounting holes in the printed circuit card prior to mounting the new key switch.

### **Printed Circuit Card Removal**

After the keyboard has been removed, the other five printed circuit cards may be removed by pulling the card straight forward out of its connector. The cards when viewed from the front, starting from the top, are:

- Deflection Amplifier Card
- Interface 1 Card
- Interface 2 Card
- MOS Card
- Control Logic Card

### **Logic Power Supply Removal**

The Logic Power Supply is secured to the terminal by five Phillips head screws. If it is necessary to gain access to the Logic Power Supply for trouble-shooting or repair, remove the two Phillips head screws on the bottom of the terminal base plate (on the right hand side about half-way toward the rear of the plate). Remove the two Phillips head screws that secure the Logic Power Supply bracket to the right hand

side of the CRT bracket. Remove the one Phillips head screw that secures the Logic Power Supply bracket to the back bracket. Using caution to avoid breaking or shorting together any of the connecting wires; lift the Logic Power Supply and bracket to clear the terminal base plate and move it out to the right hand side of the terminal.

### **NOTE**

If power is to be turned on for trouble-shooting, check first to ensure that no wires were broken or shorted together in moving the power supply out.

### **High Voltage Power Supply Removal**



Before attempting to remove the High Voltage Power Supply, ensure that the post accelerator has been discharged by shorting the post accelerator connection to ground. The post accelerator connector is located under the rubber cap on the right rear of the CRT. Use extreme caution in grounding this connection since a 15,000 volt potential may be present.

After the post accelerator has been discharged, disconnect the spring clip connector (under the rubber cap) from the side of the CRT. Disconnect the two input leads on the side of the High Voltage Power Supply. Loosen the screw on top of the power supply enough to permit removal of the spade lug on the CRT ground wire.

Support the power supply while removing the four Phillips head screws that secure the High Voltage Power Supply to the rear panel. Lift the power supply out of the terminal.

### **CRT Removal**

Disconnect the octal plug on the rear panel near the left side. Disconnect the socket on the rear of the CRT.

**CAUTION**

Discharge the post accelerator and disconnect the high voltage lead to the post accelerator connection. Remove the ground spring across the back of the CRT. Support the CRT and deflection yoke while removing the four Phillips head screws that secure the CRT faceplate to the CRT brackets. Lift out the CRT and deflection yoke.

Figures 3-1 through 3-4 show views of the Data-point 3300 with the housing removed.

Figure 3-5 shows the Logic and Deflection Power Supply cards moved out to the side to provide access to the cards for trouble shooting.

Assembly drawings are provided to facilitate locating components during trouble shooting.



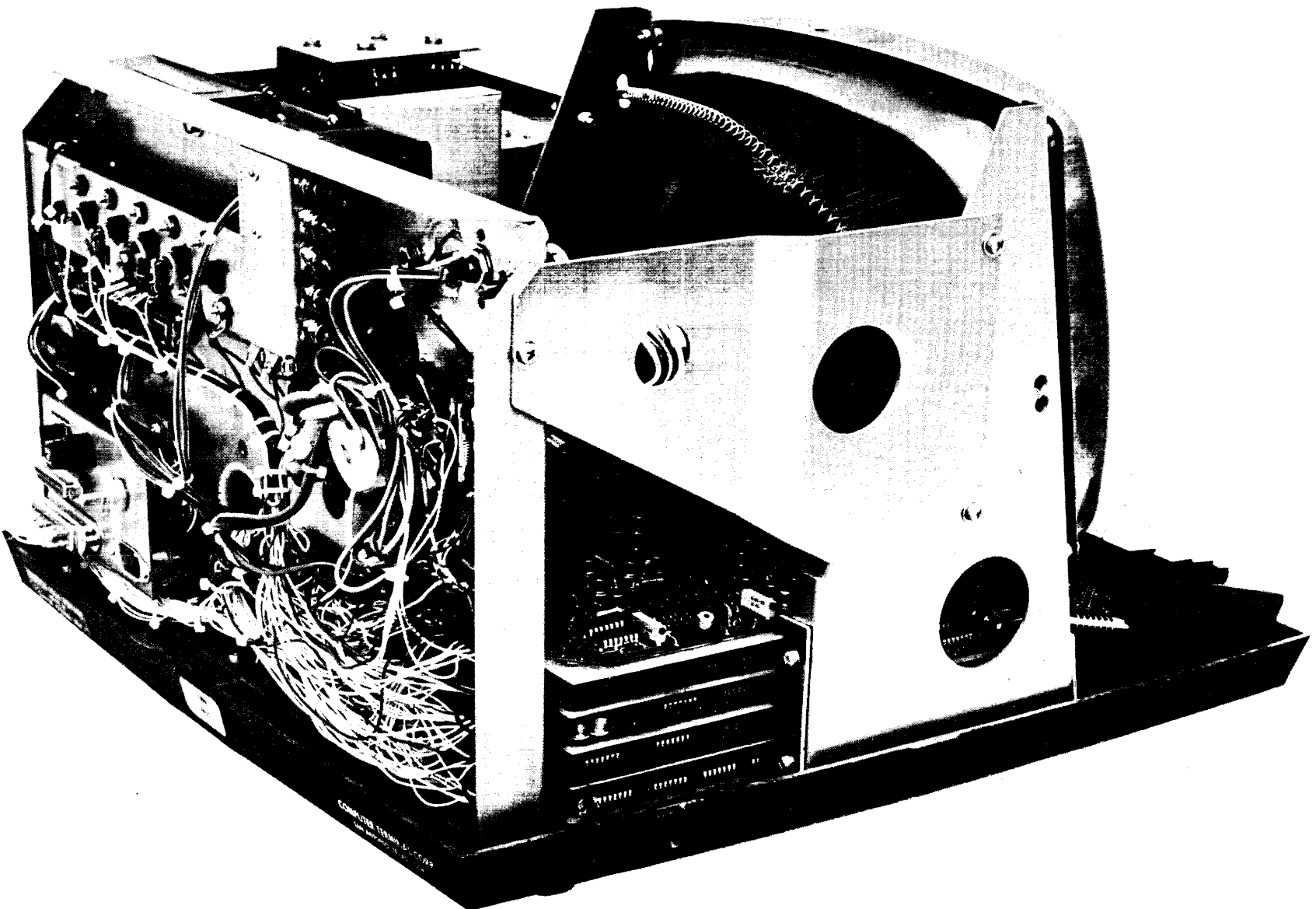


Figure 3-1. Datapoint 3300 with Cover Removed

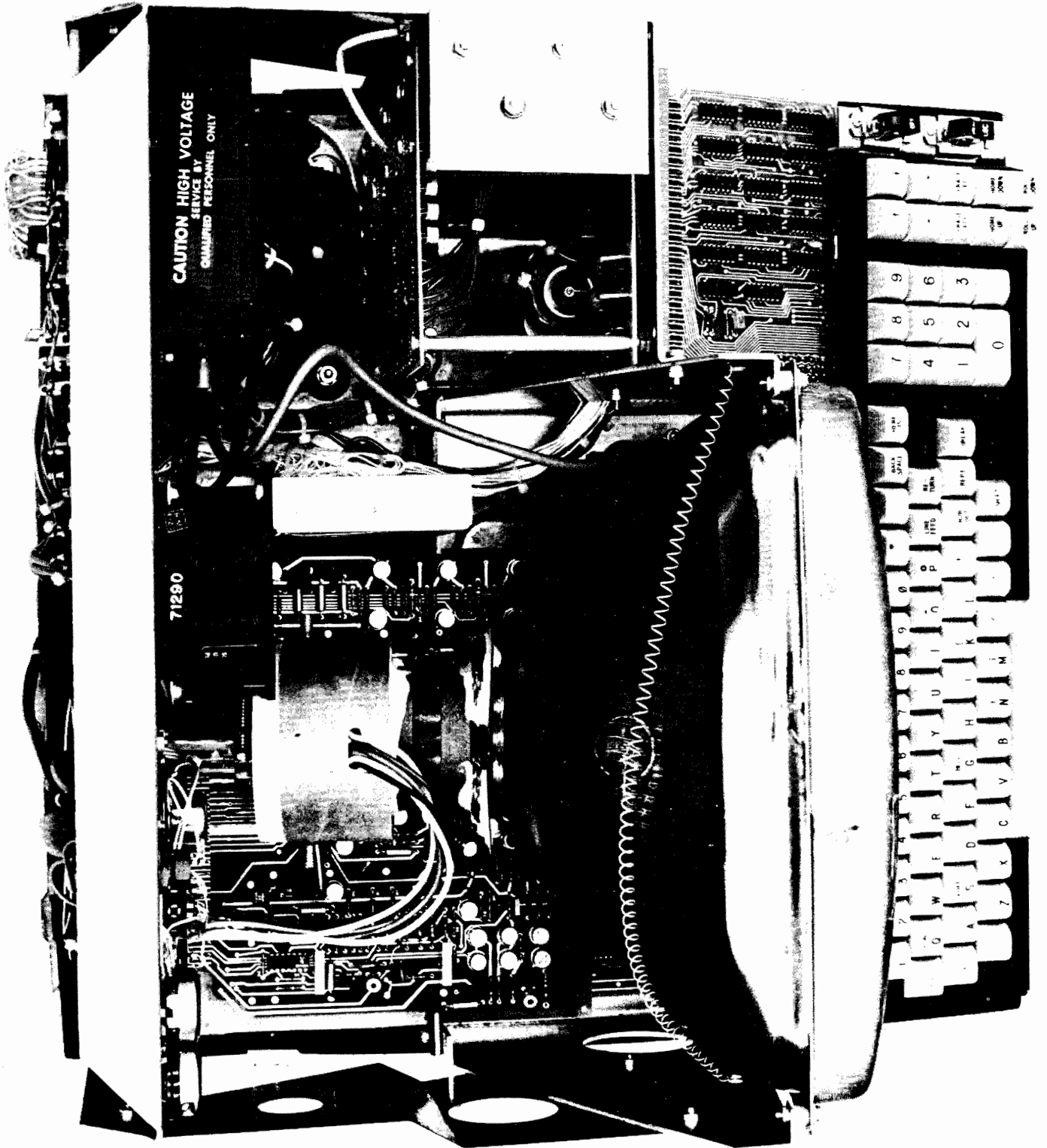


Figure 3-2. Datapoint 3300, Top View

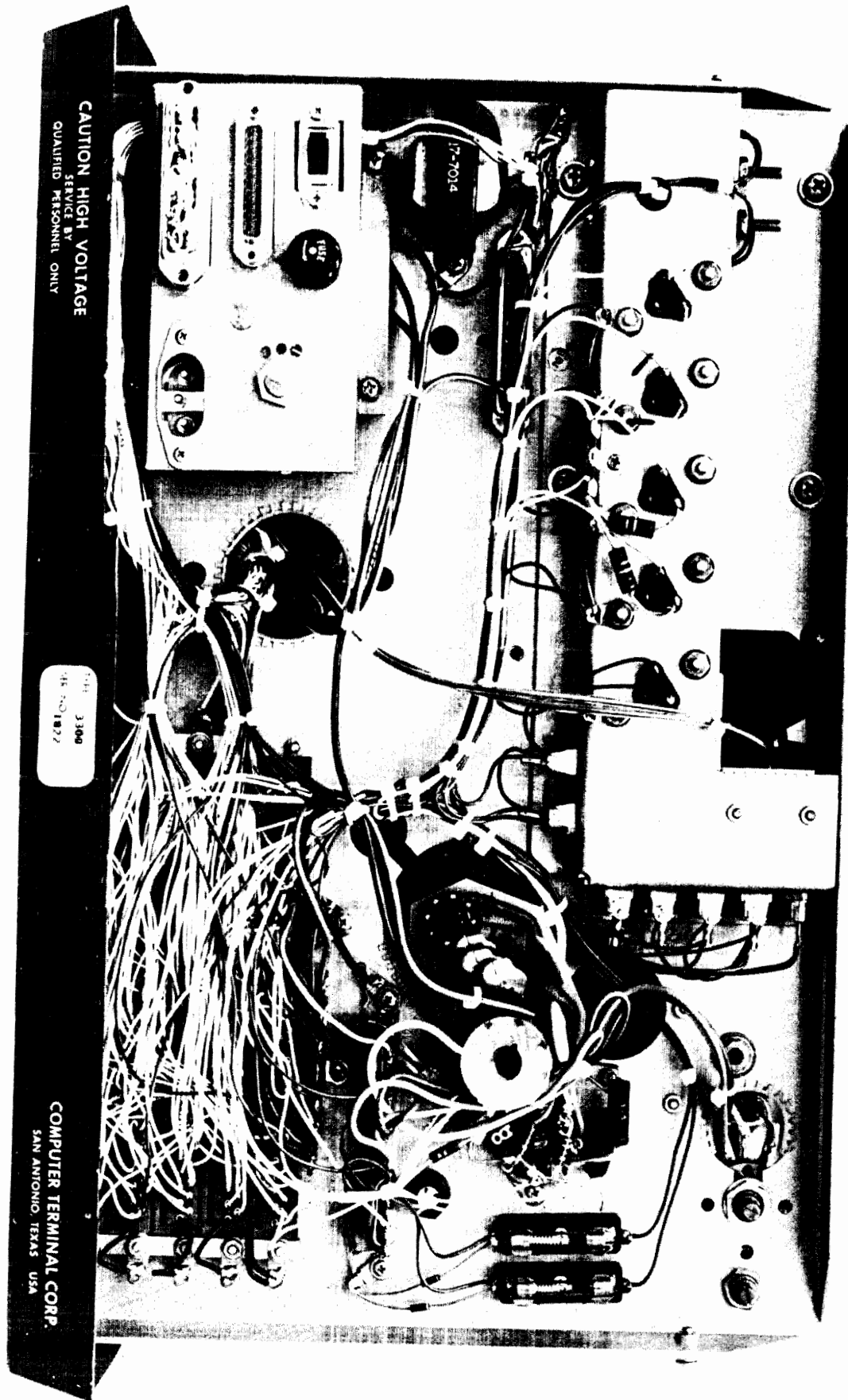


Figure 3-3. Datapoint 3300; Rear View

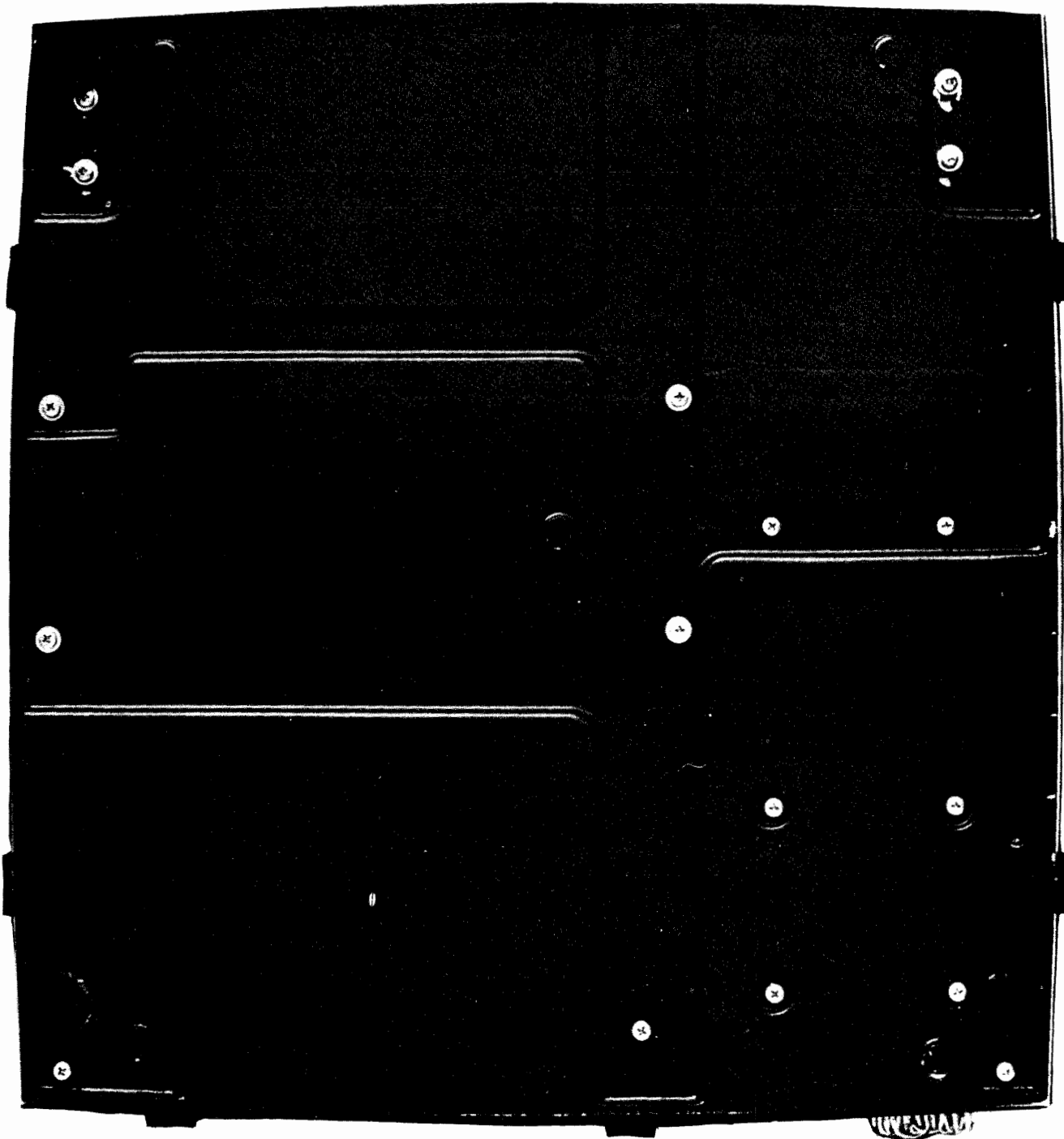


Figure 3-4. Datapoint 3300, Bottom Panel

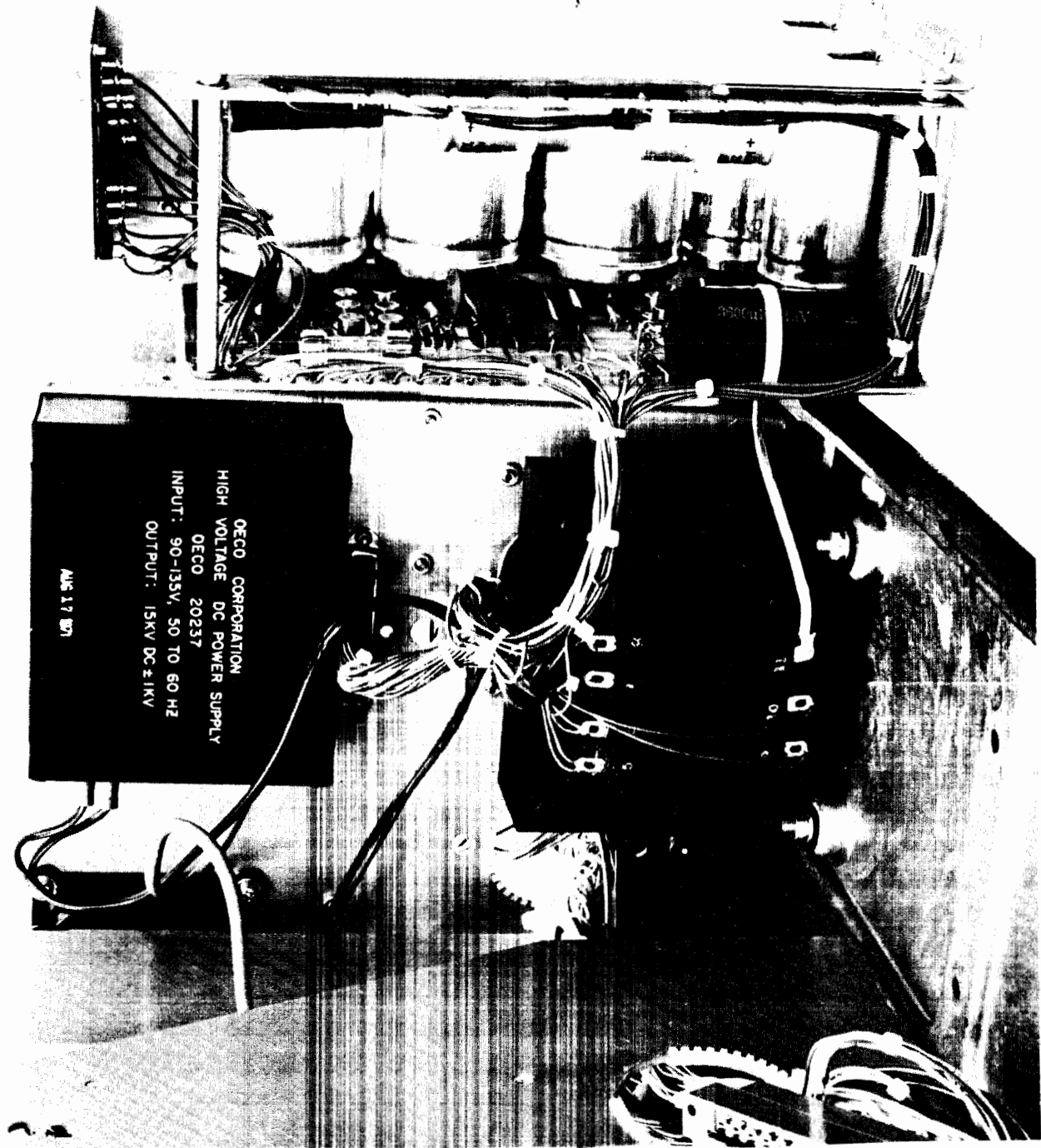


Figure 3-5 . Logic and Deflection Power Supplies

**INTENTIONALLY LEFT BLANK**

**"DRAWING DELETED"**

**Figure 3-6. Keyboard Assembly (NAUCOR)**

23	23	000-024-41	CONTACT, UPPER TIER	60-7001-05-13	ELCO		31
24	24	000-025-41	CONTACT, LOWER TIER	60-7001-15-13	ELCO		30
1	1	000-021-71	INTEGRATED CIRCUIT	SN74121N	T.I.		29
1	1	000-011-71	INTEGRATED CIRCUIT	SN7420N	T.I.		28
5	5	000-006-71		SN7474N			27
1	1	000-007-71		SN7473N			26
1	1	000-009-71		SN7440N			25
1	1	000-010-71		SN7430N			24
1	1	000-014-71		SN7401N			23
7	7	000-015-71	INTEGRATED CIRCUIT	SN7400N	T.I.		22
							21
279	279	000-008-70	DIODE	1N914	T.I.		20
1	1		CAPACITOR, TANTALUM - 10 $\mu$ F, 20 VOLT	T110B106M020AS	KERMET		19
1	1		CAPACITOR, CERAMIC - 470 $\mu$ F, 600 V	DD 471 G	CENTRAL LAB		18
1	1		TANTALUM - 6.8 $\mu$ F, 35 V	T110B685M035AS	KERMET		17
48	56		CERAMIC - .1 $\mu$ F, 10 V	UK10-104	CENTRAL LAB		16
2	2		CAPACITOR, CERAMIC - .01 $\mu$ F, 50 V	UK 50-103	CENTRAL LAB		15
1	1	000-004-65	RESISTOR, CARBON COMP - 27K $\frac{1}{4}$ W, 5%	RC07GF273J	AB		14
8	8	000-001-65	RESISTOR, CARBON COMP - 10KOHM, $\frac{1}{4}$ W, 5%	RC07GF103J	AB		13
56	56	000-021-65		RC07GF472J			12
							11
69	69	000-030-65	RESISTOR, CARBON COMP - 1KOHM, $\frac{1}{4}$ W, 5%	RC07GF102J	AB		10
75	75		REED ASSEMBLY				9
							8
							7
1	1	000-045-59	PRINTED-WIRING BOARD	01-1-02-0017-1	ENGINEERING		6
							5
							4
							3
		000-035-10	BOARD ASSEMBLY, KEYBOARD	01-1-03-0017-2	ENGINEERING		2
		000-035-10	BOARD ASSEMBLY, KEYBOARD	01-1-03-0017-1	ENGINEERING		1
-2	-1	CTC		VENDOR	REF	ITEM	
QTY		PART NO	NOMENCLATURE	PART NO	DESC		

**CODED KEY OPTIONS**  
STANDARD KEYBOARD CODING SHOWN

**BACKSPACE**

BIT	REMOVALS	
	STANDARD	OPTIONAL
1	CR 185	CR 185
2	CR 186	CR 186
3	CR 187	CR 187
4	CR 188	CR 188
5	CR 189	CR 189
6	CR 227	CR 237
7	CR 190	CR 190

**CURSOR KEYS**

STANDARD		CURSOR KEYS							
BIT	CODE	HD	HU	ERASE EOL	ERASE EOF	↑	↓	←	→
1	1	CR 223	CR 230	CR 237	CR 244	CR 251	CR 258	CR 265	CR 272
2	1	CR 224	CR 231	CR 238	CR 245	CR 252	CR 259	CR 266	CR 273
3	1	CR 225	CR 232	CR 239	CR 246	CR 253	CR 260	CR 267	CR 274
4	1	CR 226	CR 233	CR 240	CR 247	CR 254	CR 261	CR 268	CR 275
5	1	CR 227	CR 234	CR 241	CR 248	CR 255	CR 262	CR 269	CR 276
6	1	CR 228	CR 235	CR 242	CR 249	CR 256	CR 263	CR 270	CR 277
7	1	CR 229	CR 236	CR 243	CR 250	CR 257	CR 264	CR 271	CR 278

**ESCAPE**

BIT	REMOVALS	
	STANDARD	OPTIONAL
1	CR 49	CR 49
2	CR 50	CR 50
3	CR 51	CR 51
4	CR 52	CR 52
5	CR 53	CR 53
6	CR 54	CR 54
7	CR 55	CR 55

REF DESIGNATOR	ITEM
R1 THRU R49, R105, R108 THRU R124, R134, R135	10
R57 THRU R104, R126 THRU R133	12
R50 THRU R56, R107	13
R106	14
C50 C61	15
C1 THRU C48, C52 THRU C59	16
C60	17
C51	18
C49	19
CR1 THRU CR221, CR223 THRU CR278, CR287, CR288	20
Z1, 2, 4, 6, 8, 10, 7	22
Z15	23
Z13	24
Z14	25
Z16	26
Z3, 5, 9, 11, 12	27
Z17	28
Z18	29

NOTE: ALL DIODE REMOVALS WILL BE MARKED WITH AN "X". AN "X" IN A PARTICULAR BIT POSITION INDICATES A ZERO.

**CODING**

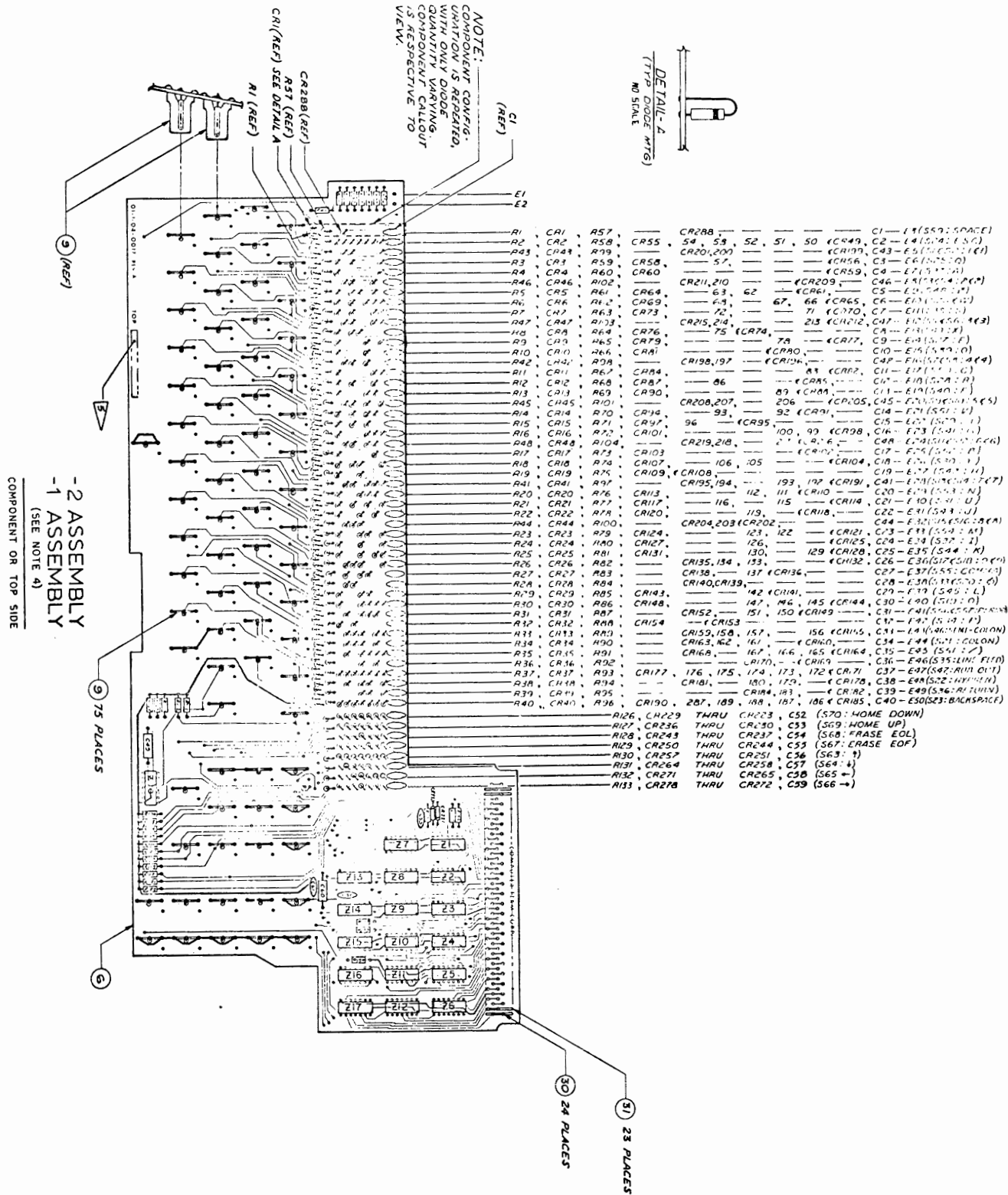
STANDARD: WILL BE SPECIFIED BY MARKETING AND WILL BE CODED PRIOR TO INSTALLATION INTO DATAPOINT 3300

OPTIONAL: WILL BE SUPPLIED BY MARKETING AND WILL BE CODED PRIOR TO INSTALLATION INTO DATAPOINT 3300.

5. AFTER ASSEMBLY IS COMPLETE, STAMP ASSEMBLY PART NO., REVISION LEVEL, AND SERIAL NO. ON TOP SIDE. CHARACTERS ARE TO BE .12 INCH HIGH, GOTHIC STYLE, COLOR BLACK. THE ASSEMBLY NO. SHALL BE PREFIXED WITH "ASSY".
4. TO BUILD A -2 CONFIGURATION, DELETE C52 THRU C59 AND MASK AREA USED BY C52 THRU C59 PRIOR TO WAVE SOLDERING.
3. FOR SCHEMATIC DIAGRAM, REFER TO DRAWING 01-1-01-0006.
2. REFERENCE DESIGNATIONS SHOWN MAY OR MAY NOT APPEAR ON ASSY.
1. EQUIVALENT VENDORS' PARTS MAY BE UTILIZED WITH COMPUTER TERMINAL CORR. ENGINEERING APPROVAL.

NOTES (UNLESS OTHERWISE SPECIFIED)

Figure 3-7. Keyboard Assembly (2 of 2)

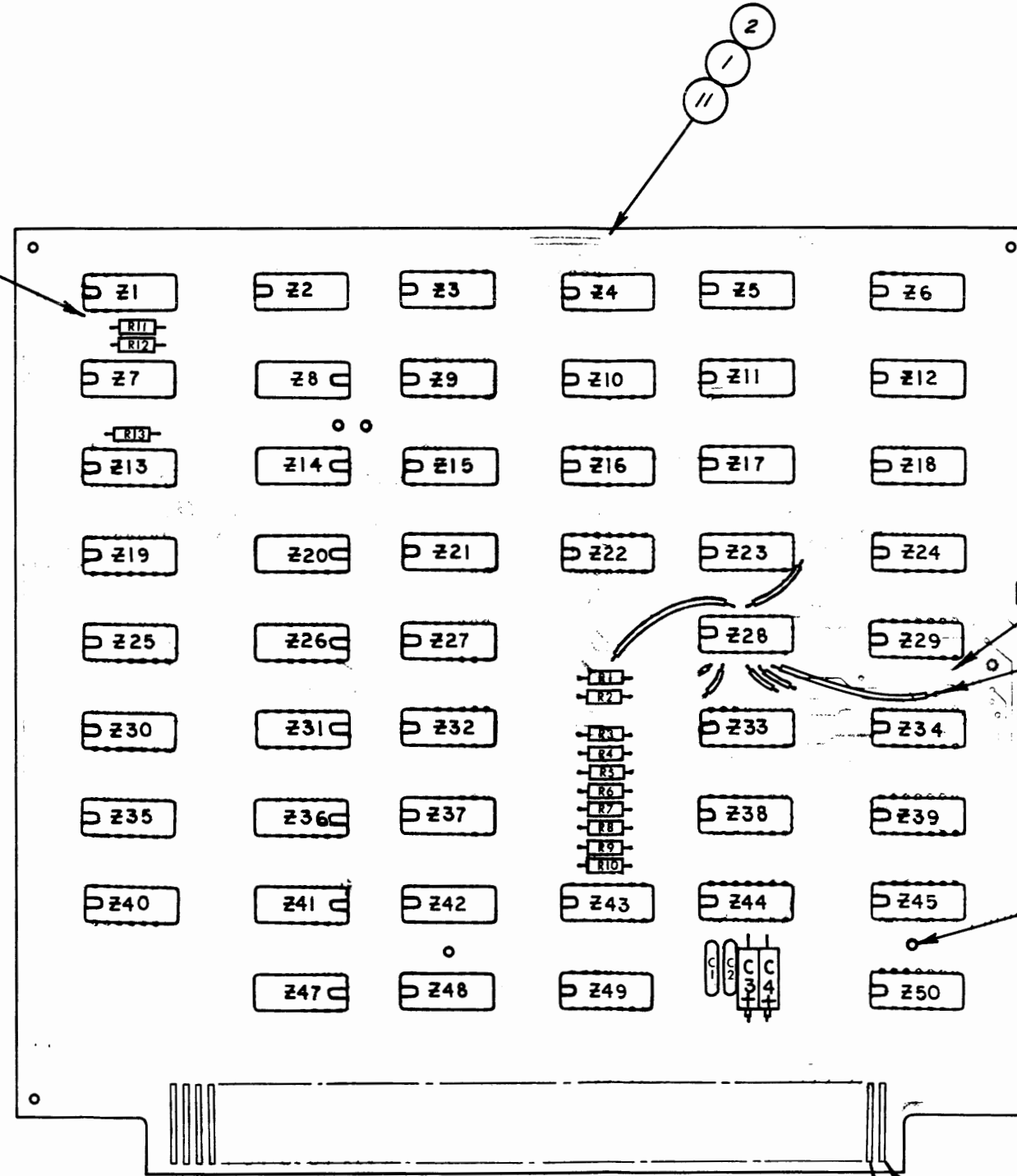








TYPICAL INDICATOR FOR LOCATING PIN NO. 1



INSTALL SOLDER SOCKETS IN HOLES IDENTIFIED WITH A, B, C, D, E, H, J, K, L, M, N, O, P, R, S, AND NUMBERS 1 THRU 8 TOTAL PLACES 23

INSTALL PER TABLES LOCATED ON SHEET 2 LENGTH A/R

TYPICAL TPI THRU TP4 4 REQ'D (REF)

-1 ASSEMBLY COMPONENT OR TOP SIDE

3. AFTER ASSEMBLY IS COMPLETE, STAMP ASSEMBLY PART NUMBER, REVISION LEVEL, AND SERIAL NUMBER ON BOTTOM SIDE. CHARACTERS ARE TO BE 1/16 INCH HIGH, GOTHIC STYLE, COLOR WHITE. THE ASSEMBLY NUMBER SHALL BE PREFIXED WITH "ASSY".
  2. FOR SCHEMATIC DIAGRAM REFER TO DRAWING 01-1-01-0005.
  1. EQUIVALENT VENDORS PARTS MAY BE UTILIZED WITH COMPUTER TERMINAL CORP. ENGINEERING APPROVAL.
- NOTES: (UNLESS OTHERWISE SPECIFIED)

REF DESIGNATOR	ITEM
C1, 2	20
C3, 4	19
R1-10	23
R11-13	24
R14-21	25
Z3, 13, 20, 25, 30, 35, 44, 45	27
Z7, 19, 43, 47	28
Z40	29
Z39	30
Z4-6, 10-12, 16-18, 22-24, 28	31
Z9, 33, 34, 38	
Z1, 2, 9, 14	32
Z26, 31, 34, 41, 47	33
Z15, 21, 27, 32, 37, 42, 48, 50, 8	34

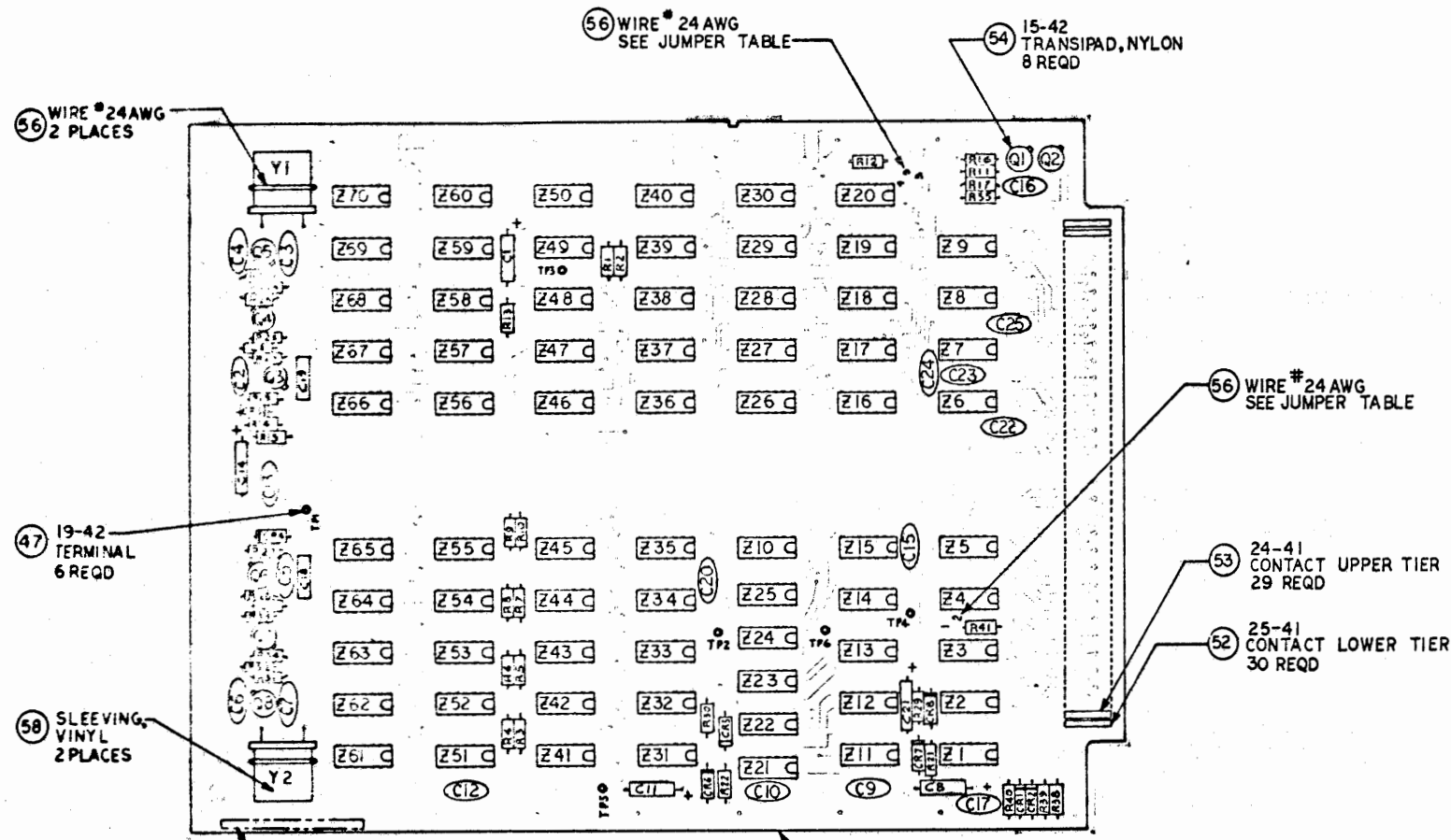
12 30 PLACES (REF)  
13 29 PLACES (REF)

Figure 3-9. Interface 1 Assembly (1 of 2)



REVISION TABLE				
ENG NO.	MFG NO.	ASSY REV.	A/W REV.	ENG APPV.
- 801	58-10	M	J	
- 804	45-10	M	J	
- 805	561-10	-	J	
- 806	562-10	-	J	

A/W REV	CONF	REV	DESCRIPTION	DATE	APPROVED
	SH1	E	REDRAWN, REVISED SH1, ADD C-D SHEETS 2 THRU 5 ADD JUMPERS 24-25, 26-27 TO TABLE OF 3	1-7-70	
	SH4	F	INCORP DCN NO. 1044	4-16-70	DDM PH
		H	INC DCN #1392	6-16-70	JOS
		J	INC EO 1850 & 2068	7-28-71	W.L.
		H	INC EO 2856	10-1-71	J.T.H.
		H	INC EO 3175 & REDRAWN -2 & -3 INACTIVATED FOR FUTURE DESIGN	12-8-71	L.M.F.
		J	INC EO 3239, 5055, 4230; REDRAWN & ADD-805 & -806	10-18-73	P.H.



JUMPER TABLE		
	FROM	TO
-801 ASSY	1	2
	3	4
-804 ASSY	3	4
-805 ASSY	1	2
	4	5
-806 ASSY	4	5

- 801 (P/N 58-10) I16 OPTION ONLY
- 804 (P/N 45-10) NO OPTIONS (STANDARD)
- 805 (P/N 561-10) I16 & I07 OPTIONS
- 806 (P/N 562-10) I07 OPTION ONLY

FOR PARTS LIST SEE PL 01-1-03-0008

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NOTES: (UNLESS OTHERWISE SPECIFIED)

Figure 3-10. PWA, Interface Logic 2

QTY	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM
3300	01-09-0001	PRINTED WIRING ASSY, INTERFACE LOGIC NO. 2		Computer Terminal Corporation		
3300	01-09-0001					
3300	01-09-0001					
3300	01-09-0001					

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH.	DRAWN: <i>g.l.u.</i>	DATE: 10-17-73
TOLERANCES: FRACTIONS ±, ANGLES ±, DECIMALS, DASH	CHECKED: <i>R. Malmon</i>	DATE: 10-18-73
	DESIGN ENGINEER	
	PROJECT ENGINEER: <i>J. Meyer</i>	DATE: 10-18-73
	<i>E. Malmon</i>	DATE: 10-19-73

SIZE: D	DWG NO: 01-1-03-0008	REV: M
SCALE: 1/1	P/N: 01-1-03-0008	SHEET: 1 OF 1





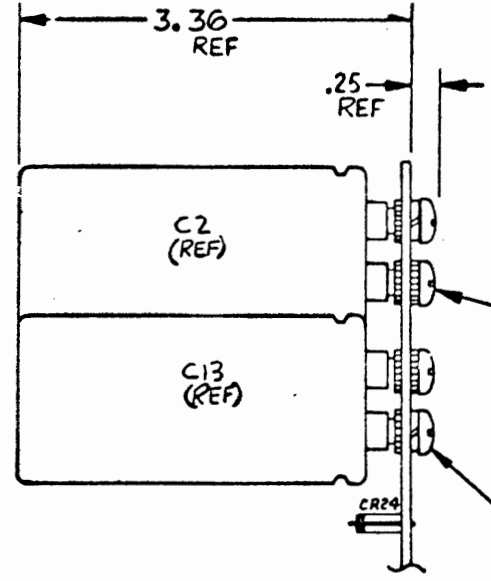
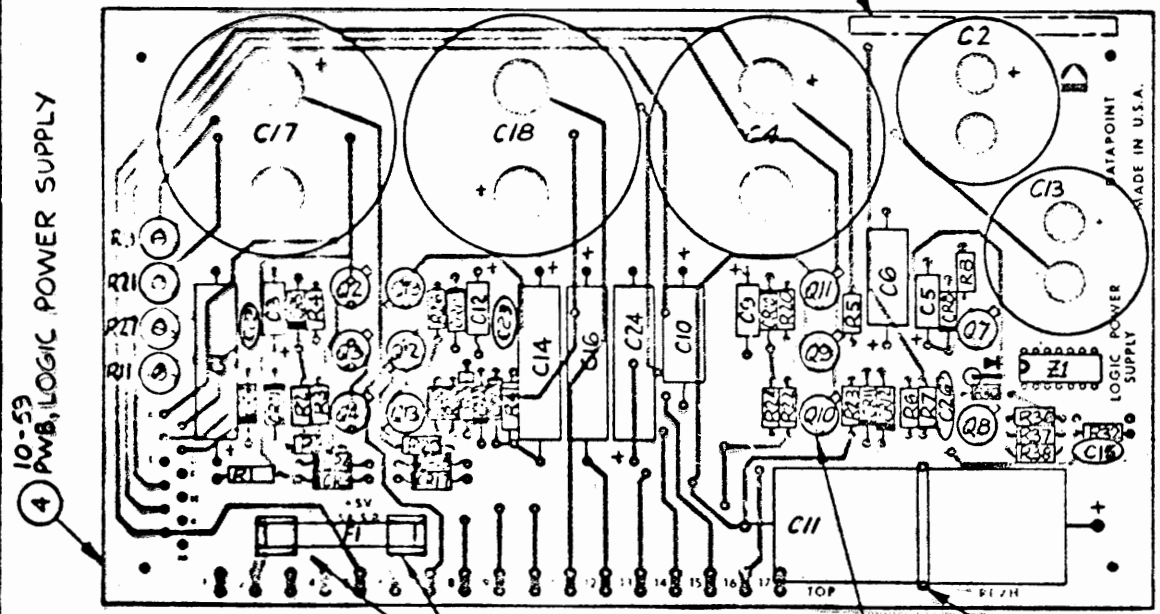






748 REV	A/W REV	ZONE	LET	DESCRIPTION	DATE	APPROVED
-801	REV					
82-10	CTR					
L		L		REPLACES REV K, WITH CHANGE. SEE DCN 1729, DCN 1601 & DCN 1734 D. SLAYTON	11-1-70	D. M. ELL GEN. M.
M		M		INC. E.O. 2072 AND 2073 G. SMITH 2/21/71	4/19/71	L.M.F B. ELL
N		N		INC. E.O. 2609 & 2053 J.T. HECTOR 7/10/71	8/4/71	
P	G	P		INC. E.O. 2970 J.T. HECTOR 9-30-71	10-4-71	K.P. JACKSON
Q	C	Q		E.O. 3233 MFG ONLY (1/1) 5/1/72	5/14/72	
R	G	R		INC. E.O. 3617 0/1/1/73	5/14/73	
S	G	S		INC. E.O. 3831 0/1/1/73	5/14/73	
T	G	T		INC. E.O. 3988 0/1/1/73	5/14/73	
U	H	U		INC. E.O. 5100 JIM L LOCK 11-7-73	11/8/73	
V	H	V		INC. E.O. 5119 JIM L LOCK 11-7-73	11/8/73	
V	H	W		MC 80 5477, JMP 11-22-74	11/22/74	

MARK ASSY 01-1-03-0001-801 REV V  
.12 HIGH CHARACTER, COLOR BLACK,  
LOCATE APPROX. AS SHOWN



- 61 51-1071-09 SCREW, PAN HD, 10-32 x 1/2 - 2 REQD
  - 62 51-1601-44 WASHER, LOCK, EXT. TOOTH #10-3 REQD
  - 63 51-1601-42 WASHER, SPLIT-LOCK #10-1 REQD
- 4 PLCS C2, C4, C13 & C17

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FOR PARTS LIST SEE PL 01-1-03-0001  
SCH: 01-1-01-0001  
PWB: 01-1-02-0001

- 52 203-42 FUSE CLIP 2 REQD
  - 53 2-47 FUSE
  - 58 15-42 TRANSIPAD
  - 56 111-42 TIE WRAP
- 801

QTY	CTC PART NO	NOMENCLATURE	VENDOR PART NO	VENDOR	REF DES	ITEM

QTY	CTC PART NO	NOMENCLATURE	VENDOR PART NO	VENDOR	REF DES	ITEM

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND UNLESS APPLICABLE FINISH	DRAWN <i>A. Meria</i> DATE 5/3/73	<p>9725 DATAPoint DR SAN ANTONIO TEXAS 78228 512 696 4520</p>
TOLERANCES FRACTIONS: 1/16 1/32 1/64 DECIMALS: .1 .05 .01 ANGLES: 30 45 60 90 120 150 180 HOLE DIA: .0015 .0025 .005 .01 .015 .02 .03 .04 .05 .06 .07 .08 .09 .1 .12 .15 .18 .2 .25 .3 .375 .4 .5 .6 .75 .8 .9 1.0 1.125 1.25 1.5 1.75 2.0 2.25 2.5 2.75 3.0 3.25 3.5 3.75 4.0 4.5 5.0 5.5 6.0 6.5 7.0 7.5 8.0 9.0 10.0 11.0 12.0 14.0 16.0 18.0 20.0 22.0 24.0 26.0 28.0 30.0 32.0 34.0 36.0 38.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 90.0 100.0	DATE 5/14/73 DATE 5/16/72	
MATERIAL	PROJECT ENGINEER <i>John King</i> DATE 5/16/72	<p>PRINTED WIRING ASSY, LOGIC POWER SUPPLY</p>
		<p>SIZE: C DWG NO: 01-1-03-0001 REV: W</p>
		<p>SCALE: 1/1 P/N: 52-10 SHEET: 3-31/(3-32 blank)</p>

NOTES: (UNLESS OTHERWISE SPECIFIED)

Figure 3-14. PWA, Logic Power Supply



4

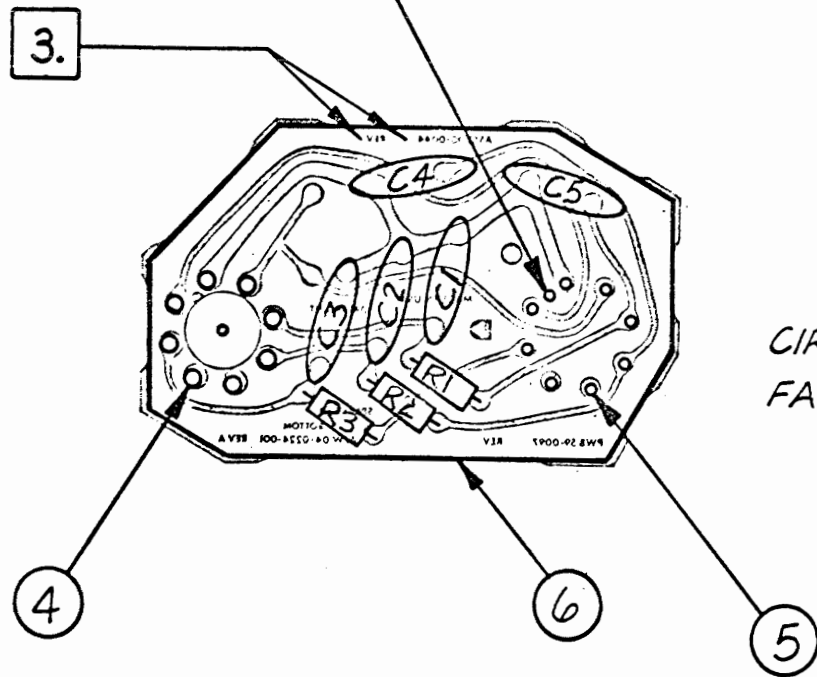
3

2

1

REVISIONS				
ZONE	LET	DESCRIPTION	DATE	APPROVED
	A	Product Structure Plan. Previous Dwg. No. 01-1-03-0026. B. Johnson 5-28-76 INCORP EO # 7079 & 6365	6-10-76	J. Wright

INSTALL KEY WAY PIN NEARSIDE



CIRCUITRY FAR SIDE

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FOR PARTS LIST SEE PL10-0044

(INSTALL 8 SOCKETS FAR SIDE)

(INSTALL 8 CONN PINS FAR SIDE)

-001 (SHOWN)

QTY	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM
-----	--------------	--------------	-----------------	--------	---------	------

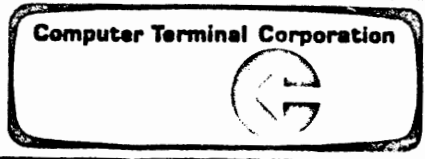
PARTS LIST

3 MARK APPLICABLE DASH NUMBER AND REVISION LETTER, LOCATE APPROXIMATELY AS SHOWN.

2. MAX LEAD LENGTH BELOW BOARD TO BE .09

1. MAX COMPONENT HEIGHT ABOVE BOARD TO BE 1.00

NOTES (UNLESS OTHERWISE SPECIFIED)

USED ON	UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH.		DRAWN <i>A. Morin</i>	DATE 8/14/72	 9725 DATAPoint DR. SAN ANTONIO, TEXAS 78229 512-696-4520
	TOLERANCES FRACTIONS ±      ANGLES ± DECIMALS .X ±      .XX ±      .XXX ±		CHECKED <i>D. Moore</i>	DATE 8-27-72	
SEE P/L	NEXT ASSY	MATERIAL:	DESIGN ENGINEER	DATE	PRINTED WIRING ASSY, SPARKGAP
			PROJECT ENGINEER <i>[Signature]</i>	DATE 8/5/72	
DASH			<i>Joe Esten</i>	8-25-72	SIZE <b>B</b>
			SCALE 1/1		DWG NO. <b>10-0044</b>
					PROJ OI REV <b>A</b>
			SHEET 1 OF 1		















APPLICATION			JAW	REVISIONS				
REV	TR	DESCRIPTION	DATE	APPROVED				
801	FINAL	3300			A	INCORPORATE D.C.N. # 131	9-29-69	
802					B	INCORPORATE DCN # 141	10-5-69	
803					C	INCORPORATE DCN # 177	11-7-69	
804		3300			D	INCORPORATE DCN # 209	11-30-69	
805	FINAL	SWEDISH 3300			E	INCORPORATE DCN # 215	12-1-69	
					F	INCORPORATE DCN # 268 JAS	2-11-71	
					G	INCORP. DCN # 172B & 214, 215	2-11-71	
					H	INC EO 2066, STANDOFF WAS BX1/A, .281 LG. ON EO.	4-4-71	11-2-71
					J	INCORP EO 3406, CREATED SEPARATE PARTS LIST, ALSO ADDED -801 TO ITEMS 11, 14, 15, 18, 19, 21, 23, 24, 27, 44, 68 AND ADDED -1 TO ITEMS 25, 26, 28, 29, 32, 33, 34 & 38 W. LOVAS 11-10-71	11-10-71	PL-2
					K	INCORP EO 3136 W/INCHES R-671 AND EO 3354 & EO 2743	11-10-71	
					L	INC EO 3762, 4263, 3905, 4058 D. O. 6/19/73	6-22-73	

SEE 01-1-09-0001 FOR REV.

REVISION INDEX	SHEET	1	2	3	4	5	6
REV	REV	M	M	M	M	M	M

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH

DRAWN BY: W. LOVAS 11-8-71

CHECKED BY: [Signature] 11-15-71

ENGINEER: [Signature] 11-15-71

PROJECT ENGINEER: [Signature]

TOLERANCES: PLACE 1 PLACE 2 ANGLES 1

MATERIAL:

Computer Terminal Corporation  
8725 DATAPoint DR. SAN ANTONIO, TEXAS 78229 512-536-4320

Computer Terminal Corporation Logo

TITLE: ASSEMBLY - DATAPoint 3300

SIZE: A

DWG NO.: PLOI-1-09-0001

SCALE: -

SHEET: 1 OF 6

REV: M

Computer Terminal Corporation		8725 DATAPoint DR. SAN ANTONIO, TEXAS 78229 512-536-4320		PARTS LIST		DWG TITLE: ASSEMBLY - DATAPoint 3300		DWG NO.: PLOI-1-09-0001		REV M	
QTY PER UNIT	ITEM	PART NO	DESCRIPTION	REF DES	VENDOR P/N	VENDOR	QTY ISSUED	QTY SHRT	STD COST	EXT	SH 2 OF 6
	1		DATAPoint 3300, 115V, 60 HZ			DATAPoint					
	2		DATAPoint 3300, 230V, 50 HZ								
	3		DATAPoint 3300, A-B, 115V, 60 HZ								
	4		DATAPoint 3300, A-B, 230V, 50 HZ								
	5		DATAPoint 3300, SWEDISH, 50 HZ								
	6										
	7	100050	ASSY, REAR PANEL, 115V, 60 HZ		01-1-09-0003-801						
	8	100514	ASSY, REAR PANEL, 230V, 50 HZ		01-1-09-0003-802						
	9	100545	ASSY, REAR PANEL, A-B, 115V, 60 HZ		01-1-09-0003-803						
	10	100546	ASSY, REAR PANEL, A-B, 230V, 50 HZ		01-1-09-0003-804						
	11	100010	ASSY, POWER SUPPLY		01-1-09-0004-801						
	12	100069	ASSY, KEYBOARD & BRACKET		01-1-09-0012-801						
	13	100547	ASSY, KEYBOARD & BRACKET		01-1-09-0012-802						
	14	100042	PWA, ANSWER-BACK		01-1-03-0007-801						
	15	100043	PWA, CONTROL LOGIC		01-1-03-0009						
	16	100005	PWA, MOS CONTROL LOGIC 60 HZ		01-1-03-0004-801						
	17	100469	PWA, MOS CONTROL LOGIC 50 HZ		01-1-03-0004-802						
	18	100045	PWA, INTERFACE LOGIC NO.2		01-1-03-0008-804						
	19	100016	PWA, INTERFACE LOGIC NO.1		01-1-03-0005-801						
	20	100053	PWA, DEFLECTION AMPLIFIER		01-1-03-0003-801						
	21	100038	ASSY, MOLDED HOUSING		01-1-09-0007-801						
	22	560001	ASSY, YOKE		01-1-09-0006-801						
	23	450067	ASSY, POWER CORD		09-1-16-0001-801	DATAPoint					

CHARGE NO. \_\_\_\_\_ QTY \_\_\_\_\_ MATL ISSUED BY \_\_\_\_\_ DATE \_\_\_\_\_ REC'D BY \_\_\_\_\_ DATE \_\_\_\_\_

Figure 3-18A. (1 of 3)

Computer Terminal Corporation		3725 DATAPoint DR. SAN ANTONIO, TEXAS 78229 512-636-4528		PARTS LIST		DWG TITLE ASSEMBLY - DATAPoint 3300		DWG NO. PLOI-1-09-0001 ETC P/N		REV M SH 3 OF 6	
QTY PER UNIT		ITEM	PART NO	DESCRIPTION	REF DES	VENDOR P/N	VENDOR	QTY ISSUED	QTY SHORT	STD COST	EXT
1	1	1	1	1	24	20 0023	ASSY, GUIDE CARD NO. 2				
1	1	1	1	1	25	20 0052	BASE, CASTING				
1	1	1	1	1	26	20 0166	COVER, RIBBED PLASTIC				
1	1	1	1	1	27	20 0021	PANEL, HOUSING, BACK, MOLDED				
1	1	1	1	1	28	20 0013	BRACKET, POWER SUPPLY				
1	1	1	1	1	29	20 0017	BRACE, CHASSIS				
1	1	1	1	1	30	20 0035	BRACKET, CRT MOUNTING, RIGHT				
1	1	1	1	1	31	20 0036	BRACKET, CRT MOUNTING, LEFT				
1	1	1	1	1	32	20 0022	GUIDE, CARD NO. 1				
1	1	1	1	1	33	20 0024	GUIDE, CARD NO. 3				
1	1	1	1	1	34	20 0025	GUIDE, CARD NO. 4				
					35						
1	1	1	1	1	36	20 0149	GASKET, AIRDUCT				
2	2	2	2	2	37	42 0010	SPRING, CRT GROUND				
1	1	1	1	1	38	50 0090	INSULATOR, POWER SUPPLY				
1	1	1	1	1	39	26 0002-05	LABEL, DATAPoint S.A. TEX.				
-	-	1	-	1	40	20 0034	PLATE IDENTIFICATION				
-	-	1	-	1	41	45 0001	CORD, POWER				
-	2	2	-	-	42	42 0018	BAR, SPACER				
1	1	-	1	-	43	20 0576	PLATE, IDENTIFICATION				
1	1	1	1	1	44	83 0001	CATHODE RAY TUBE 12"W/BEZEL				
4	4	4	4	4	45	42 0001	FEET, RUBBER				
-	2	2	-	-	46	50 0043	SCREW, LOCK ASSY (MALE)				

CHARGE NO. \_\_\_\_\_ QTY \_\_\_\_\_ MATL ISSUED BY \_\_\_\_\_ DATE \_\_\_\_\_ REC'D BY \_\_\_\_\_ DATE \_\_\_\_\_

Computer Terminal Corporation		3725 DATAPoint DR. SAN ANTONIO, TEXAS 78229 512-636-4528		PARTS LIST		DWG TITLE ASSEMBLY - DATAPoint 3300		DWG NO. PLOI-1-09-0001 ETC P/N		REV M SH 4 OF 6	
QTY PER UNIT		ITEM	PART NO	DESCRIPTION	REF DES	VENDOR P/N	VENDOR	QTY ISSUED	QTY SHORT	STD COST	EXT
6	5	5	5	5	47	51-2093-04	SCREW, CROSS-RECESSED, OVAL HD, 2-5/8 X 5/8 BLACK OXIDE FINISH				
4	4	4	4	4	48	50 0055	SPACER - #10 X 5/16, .250 LG				
-	2	2	-	-	49	51-4111-09	SCREW, CROSS-RECESSED, PHILLIPS HD 4-40 X 3/4				
7	7	7	7	7	50	51-6051-09	PHILLIPS HD 6-32 X 3/8				
6	6	6	6	6	51	51-6071-09	PHILLIPS HD 6-32 X 1/2				
7	7	7	7	7	52	51-8051-09	PHILLIPS HD 8-32 X 3/8				
5	5	5	5	5	53	51-8071-09	PHILLIPS HD 8-32 X 1/2				
12	12	12	12	12	54	51-8091-09	CROSS-RECESSED, 8-32 X 5/8				
1	1	1	1	1	55	51-7071-03	FH SOCKET CAP 1/4-20X1/2				
2	2	2	2	2	56	51-7091-03	SCREW, FH SOCKET CAP 1/4-20X 5/8				
-	2	2	-	-	57	51-4611-40	WASHER, FLAT NO. 4				
14	14	14	14	14	58	51-6611-40	FLAT NO. 6				
22	22	22	22	22	59	51-8611-40	FLAT NO. 8				
-	22	22	-	-	60	51-4601-42	SPLIT NO. 4				
27	27	27	27	27	61	51-6601-42	SPLIT NO. 6				
14	14	14	14	14	62	51-8601-42	SPLIT NO. 8				
1	1	1	1	1	63	51-6601-44	WASHER, EXT TOOTH NO. 6				
-	2	2	-	-	64	51-4001-30	NUT, HEX NO. 4-40				
5	5	5	5	5	65	51-6001-30	NUT, HEX NO. 6-32				
A/R	A/R	A/R	A/R	A/R	66	30 0004	ADHESIVE				
A/R	A/R	A/R	A/R	A/R	67	42 0027	GROMMET, CATERPILLAR				
1	1	1	1	1	68	10 0024	CONNECTOR ASSY, TAPE PLUG				
1	1	1	1	1	69	26 0002-05	LABEL, IDENTIFICATION: S/N				

CHARGE NO. \_\_\_\_\_ QTY \_\_\_\_\_ MATL ISSUED BY \_\_\_\_\_ DATE \_\_\_\_\_ REC'D BY \_\_\_\_\_ DATE \_\_\_\_\_

Figure 3-18A. (2 of 3)



## DIFFERENCE DATA FOR 50 CYCLE OPERATION

For 50 cycle operation of the Datapoint 3300, no changes are required on the following cards:

- Deflection Amplifier
- Interface I
- Interface II
- Control Logic

On the keyboard, a 47 ohm resistor is installed in series with the ON/OFF light bulb.

On the MOS card, install a 21.4 MHz crystal in place of the 26.6 MHz crystal. In the circuit from connector pin 28 to Schmidt trigger Z40, add two 1.8K ohm resistors, tapped by a 0.01  $\mu\text{f}$  capacitor. Figure 1 shows the resulting circuit.

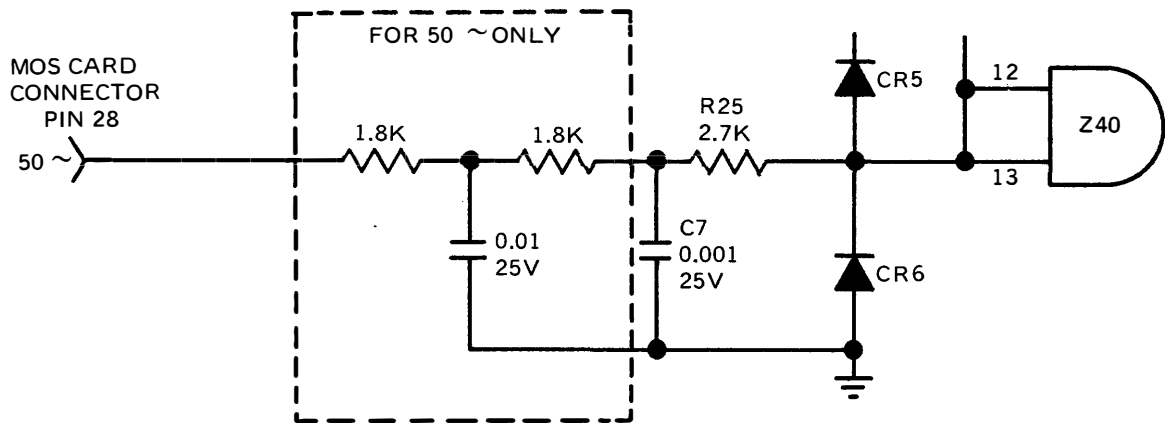


Figure 1

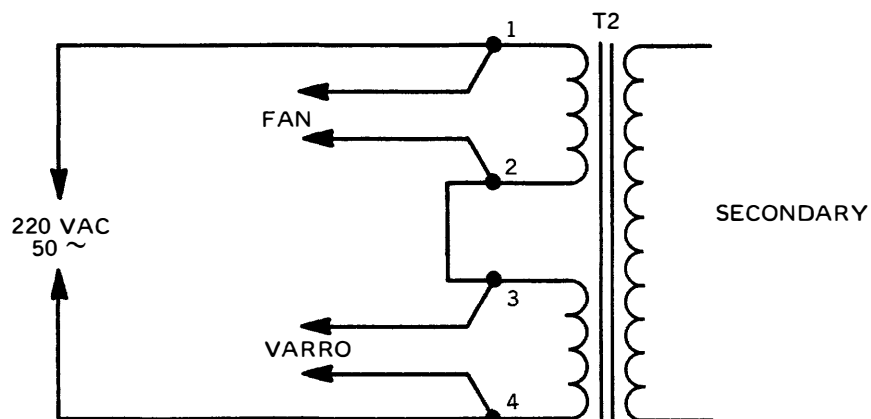


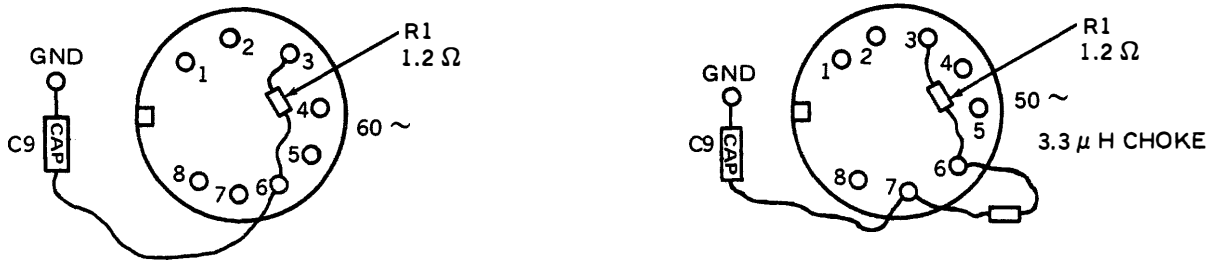
Figure 2

Changes necessary in the power supply are:

- Remove jumpers on transformer T2 from terminals 1 to 3 and 2 to 4.
- Jumper terminals 2 and 3 together.
- Check to ensure fan motor is now connected across terminals 1 and 2 of T2.
- A 15KV Varro high voltage supply designed for 110V 50 cycle input is connected across terminals 3 and 4 of T2. (See figure 2.)

The existing filament transformer T1 must be replaced with a UTRAD Corporation transformer, Part Number 5714 revision A. This transformer has a 220VAC input with 6.3VAC output.

On the base of the octal plug socket located on the rear panel, a 3.3  $\mu\text{h}$  choke must be installed. The choke is a Miller Products Part Number 74F336AP. Figure 3 shows the base of the socket for 50 cycle and 60 cycle operation.



**Figure 3**

This completes the changes necessary for 50 cycle operation of the Datapoint 3300.

**REFERENCE DRAWINGS**

**3300 BACK PANEL (OLD STYLE)**

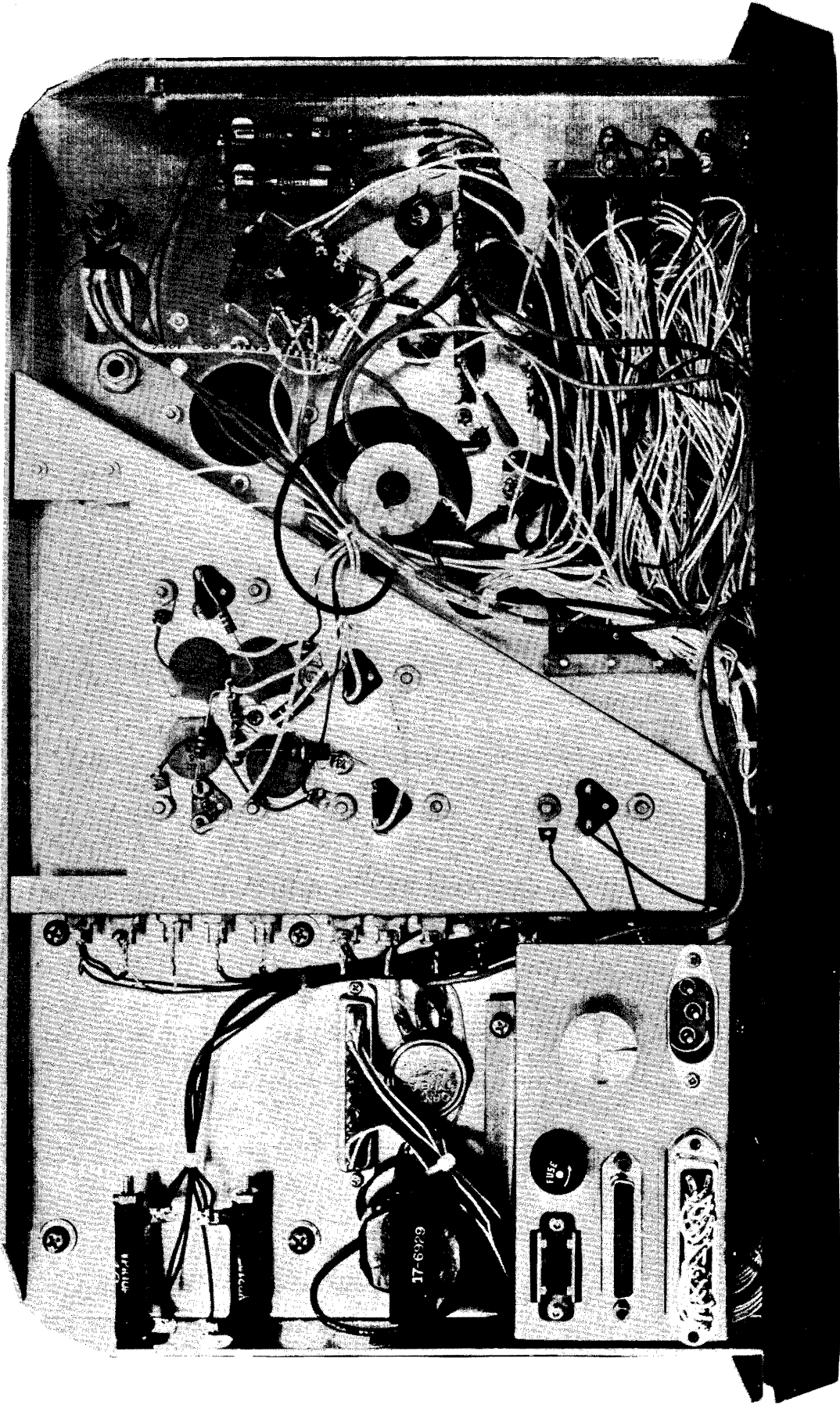


Figure 1. Datapoint 3300, Rear View (Old Style)

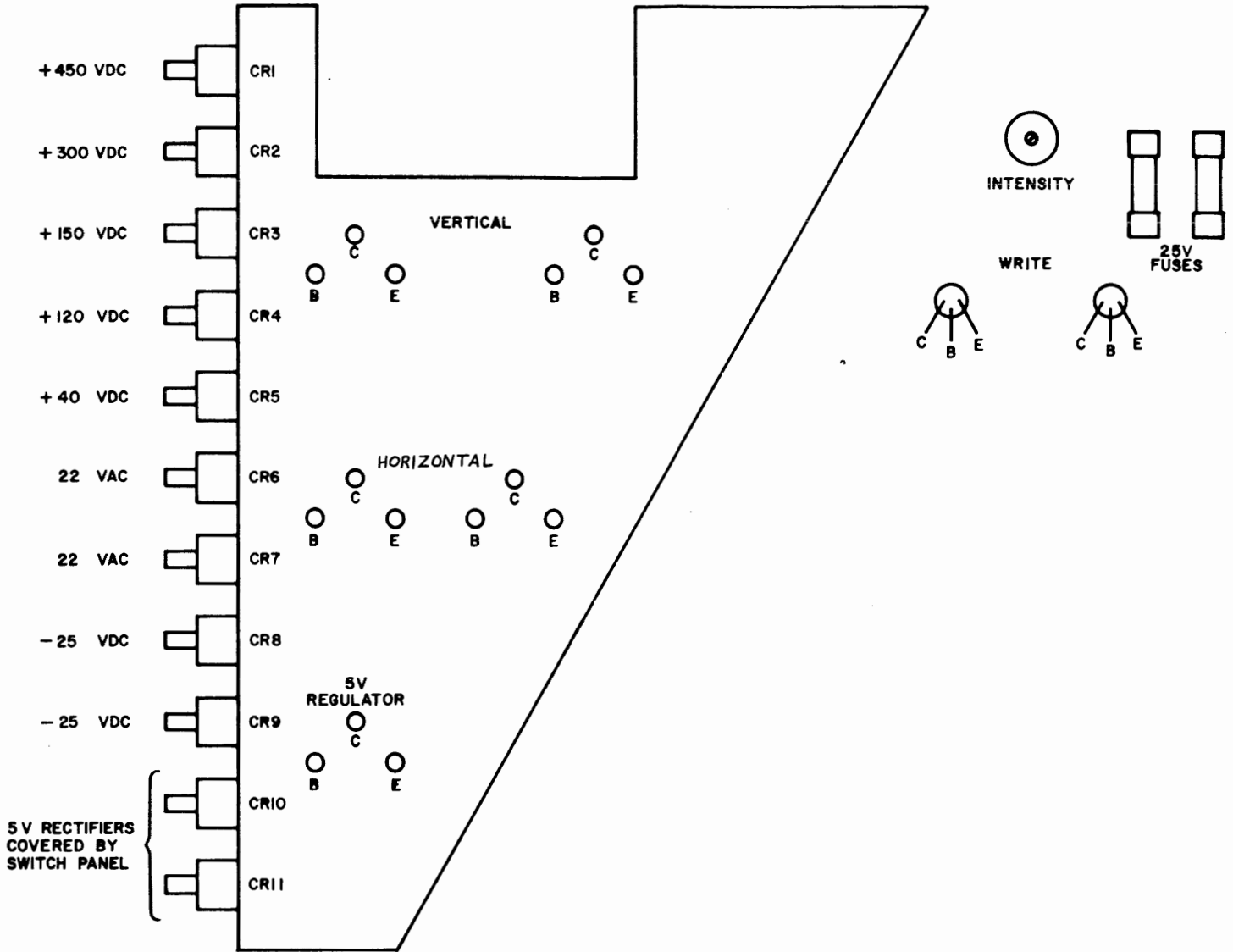


Figure 2. Rear Panel Assembly (1 of 3)



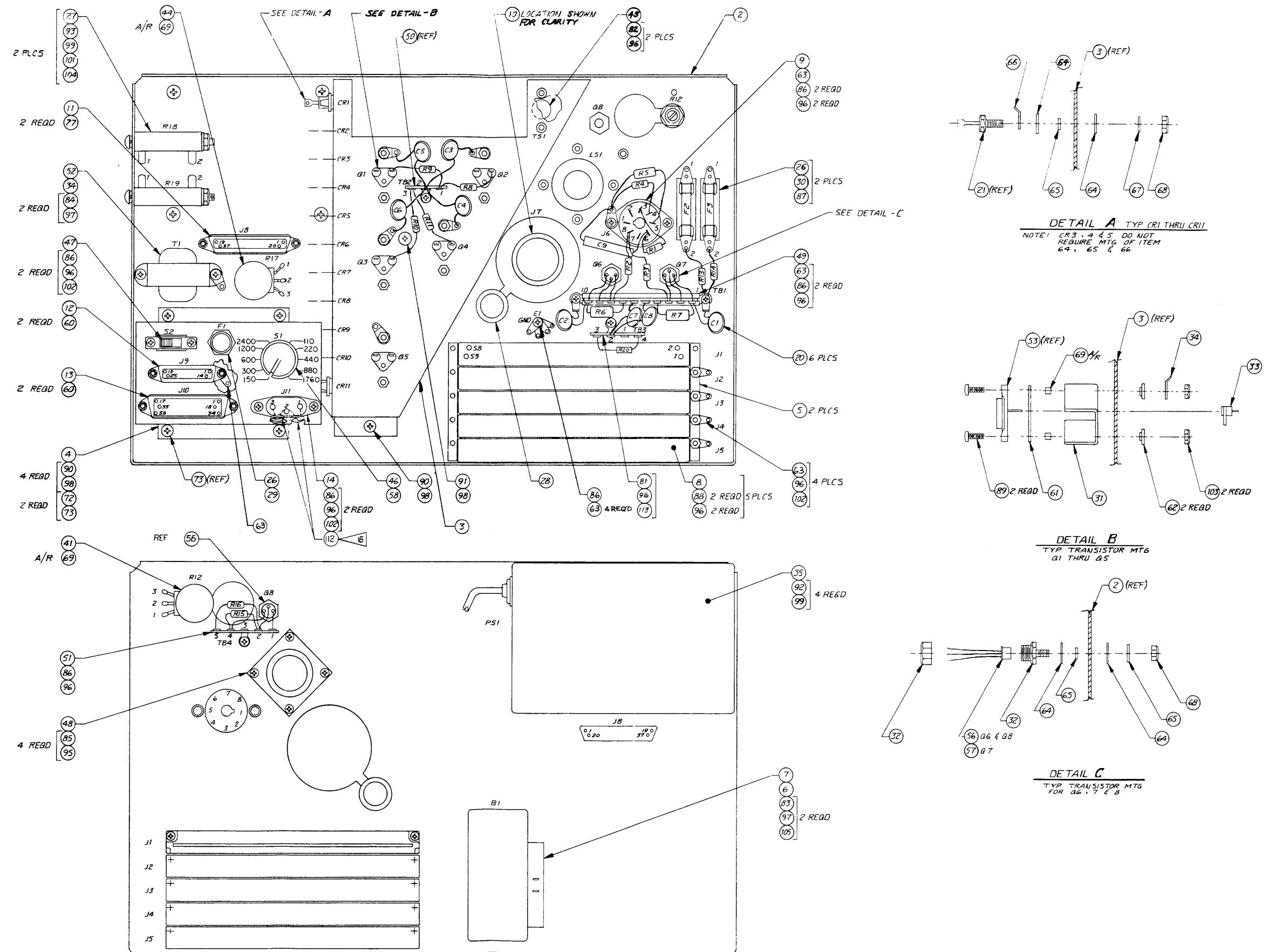


Figure 2. Rear Panel Assembly (2 of 3)

- 16 ADD CAPACITOR C10 AT J11 BETWEEN PINS 1 & 2 FARSIDE. ADD CAPACITOR C11 AT J11 BETWEEN PINS 2 & 3 FARSIDE. CAPACITORS WILL BE .01µF, 600 OR 1000 V, CERAMIC DISC.
  - 15 INSULATE LEADS OF ITEM 114 WITH ITEM 69.
  - 14 ITEMS NOT SHOWN ON FACE OF DWG.
  - 13 ITEM 59 TO BE INSTALLED IN ITEMS 8, 15 & 17, PER WIRE LIST NO. 01-1-05-0001.
  - 12 ITEMS 17 & 18 ARE MATING CONN TO KEYBOARD ASSY & ITEM 77 MOUNTING FOR ITEM 18
  - 11 DIODES CR3, 4 & 5 DO NOT REQUIRE INSULATING HDW.
  - 10 REF DES. SHOWN ON FACE OF DWG MAY NOT APPEAR COMPLETED ASSY.
  - 9 FOR ITEMS NOT BALLOONED ON FACE OF DWG SEE REF DES. IN LIST OF MATERIALS.
  - 8 BEFORE TESTING, ITEM 46 TO BE INDEXED TO POSITION (150), AND SHALL BE INDICATED BY POSITIONING OF POINTER KNOB.
  - 7 INSULATE LEADS 1, 2 & 3 OF R12 & R17.
  - 6 ITEM 46 TO BE MODIFIED TO CENTRALAB STANDARD MINIMUM BEHIND PANEL EXTENSION OF .875 INCH.
  - 5 MTG OF RESISTOR R5 TO BE FREE FROM CONTACT OF ANY ITEM.
  - 4 ITEM 15 & 16 TO BE USED ONLY WITH INSTALLATION OF ANSWER BACK.
  - 3 ON DIODE (CR10) CUT OFF CATHODE APPROX .270 INCH.
  - 2 VENDOR ITEMS GIVEN ARE SUBJECT TO REPLACEMENT BY CTC ENGRS APPROVED EQUIV.
  - 1 ASSEMBLE PER CTC MFG STANDARDS.
- NOTES: (UNLESS OTHERWISE SPECIFIED)

REF	SCHEMATIC, DATAPoint 3300	01-1-01-0011	CTC ENG	124	
REF	WIRE LIST, DATAPoint 3300	01-1-05-0001	CTC ENG	123	
				122	
				121	
				120	
				119	
				118	
				117	
				116	
				115	
1	RESISTOR METAL FILM 992 Ω, 1/4 W, ±1%	RN60C3320F	TI	R21 114	
1	RESISTOR CARBON 470 Ω, 1/4 W	RC07GF47J	ALLEN BRADLEY	R20 113	
2	CAPACITOR CERAMIC .01 500 V			C01C11 112	
1/4 R	WIRE, STRANDED, 18 AWG (VIO)			111	
1/4 R	WIRE, STRANDED, 20 AWG (YEL)			110	
1/4 R	WIRE, STRANDED, 22 AWG (RED)			109	
1/4 R	WIRE, STRANDED, 24 AWG (WHT)			108	
				107	
2	WELL-NUT 6-32	E-632	MOLLY CO	106	
2	NUT, HEX 10-32			105	
10	NUT, HEX 6-32			104	
8	NUT, HEX 4-40			103	
2	WASHER, FIBER NO. 10			102	
6	WASHER, SPLIT-LOCK NO. 10			101	
6	WASHER, SPLIT-LOCK NO. 8			99	
4	WASHER, SPLIT-LOCK NO. 6			98	
27	WASHER, SPLIT-LOCK NO. 4			97	
4	WASHER, SPLIT-LOCK NO. 2			96	
				95	
2	SCREW, CROSS RECESSED 10-32 X 1/4			94	
4	SCREW, CROSS RECESSED 10-32 X 1/4			93	
1	SCREW, PAN HD 8-32 X 1 1/2			92	
5	SCREW, PAN HD 8-32 X 1 1/2			91	
10	SCREW, PAN HD 6-32 X 1 1/2			90	
10	SCREW, PAN HD 4-40 X 3/4			89	
2	SCREW, PAN HD 4-40 X 3/4			88	
12	SCREW, PAN HD 4-40 X 3/4			87	
4	SCREW, PAN HD 2-56 X 1/4			86	
2	SCREW, PAN HD 6-32 X 3/4			85	
2	SCREW, CROSS RECESSED 6-32 X 1/2			84	
2	SCREW, CROSS RECESSED 4-40 X 1/4			83	
2	SCREW, PAN HD 4-40 X 1/4			82	
1	TERMINAL, STRIP (4 PIN)	B50	H.H. SMITH	TB3 81	
1	TRANSISTOR, PNP	2N3789		B4 80	
1	CAPACITOR, 11 µF, 35 V, 10%	6711BL	KEMET	C9 79	
2	CAPACITOR, 05 µF, 600 V, 20% CER	DD-503	CRL	C7,8 78	
2	SCREW LOCK ASSY (MALE)	D 20419-1B	CINCH OR CANNON	77	
1	TRANSISTOR, NPN	2N3713		B3 76	
1	TRANSISTOR, NPN	2N3055		B5 75	
1/4 R	WRAP, CABLE TIE	SST-1M	PANDUIT	74	
2	SPACER, .250 O.D. X .250 LG	a-1-06-005A-1	CTC ENG	73	
2	SPACER, .250 O.D. X .375 LG	01-1-06-005A-2	CTC ENG	72	
1/4 R	TUBING, SHRINK, 1/8 DIA POLYOLEFIN	TYPE FIT221	ALPHA WIRE	71	
1/4 R	TUBING, SHRINK, 1/4 DIA POLYOLEFIN	TYPE FIT221	ALPHA WIRE	70	
1/4 R	TUBING, CLEAR VINYL NO. 10			69	
11	NUT, NUT	NAT3C	RCA	68	
11	NUT, NUT	NR109A	RCA	67	
-1	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR REF. DES.	ITEM NO.

8	000-023-42	LUG, TERMINAL NO. 10	NRS9B	RCA	66
8	000-031-50	INSULATOR, TEFLON	DF3D	RCA	65
16	000-032-50	INSULATOR, MICA	DF6C	RCA	64
12		LUG, TERMINAL NO. 4	810-04-00	SHAW-WALKER	63
10	000-076-50	INSULATOR, SHOULDER BUSHING	01-1-06-005B	CTC ENG	62
5	000-034-50	INSULATOR, MICA	495320	RCA	61
4	000-035-50	SCREW LOCK ASSY (FEMALE)	D 20418-2	CANNON	60
295	000-021-41	CONTACT, CRIMP (FREE)	60-801-03-13	ELCO	59
1	000-017-42	KNOB, AL ALY .093 DIA	KHF900A	ALCO ELEC	58
1	000-010-73	TRANSISTOR, PNP	2N4036		B7 57
2	000-011-73	TRANSISTOR, PNP	2N2102		B6,8 56
1	000-002-73	TRANSISTOR, PNP	2N4902		B2 54
1	000-006-73	TRANSISTOR, NPN	2N5068		B1 53
1	000-001-81	TRANSFORMER, FILAMENT 6.3V	T-52A	HERALD ELEC	T1 52
1	000-014-41	TERMINAL, STRIP (5 PIN)	54 B	CINCH	TB4 51
1	000-018-41	TERMINAL, STRIP (3 PIN)	86 A	H.H. SMITH	TB2 50
1	000-006-41	TERMINAL, STRIP (10 PIN)	3010	H.H. SMITH	TB1 49
1	000-021-42	SPEAKER	PM-1 1/2	CALRAD	LS1 48
1	000-005-78	SWITCH, SLIDE 4 AMP @ 125V	85-85	STACOR	52 47
1	000-004-78	SWITCH, ROTARY	01-1-07-0004	CTC ENG	51 46
1	000-003-78	SWITCH, THERMAL	3150-13-12	ELMWOOD	T51 45
1		RESISTOR, POT 750K, 2W		ALLEN BRADLEY	R17 44
2		RESISTOR, 1K, 1/4 W	RC07GF102J		R15,16 43
2		RESISTOR, 4.7K, 1/4 W	RC07GF472J		R13,14 42
1	000-008-66	RESISTOR, POT 20K, 2W, ±10%			R12 41
2	000-034-65	RESISTOR, .22 Ω, 2W, ±5%			R10,11 40
2	000-038-65	RESISTOR, 1.3 Ω, 1/2 W, ±5%	RC206FIR3J		R8,9 39
1	000-041-65	RESISTOR, 1.5 Ω, 5W, ±5%			R5 38
3	000-040-65	RESISTOR, 10 Ω, 2W, ±5%			R4,7 37
3	000-037-65	RESISTOR, 1.2 Ω, 1/2 W, ±5%	RC206FIR2J	ALLEN BRADLEY	R12,3 36
1	000-003-81	POWER SUPPLY, 15KV		VARO	P51 35
2		LUG, TERMINAL NO. 6	110-0-06-00	H.H. SMITH	34
5	000-022-41	SOCKET, CRYSTAL	RT5-3	CINCH	33
3	000-002-54	HEAT SINK, TRANSISTOR		THERMALLOY	32
5	000-001-54	HEAT SINK, TRANSISTOR TD-3	MC-631-3	WAKEFIELD	31
2	000-012-42	HOLDER, FUSE (CLIP)	35-700-1	LITTLEFUSE	30
1	000-016-42	HOLDER, FUSE	39022	LITTLEFUSE	29
1	000-005-42	GROMMET, 1/2 ID, 3/8 OD, 1/4 TH	1842	ITTAVCO	28
2	000-087-65	RESISTOR, 2 Ω, 10W	VPR10F	CLAROSTAT	R18,19 27
3	000-001-47	FUSE, SLO-BLO 2.5 AMP		BRUSSARD	F1,2,3 26
2	000-011-70	DIODE, RECTIFIER 50 V	MR1120		CR10,11 25
4	000-001-70	RECTIFIER 100 V	MR1121		CR6-9 24
1	000-012-70	ZENER, 39 V	1N2992B		CR5 23
1	000-013-70	ZENER, 120V	1N3008		CR4 22
3	000-010-70	DIODE, ZENER, 150V	1N3011A		CR1,2,3 21
6	000-016-35	CAPACITOR, .05 µF, 50V			CI-C6 20
1		CONNECTOR ASSY (TAPE PLUG)		CTC ENG	PI0 19
1	000-019-41	CONNECTOR, 15 PIN	17-10150-1	AMPHENOL	P15 18
1	000-007-41	.47 PIN (PC CONN)	00-7015-047	ELCO	J14 17
1	000-014-41	.25 PIN (MALE)	17-10250-1	AMPHENOL	J13 16
1	000-003-41	.35 PIN (PC CONN)	00-7015-035	ELCO	J12 15
1	000-016-41	.4 C. JACK	2RF-1	CINCH	J11 14
1	000-010-41	.50 PIN (FEMALE)	17-10500-1	AMPHENOL	J10 13
1	000-013-41	.25 PIN (FEMALE)	17-10250-1	AMPHENOL	J9 12
1	000-011-41	.37 PIN (MALE)	17-20370-1	AMPHENOL	J8 11
1	000-004-41	C.R.T.	57-18 DD	E B Y	J7 10
1	000-002-41	.8 PIN (OCTAL)	MIP 88-8	AMPHENOL	J6 9
5	000-008-41	CONNECTOR, 59 PIN (PC CONN)	00-7015-059	ELCO	J1-15 8
1	000-001-57	BLOWER	N112 F	ROTRON	B1 7
1	000-015-20	GASKET, FAN	01-1-06-002B	CTC ENG	6
2	000-016-20	PLATE, NUT	01-1-06-0009		5
1	000-003-20	BRACKET, COMPONENT MTG	01-1-06-0010		4
1	000-002-20	DUCT, AIR	01-1-06-0011		3
1	000-006-20	BRACKET, REAR	01-1-06-0012	CTC ENG	2
-1	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR REF. DES.	ITEM NO.

Figure 2. Rear Panel Assembly (3 of 3)