2. THE 8500 CPU PRINTED CIRCUIT BOARD (PCB).

Most of the data contained in this Section is for information purposes only as the operating system handles the operations discussed herein. The 8500 CPU PCB has the capability of supporting up to four floppy disk drives and up to two eight-inch hard disks. Figure 2-1 is a matrix map of the 8500 PCB.

2.1 Memory.

The 8500 PCB Memory bank switching allows selection of the bank the DMA will access independently of the bank selected for access by the CPU. Thus, the CPU may be operating in one memory bank when the DMA interrupts to read from or write to another memory bank. This requires two more bits (UN3 and UN4) at port 25.

The ability to swap the fixed 16K address space from high-order memory to low-order memory has been facilitated by a pair of jumpers (S21 and S22), on the PCB at matrix postitions A21 and A22. The write protect function operates on the common memory only, independently of whether common memory is pinned to be in high-order or low-order space.

2.2 The Hard Disk Controller (HDC).

The hard disk controller is a separate PCB that attaches, piggyback, onto the mother board. This allows different types of disk drives to be used. Currently, there are two hard disk controllers that will mount on the mother board:

a. One for the hard-sectored drives such as the SA4000

b. One for the soft-sectored drives such as the SA1000

Neither controller will program exactly the same as the 8200 PCB hard disk controller. See Section 3 for a detailed discussion on the 8500 PCB Controller.

2.3 Floppy Disk Controller (FDC).

When double-sided floppy disk drives are installed, they are pinned for accessability as one logical drive with two heads via the side-select control line.

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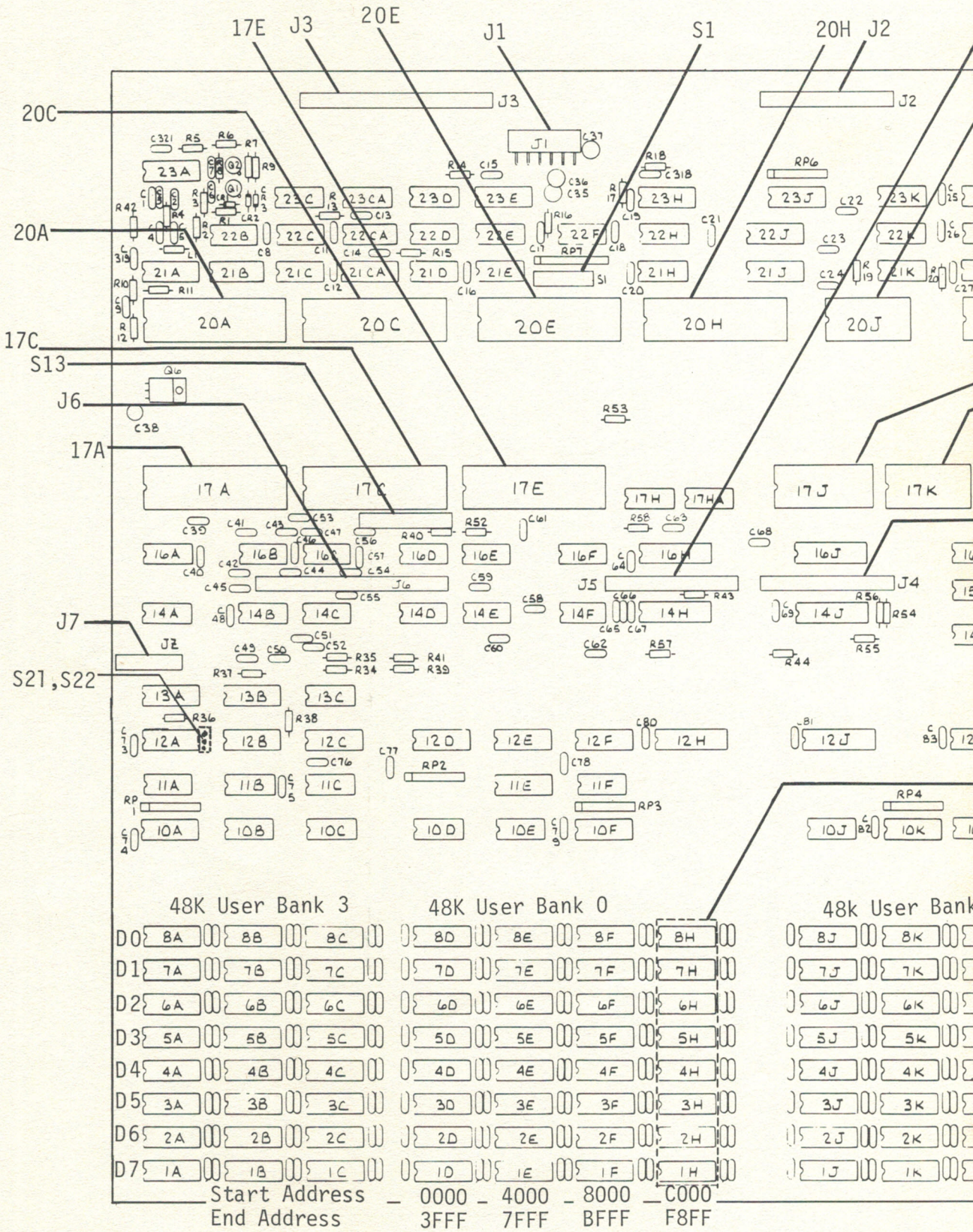
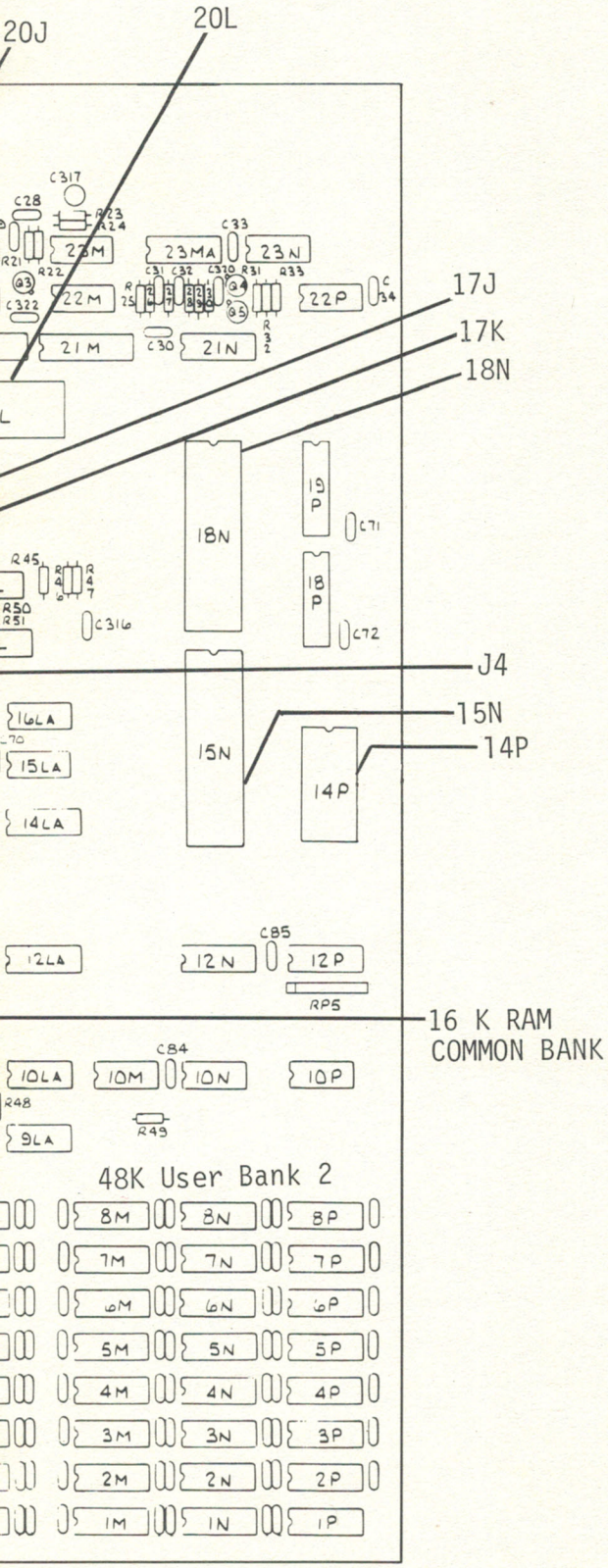
*Refer to the ACS8000 Microcomputer Family User's Manual for information on the 8000 series PCBs.

Start


17E J3 20E J1 S1 20H J2
20C
20A
17C
S13
J6
17A
J7
S21,S22
J3
J2
J1
S1
J4
J5
J6
J7
20A 20C 20E 20H 20J
17A 17C 17E 17H 17HA 17J 17K
48K User Bank 3
48K User Bank 0
48k User Bank
D0 D1 D2 D3 D4 D5 D6 D7
Start Address 0000 4000 8000 C000
End Address 3FFF 7FFF BFFF F8FF



LEGEND: 8500 PC Board

S21, S22 Common Memory:
Top Two Pins Jumpered - Standard
Bottom Two Pins Jumpered - Oasis
J7 High Speed Serial Connector
17A SIO IC Console #4, Printer #2
J6 RS232 Connector to Rear Panel
S13 High Speed Networking Jumper Block
17C SIO IC Console 2 and 3
20A FDC IC 1797
20C FDC PIO IC
17E SIO IC Console #1, Printer #1
J3 FDC Connector
20E PIO IC Memory Bank Select
J1 Power Connector
21F S1 System Configuration Block
20H PIO IC Parallel Printer
J2 Parallel Printer Port
J5 MTU Connector
20J AMD 9511 FPP
20L CTC IC
17J Address Decoder IC
17K CTC IC
18N Z80
J4 HDC Connector
15N DMA IC
14P Version 5.01 EPROM
16K ICs RAM Common Bank

Figure 2-1. 8500 CPU PCB
Matrix Map

2.3 --Continued.

When switching from one floppy drive to another, it is necessary to force unloading of the head-load signal. This insures that, when the newly selected drive is READ from or WRITTEN to, the head load delay one-shot in the controller circuit will be triggered and delay sufficiently for the head of the newly selected drive to settle. This is done by doing a SEEK with the head load flag bit set to unload the head at the beginning.

The FDC IC chip has been changed from the FD1791 to the FD1797. The 1797 chip is able to read to some single-density diskettes that the 1791 cannot.

By changing to the 1797 the meaning of bits 1 and 3 in the READ and WRITE SECTOR commands to the contoller chip have been altered. Bit 1 on the 1791 chip enabled or disabled comparison of the side byte; bit 3 established which side was being compared. Bit 1 on the 1797 establishes which side is being read; bit 3 dynamically alters the code for the sector length field (This is done in conjunction with the sector length byte in the header). Thus, the side select bit changes from bit 3 to bit 1, and the option not to compare is not available. To maintain compatibility with the present sector length field code, bit 3 should be set to bit 1.

The 1797 has an output that can be used to control the side-select line to the disk drive. This happens automatically as determined by bit 1 in the READ and WRITE commands. However, the CPU board is wired to use bit 5 out of the PIO at port 9 to do this selection. If necessary, the signal from the 1797 can beused to control side select by cutting a trace and installinga jumper at S25.

2.4 I/O Port Assignments for the 8500 PCB.

Table 2-1 lists the I/O port assignments with their corresponding schematic reference and functions. Table 2-2 lists the bit assignments for the I/O ports.

Table 2-1. I/O Port Assignments for the 8500 PCB

PORT NUMBER	SCHEMATIC REFERENCE	FUNCTION
00-03	Y0 (DMA)	Initialize DMA.
04	Y1 (FD179X)	Input drive/controller status. Output command.
05	(Floppy disk)	Input/output track number.
06		Input/output sector number.
07		Input data. Output data when WRITING to the disk and the desired track number prior to doing a SEEK.
08	Y2 (PIO-CH A)	Input interrupts from FDC and from HDC. Output floppy disk drive select, side select, and recording density.
09	Y2 (PIO-CH B)	Input END from 9511A, DISK CHANGE, CPU board type and two-sided signal from floppy disk drive. Out put MR to FDC chip.
0A	Y2 (PIO-CH A)	Initialize channel A.
0B	Y2 (PIO-CH B)	Initialize channel B.
0C	Y3 (CTC-CH 0)	Baud rate generator for console number 1 at JY.
0D	Y3 (CTC-CH 1)	not used.
0E	Y3 (CTC-CH 2)	Baud rate generator for printer number 1 at JX.
0F	Y3 (CTC-CH 3)	Used to count index pulses of the floppy disk drive.
10	Y4 (PIO-CH A)	Parallel port I/O at J4 (normally used in I/O mode).
11	Y4 (PIO-CH B)	Parallel port I/O at J4 (normally used for data in an I/O mode).
12	Y4 (PIO-CH A)	Initialize channel A.
13	Y4 (PIO-CH B)	Initialize channel B.
14-17	Y5 (IPL)	An output to any of these ports turns off the PROM after initial program load (IPL).
18	Y6 (9511)	Input/output data from the 9511's stack.
19	"	Input status, output commands to/from the 9511.
1A	"	S/A 18.
1B	"	S/A 19.

Table 2-1. Continued

PORT NUMBER	SCHEMATIC REFERENCE	FUNCTION
1C	Y7 (SIO-CH A)	Input/output data to I/O port at JY (normally
1D	"	Input status of channel A. Output commands to CH A.
1E	Y7 (SIO-CH B)	Input/output data to I/O port at JX (normally printer number 1).
1F	"	Input status of channel B. Output commands to CH B.
20	Y8 (HD DSK)	Output drive and head number to HDC.
21	"	Output sector number and old cylinder number to the HDC; also input and output data to or from the hard disk via the DMA.
22	"	Output new cylinder number to the controller.
23	"	Output commands to the controller. Input status of the controller.
24	Y9 (PIO-CH A)	Input configuration of CPU and controllers.
25	Y9 (PIO-CH B)	Input nothing. Output memory write protect bit and memory bank select bits.
26	Y9 (PIO-CH A)	Initialize channel A.
27	Y9 (PIO-CH B)	Initialize channel B.
28	Y10 (SIO-CH A)	Input/output data to I/O port at JV (normally printer nummber 2 but on the 8500 is reconfigurable as a bisync modem port).
29	"	Input status of channel A. Output commands to CH A.
2A	Y10 (SIO-CH B)	Input/output data to I/O port at JW (normally console number 4).
2B	"	Input status of channel B. Output commands to CH B.
2C	Y11 (SIO-CH A)	Input/output data to I/O port at JT (normally console number 2). Also input/output data to network port.
2D	"	Input status of channel A. Output commands to CH A.
2E	Y11 (SIO-CH B)	Input/output data to I/O port at JU (normally console number 3).
2F	"	Input status of channel B. Output commands to CH B.
30	Y12 (CTC-CH 0)	Baud rate clock for consol number 2 at JT.
31	Y12 (CTC-CH 1)	Baud rate clock for consoles numbered 3 and 4 at JU and JW.
32	Y12 (CTC-CH 2)	Baud rate clock for printer number 2 at JV.
33	Y12 (CTC-CH 3)	Real time clock generator for time slicing the usage of the processor.

Table 2-2. Bit assignments for the I/O ports

PORT	BIT	DESCRIPTION
00-03 (DMA)		(Not applicable).
04-07 (FD179X)		(See the applicable Western Digital data sheet).
08 (PIO-CH A)	7	INTERRUPT input from the HDC.
	6	INTERRUPTinput from the FDC chip.
	5	DRIVE SELECT 4 to select drive D. 0=unselected, 1=selected. Select only one drive at a time.
	4	DRIVE SELECT 3 to select drive C.
	3	DRIVE SELECT 2 to select drive B.
	2	DRIVE SELECT 1 to select drive A.
	1	HLD input from the floppy disk controller chip to indicate when the head is loaded. 0=not loaded; 1=loaded.
	0	DDEN output to set the recording mode. 0=single density, 1=double density.
09 (PIO-CH B)	7	TWO-SIDED input from the floppy disk drive. 0=single-sided diskette, 1=two-sided diskette.
	6	Input (hardwired) to indicate the type of PCB. 0=8500..
	5	Side select output to the floppy disk drives (unless SSO on the controller chip is used). 0=side 0 selected, 1=side 1 selected.
	4	Not connected.
	3	Not connected.
	2	/DISK CHANGE input from the floppy disk drive. (See the disk drive spec sheet for details).
	1	/MR (master reset) output to the floppy disk controller chip. Normally a 1, take 50 seconds to reset.
	0	END, input from the 9511A to indicate the completion of a calculation.
0C (CTC-CH 0)	In	2 Mhz.
	Out	Baud rate for channel A of the SIO that outputs to JY normally console number 1).
0D (CTC-CH 1)	In	2 Mhz.
	Out	Not attached.

Table 2-2. Continued

0E (CTC-CH 2)	In		2Mhz.
	Out		Baud rate for channel B of the SIO that outputs to JX (normally printer number 1).
0F (CTC-CH 3)	In		Index pulses from the selected floppy diskk drives.
	Out		(None).
10 (PIO-CH A)	BIT	7	(Unnamed) normally an input from printer to PIO
		6	SELECT "
		5	BUSY "
		4	PAPER EMPTY "
		3	FAULT "
		2	CNTL normally an output to the printer.
		1	INPUT PRIME "
		0	DATA STROBE "
11 (PIO-CH B)		7	DATA 7 normally an output to the printer.
		6	DATA 6 "
		5	DATA 5 "
		4	DATA 4 "
		3	DATA 3 "
		2	DATA 2 "
		1	DATA 1 "
		0	DATA 0 "
14-17 (IPL)			(Not applicable).
18,19 (9511A)			(See the AMD9511A specification sheet).
1C (SIO-CH A)			(Not applicable).
1E (SIO-CH B)			(Not applicable).
20-23 (Hard disk)			(See the HARD DISK interface specification).
24 (PIO-CH A)			All bits have yet to be assigned. They will be pinned to indicate the type(s) of controllers attached to the CPU board.
25 (PIO-CH B)		7	UN4, MSB of a two bit nibble that sets the bank of memory that DMA accesses.
		6	UN3, LSB of the above nibble.
		5	WRITE PROTECT, output to the hardware to prevent writing into the upper 16K of memory space. 0=not protected, 1=write protected.

Table 2-2. Continued

PORT	BIT	DESCRIPTION
25 (PIO-CH B)	4	UN2, MSB of a two bit nibble that sets the bank of memory that the CPU accesses.
	3	UN1, LSB of the above nibble.
	2	Unassigned.
	1	Unassigned.
	0	Unassigned.
28 (SIO-CH A)		(Not applicable).
2A (SIO-CH B)		(Not applicable).
2C (SIO-CH A)		(Not applicable).
2E (SIO-CH B)		(Not applicable).
30 (CTC-CH 0)	In	2Mhz.
	Out	Baud rate for channel A of the SIO that outputs to JT (normally console number 2).
31 (CTC-CH 1)	In	2Mhz.
	Out	Baud rate for channel B of the SIO that outputs to JU and channel B of the SIO that outputs to JW (normally consoles 3 and 4).
32 (CTC-CH 2)	In	2Mhz.
	Out	Baud rate for channel A of the SIO that outputs to JV (normally printer number 2).
33 (CTC-CH 3)	In	2Mhz.
	Out	(none).

2.5. Z80 Interrupt Daisy Chain.

On the Z80 interrupt chain the SIOs are at the bottom of the chain so they can return from interrupt by a command rather than by RETI instruction which ripples down the daisy chain. See Table 2-3 for the interrupt daisy chain sequence.

Table 2-3. Interrupt Daisy Chain

Top of chain	YO	DMA
	Y2	PIO (Hard disk, Floppy disk and 9511 interrupts)
	Y4	PIO (user's port)
	Y3	CTC (Baud rates and timer)
	Y12	CTC (baud rates and real time clock)
	Y7	SIO (console 1 and Printer 1)
	Y10	SIO (printer 2 and Console 4)
Bottom of Chain	Y11	SIO (Consoles 2 and 3)